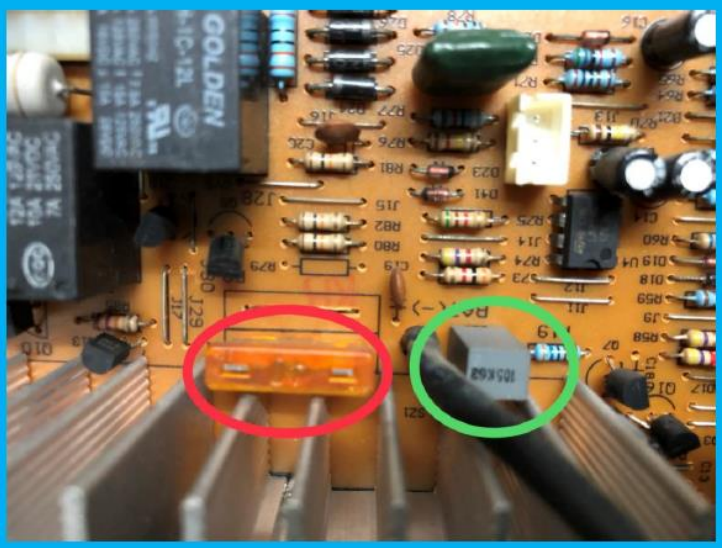
MSCPH509

M. Sc. II[nd] Semester

Electronics



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Course: Electronics **Course code: MSCPH509**

Credit: 3

UNIT 1: Semiconductor devices

Outline of unit 1

1.1 Objectives:

After study of unit the student will be able

i. To study the classification of semiconductor devices and understand the concept of homo and hetro junction devices.

ii. To understand the construction, working, advantages and disadvantages of different semiconductor diodes.

iii. To describe construction and working of solar cell.

iv. To explain different types of clipping and clamping circuits (Wave shaping circuits).

iv) To understand working and uses of voltage regulator.

v) To explain frequency dependence of semiconductor devices Voltage regulator

. vi) To describe application of semiconductor devices

1.2 Introduction: Semiconductor devices

Semiconductors are materials that are neither good conductors nor good insulators means conductivity of such substances lies in between conductor and insulator. Infect at absolute zero temperature they are perfectly insulators. Conductivity of intrinsic semiconductor is too less to be of any practical use however incorporating trivalent or pentavalent impurity and converting intrinsic semiconductor into p type or n type semiconductor makes a revolution in electronic industry.

Using semiconductor materials different electronic components are made that uses the electronic properties of semiconductor materials, like silicon, germanium, and gallium arsenide. Semiconductor devices have almost replaced vacuum tubes in different electronic applications. Instead of using thermionic emission in a high vacuum, semiconductor devices use electronic conduction in the solid state. They are manufactured for both discrete devices and integrated circuits. Because of their reliability, compactness, low cost and wide range of current and voltage handling components semiconductor devices becomes the key element in most of the daily use electronic instruments, industrial control instruments, computing and data processing equipment as well communication devices too.

1.2.1 Classification

Semiconductor devices can be classified according to the no. of terminals in i.e. two terminal, three terminal, four terminal devices etc. The chart given below (Figure 1.1) depicts different types of semiconductor devices and commonly used examples of them.

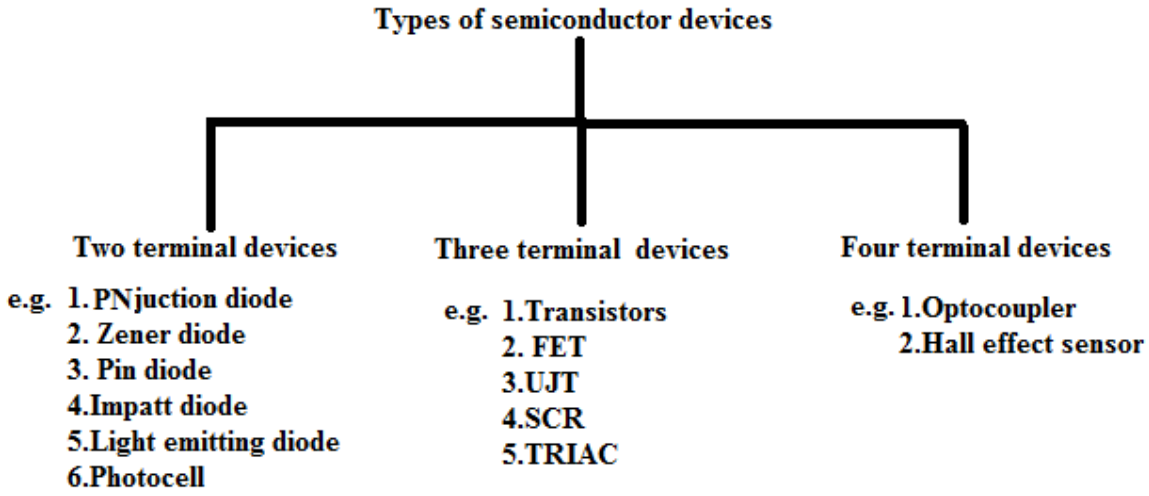


Figure 1.1 Types of semiconductor devices

1.2.2 Homo and hetrojunction devices

In a simplest definition, a homojunction is a junction between the same materials with the same crystalline structure (e.g. silicon with silicon or germanium with germanium) while a hetrojunction is a junction between different materials or between the same materials, but with different crystal structure. (e.g silicon with germanium or nickel with gallium arsenide). Homojunction materials have equal band gaps but their doping may be different. In most practical cases a homojunction occurs at the interface between an n-type (donor doped) and p-type (acceptor doped) semiconductor such as silicon or germanium, generally called a PN

junction. Unlike homojunction devices hetrojunction devices have unequal bandwidths Semiconductor devices like diode can be of any type either homojunction or hetrojunction.

1.3 P-N junction diode

When a P type semiconductor material is suitably in contact with N type material then the interface between the different regions is called PN junction.

1.3.1 Construction & symbol: It is not just like P type material is brought in contact with N type semiconductor.PN junction is fabricated by special techniques. Some of popular fabrication techniques are

a)Diffusion method b)Alloy method

As the junction is formed, the free electron near the junction in N type regions moves across the junction to P region and combine with holes near the junction.Similarly holes move to N junction and this crosses a layer of positive charges towards N type region and a layer of negative charges towards P type region.This region is called deletion layer.(Region of immobile charge carrier due to recombination of hole and electron near the junction).As soon as junction is fabricated depletion layer is formed however it is very thin compared to the N region and P region, Diffusion of the further electron from N type to P type region stops as the depletion layer formed as negative layer towards P types repel further diffusion of electron.

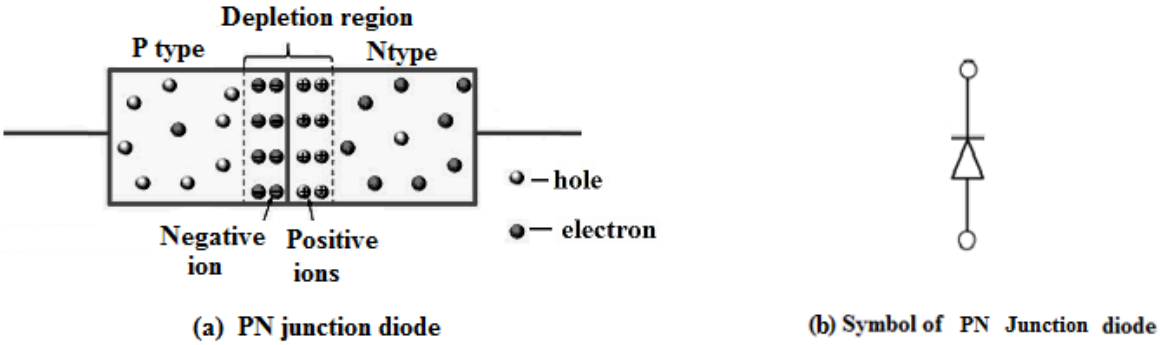


Figure 1.2 PN junction diode and it's symbol

1.3.2 Biasing Schemes:

Forward bias: In forward bias positive terminal of the battery is connected to P type and negative terminal is connected to N type (Figure 1.3(a)). In this case external d.c. voltage is against the field due to potential barrier. As potential barrier voltage is very small (0.3 to 0.7 V),a small forward voltage is sufficient to remove potential barrier. Once potential barrier is eliminated, current can easily flow in the circuit and resistance becomes almost zero. Magnitude of current depends upon the applied forward voltage.

Reverse bias: As shown in Figure 1.3(b) in reverse bias positive terminal of the battery is connected to N type and negative terminal is connected to P type. In this case external d.c. voltage favours the field due to potential barrier. And ideally no current flows(practically a small leakage current flows because of minority charge carriers.

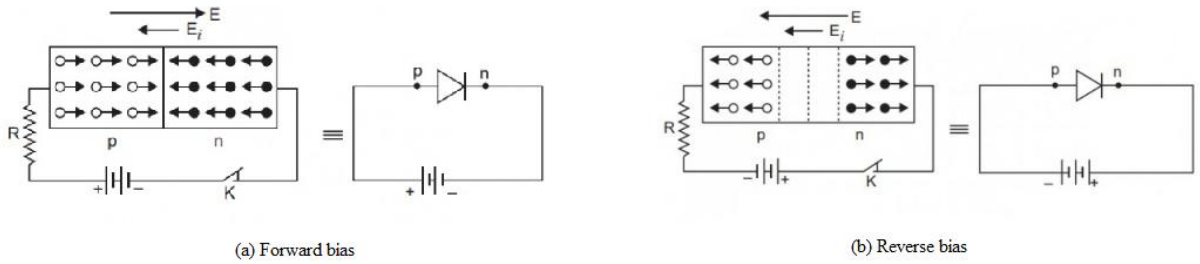


Figure 1.3 Forward bias and reverse bias

1.3.3 Current voltage characteristics of PN junction diode

It is the curve between voltage across the junction taken along X axis and current through the circuit taken along Y axis(Figure 1.4).

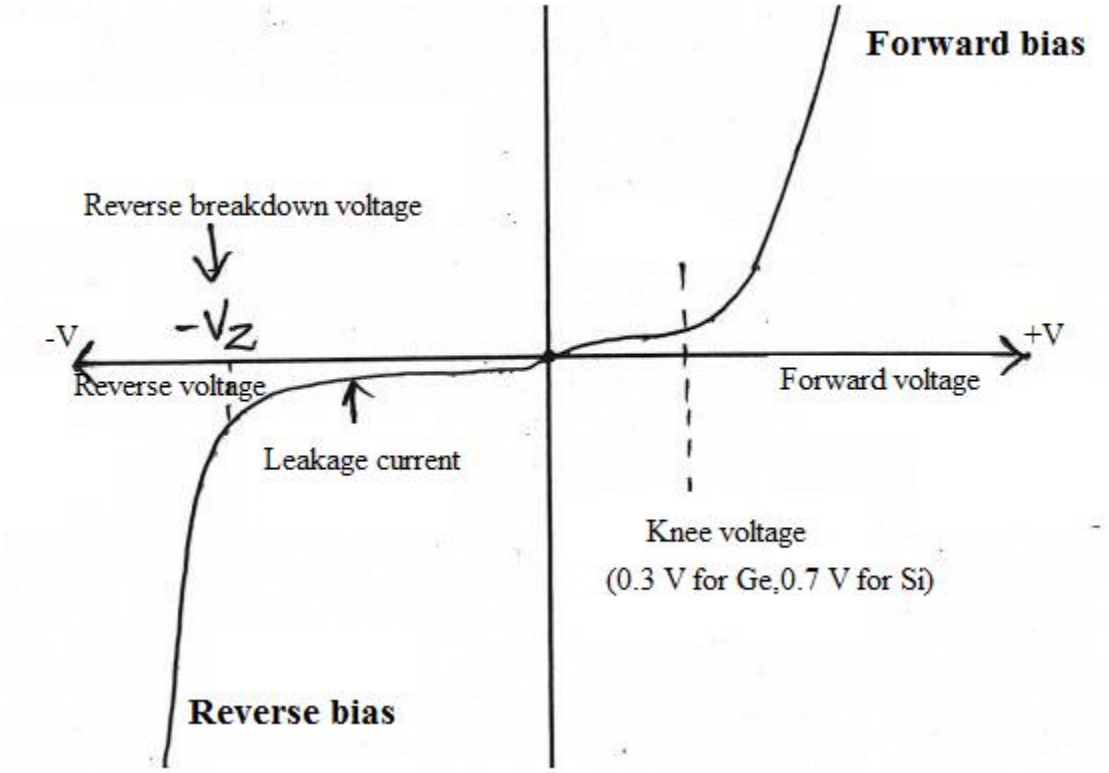


Figure 1.4 V-I characteristics of PN junction diode

As shown in the Figure 1.4, when P-N junction is forward biased, by connecting positive terminal of battery to P-type and negative terminal to N type material of diode, almost no current flows initially until the potential barrier overcome. With the further increase in applied forward voltage the current increases with the increase in applied voltage and the curve shows linear variation. But as the applied voltage of about 3 volt, the majority charge carrier crossing the junction gain

sufficient kinetic energy to knock out valence electrons bound to the crystal lattice and raise them to the conduction band.

1.3.4 Uses of PN junction diode

1. In power supplies as a rectifier, voltage multiplier, voltage regulator circuits etc.

2. In wave shaping circuits like clipping and clamping circuits.

3 In digital circuits. Etc.

Example 1.1. A P-N junction silicon diode conducts 240 mA current when a forwardvoltage 0.8 volts is applied.Find Current for forward voltage of 0.7 volt.

Solution: From PN junction diode equation
$I=I_0(eV_e/\eta kT-1)$
$kT/e=(1.38x10\text{-}23x300)/(1.6x10^{-19})=0.026$ volt considering $T=27^0C$ or 300 K
For silicon $\eta=2$
So $I=I_o(e^{0.8/(2\ x\ 0.026)}$ for $V_e=0.8$ V
And $I'= I_o(e^{0.7/(2\ x\ 0.026)}$ for $V_e=0.7$ V

$$\therefore \frac{I}{I'} = \exp\frac{2 \times 0.026}{0.7 - 0.8}$$

$$I' = I \exp\frac{0.7 - 0.8}{2 \times 0.026}$$

$I' = 240 \exp\frac{0.7-0.8}{2\times0.026}$=35 mA

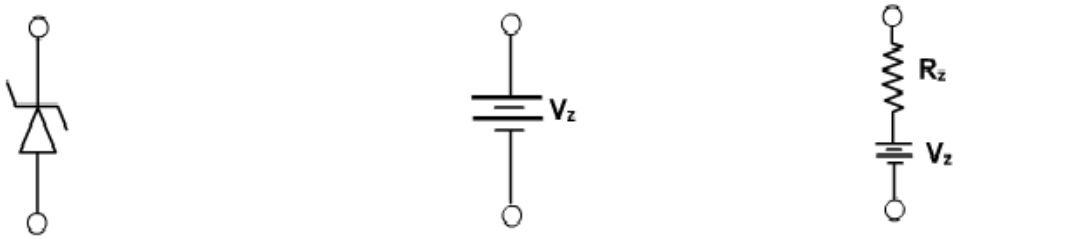
1.4 Zener diode

It is heavily doped PN junction diode which works in breakdown region under reverse bias condition.

1.4.1 Construction & symbol: Zener diode is like an ordinary PN junction diode except it is properly doped so that to have a sharp breakdown voltage .For heavily doped diode the depletion layer is very narrow and when the reverse bias across the diode is increased, breaking of covalent

bonds takes place by the intense electric field set up across the depletion layer. It results in the production of a large number of electron hole pair and reverse current increase .

The circuit symbol for a zener diode is shown in Figure 1.5. We see that the bar of PN junction diode is turned into Z shape in zener diode.



(a) Symbol of zener diode (b) Ideal zener diode (c) Practical zener diode

Figure 1.5 Zener diode: symbol and equivalent circuit

1.4.2 Equivalent circuit As shown in Figure 1.5 (b), since in breakdown region the voltage V_Z remains constant but current increases, an ideal zener diode can be represented by a battery of voltage V_Z under such condition the zener diode is said to be in the ON state. However if the reverse bias voltage is less than zener breakdown voltage no current flows under such condition the zener diode is said to be in the OFF state. However in practical zener diode the breakdown characteristic is not perfectly straight so a series resistance is introduced which represents zener resistance (fig 1.5 (b)). Only small leakage current flows in practical zener diode when reverse bias voltage is less than zener breakdown voltage.

1.4.3 Current voltage characteristics of zener diode Like an ordinary diode the V-I characteristic of zener diode can be studied in forward bias and reverse bias condition (Figure 1,6). In forward bias condition the characteristic of zener diode is just like an ordinary PN junction diode. Similarly just like a PN junction diode in reverse bias condition, minute current flows

because of the minority charge carriers and when the reverse bias is gradually increased a point is released when the junction breakdown and reverse current increases abruptly this is called breakdown region and this breakdown voltage is called zener voltage and the reverse current is known as zener current the general voltage depends upon the amount of doping. Heavily doped diode has a narrow depletion layer which makes a lower breakdown of zener voltage. For the lightly doped zener diode zener voltage will be obviously higher.

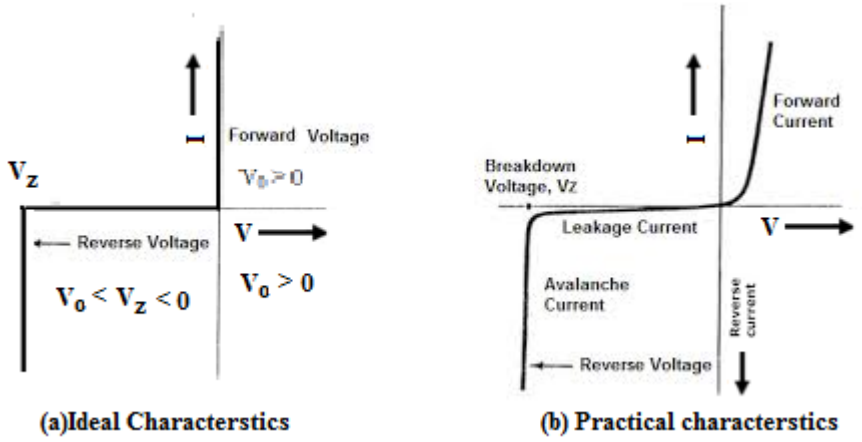


Figure 1.6 V-I characteristics of Zener diode

1.4.4 Uses of zener diode When a zener diode is operated in the breakdown region the voltage across the diode reveals almost constant and is equal to the zener voltage for the large change in the reverse zener current. Hence in this region zener can be used as constant voltage source for stabilizing a voltage at a predetermined value. Some important application of the zener as voltage regulator, as a fixed voltage reference in a network for biasing and comparison for calibrating voltmeter,for avoiding accidental application of excessive voltage.

Example 1.2. A zener diode has a breakdown voltage of 9 volts with a maximum power dissipation of 360 milliwatts.calculate the maximum current the diode can handle?
Answer : for zener diode $P_{max}=V_z.I_z(max)$

Hence maximum current the zener diode can handle

$I_z(max)= P_{max}/V_z=360 \times 10^{-3} /9=40$ mA

1.5 Light emitting diode:

As the name suggests a light emitting diode (LED) is a specially made forward biased PN junction diode which emits visible light when energized (Forward biased) and block the flow of current in reverse direction.

They are made from a very thin layer of fairly heavily doped semiconductor material which is colorless and the light is used through the junction of the diode.

1.5.1 Construction and symbol: At first N type layer is grown on substrate. As the recombination of the charge carrier occurs in the p type material, hence P type material is deposited on it by the process of difision.Metal contacts(anode) are made at the outer edge of the P layer so tht more upper surface is left free for light to escape.For cathode connection metal film is coated at the bottom of the substrate.it also reflects as much light as possible to the surface of the device.When forward biased such a specially made PN junction diode (LED) gives emission in the visible region by a proper choice of band gap and the material.

In general LED are made by using elements like gallium, arsenic or phosphorous.by varying the quantities of these elements,it is possible to produce light of different wavelengths (colours).e.g. LED produces a red light if manufactured using gallium arsenide,and green light if made with gallium phosphide.

Figure 1.7(b) shows the schematic symbol for a LED.the arrows are shown as pointing away from the diode,indicating that light is being emitted by the device when forward biased. However the symbol is same for all LED even with different colours.

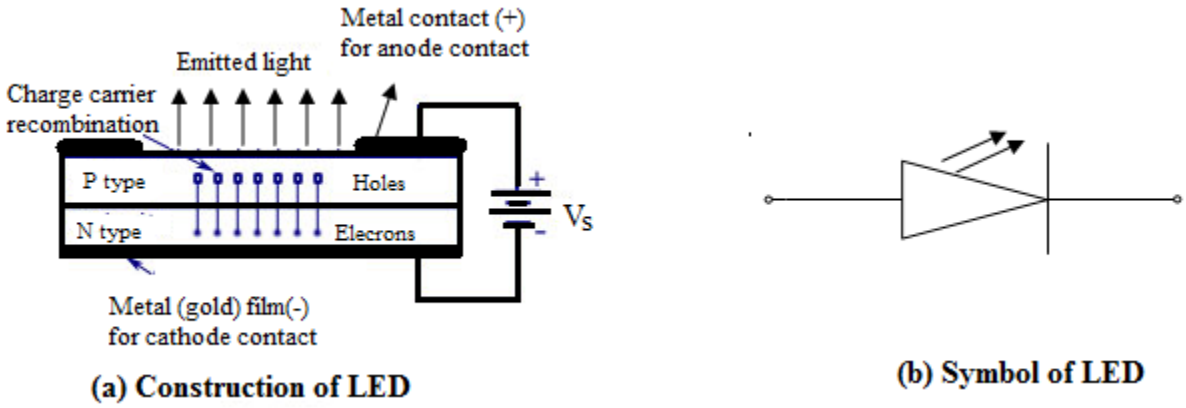


Figure 1.7

1.5.2 Theory: When the LED is forward biased,the potential barrier lowered and the majority charge carriers start crossing the junction. The electrons from N type material cross the pn junction and recombine with Holes in the P type material. as these conduction band electrons, which are at a higher energy level than the valence band holes,recombines with holes the recombining electrons release energy in the form of heat and light.

If Eg is the semiconductot band then the energy Eg=hc/λ may be emitted in the form of radiation.The corresponding emission wavelength is given by

λ=hc/eg.

For GaAs,band gap Eg=1.45 eV and we get

$\lambda = \frac{hc}{E_g} = \frac{6.64\times10^{-34}\times3\times10^{8}}{1.45\times1.6\times10^{-19}} m = 8500\ A^0$ which lies in the infraredregion.

But for For GaAsP,band gap Eg≈1.9 eV and we get

$\lambda = \frac{hc}{E_g} = \frac{6.64\times10^{-34}\times3\times10^{8}}{1.9\times1.6\times10^{-19}} m = 6500\ A^0$ which lies in the vigible (red or yellow amber).

Thus by a proper choice of band gap and the material,radiation of desired wavelength can be obtained.

In germanium and silicon diode almost all the energy is given up in the form of heat and emitted light is insignificant.However,in materials,like gallium arsenide, the number of photons of light energy is sufficient to produce quite intense light.

Figure 1.8(a) shows the graph between radiated light and the forward current of the LED.It is clear from the graph that the intensity of radiated light is directly proportional to the forward current of LED.

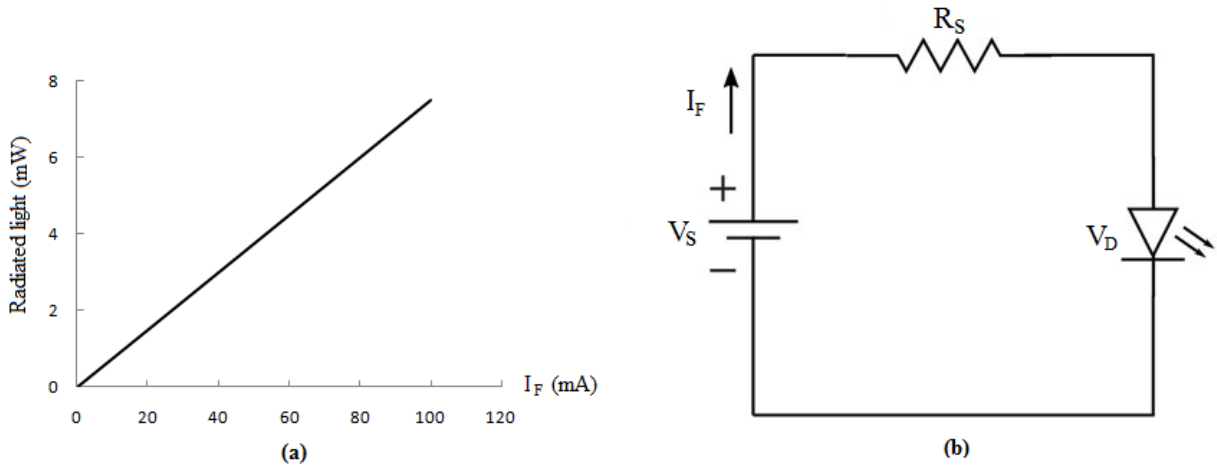


Figure 1.8

The forward voltage rating of most LED is from 1 V to 3 V and forward current ratings range from 20 mA to 100 mA.In order that current through the LED doesn't exceed the safe value,a resistor R_S is connected in series with it as shown in Figure 1.8(b)

Example 1.3 calculate the value of series resistance required to limit the current through a LED to 20 mA with a forward voltage drop of 1.4Vwhen connected with 8 V supply.

Answer Series resistance $R_s = (V_s - V_d)/I_f$

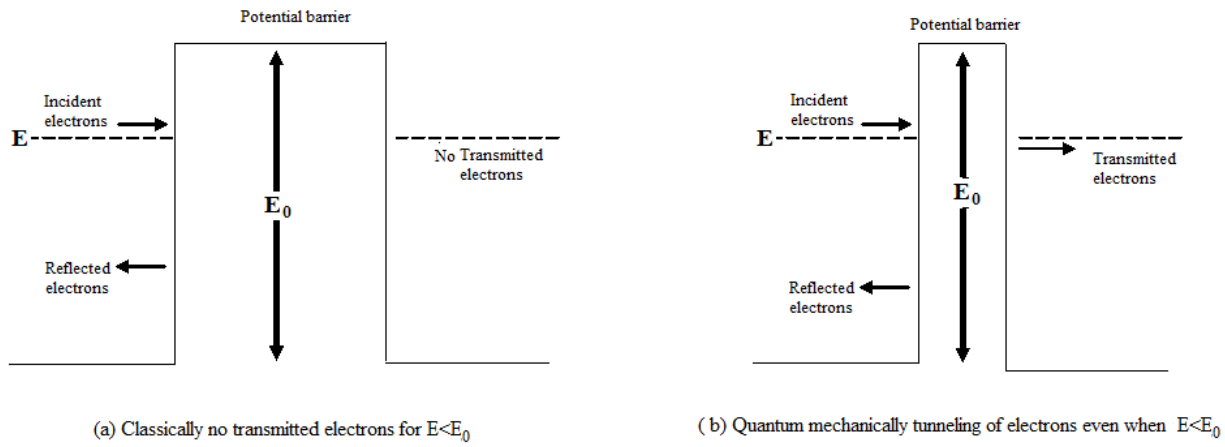
Given V_s=8 V, V_d=1,6 V,I_f=20 mA=20 x 10^{-3}A

Hence R_s =(8-1.6)/ 20 x 10^{-3}=320 Ω

1.6 Tunnel diode:

It is a highly doped PN junction diode which utilizes the phenomenon of tunneling of charge carriers through the junction potential barrier. Tunnel diode was invented by Japanese scientist Leo Esaki in 1958 hence also known as Esaki diode.

1.6.1 Tunneling effect: Classically a particle must have an energy at least equal to the height potential of barrier to cross it to the other side however according to quantum mechanics there is still a small finite probability **of** penetrating the potential barrier by the subatomic particle having energy less than potential barrier. Such crossing of a higher potential barrier by subatomic particle is called tunnel effect(Figure 1.9).



(a) Classically no transmitted electrons for $E<E_0$

(b) Quantum mechanically tunneling of electrons even when $E<E_0$

Figure 1.9

The probability of penetrating through the potential barrier decreases exponentially with the width of the barrier as well as barrier height. Barrier width is decreased by increasing the doping concentration as in the case of tunnel diode. A conventional P-N junction diode has the depletion layer of the order of 5 microns with impurity doping concentration is 1 part in 10^8. So the charge carrier must have energy 0.3 eV for Ge and 0.7 eV for Si to overcome the potential barrier However in tunnel diode the concentration of impurity atom is greatly increased (≈1 part in 103)

to decrease the width of depletion layer to a very small value (≈100 A^0), which induces the tunneling effect and due to tunneling effect the characteristics of tunnel diode are completely changed.

1.6.2 Construction and symbol A tunnel diode is a heavily doped P-N junction diode. Because of heavy doping of P and N regions of the diode width of the depletion layer reduces to extremely small value (≈100 A^0).Due to the extremely thin depletion layer, electrons are capable of tunneling through from one side of the junction to the other at relatively low forward bias voltage, even less than 0.5 volt. Also the electric field in the depletion region becomes so intense that the junction is in a state of zener breakdown with almost no voltage. Tunnel diodes are commonly made from germanium or gallium arsenide(GaAs) and gallium antimonide(GaSb).

The circuit symbol for a tunnel diode is shown in Figure 1.10(b) As it is a low power device, it can be easily damaged by heat and static electricity, hence must be handled with caution.

Figure 1.10 Symbol of tunnel diode

1.6.3 The volt-Ampere (V-I) characteristics of tunnel diode

Figure 1.11 shows the V-I charactersics of a Tunnel diode which is quite different from normal P-N junction diode and shows negative resistance section between point P and V.

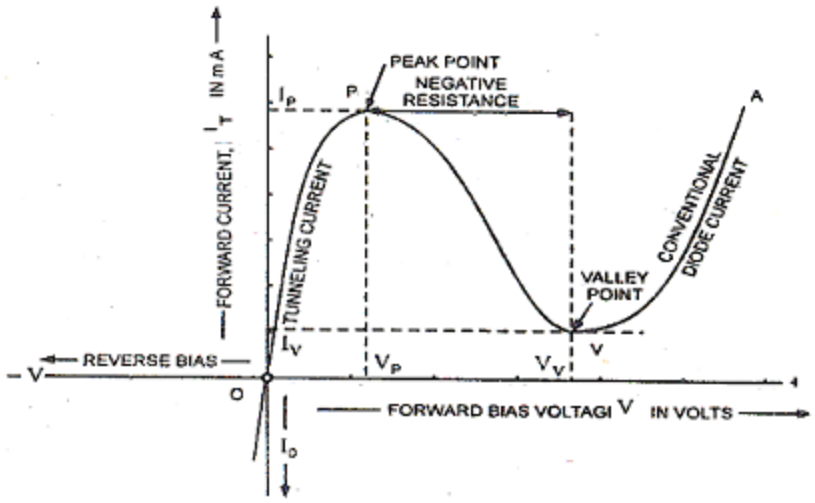


Figure 1.11 (V-I) characteristics of tunnel diode

Region OP (tunneling current section) Initially as the forward voltage across the tunnel diode is increased from zero, electrons from the n type region tunnel through the potential barrier to the p type region with the increase in forward voltage the tunnel diode current also increases until it reaches the peak point P.This is due to region of high doping which results very narrow depletion region hence very high electic field (E=V/D) across the junction and allows carriers in the valence energy band on one side of the junction to tunnel through to the conduction band on the other side of the junction without overcoming the potential barrier(tunneling effect).

Region PV (Negative resistance region) As the voltage is increased beyond peak voltage V_P,the tunneling action starts decreasing and tunnel diode current decreases until it reaches the valley point V.Between point P and point V as the forward bias is increased the current decreases i.e.the diode exhibits negative resistance.

Region VA(Behaving like a normal diode): Beyond valley point voltage, further increase in forward voltage causes increase in tunnel diode current . Again as in any normal pn junction diode because the tunneling effect ceases.

Though a tunnel diode has a high current but operation under this condition is not generally used.

1.6.4 Application of tunnel diode: A tunnel diode can be used as an oscillator in the negative resistance region as it will generate power if operated over this region. It can also be used as microwave oscillator at a frequency of about 10 GHz because of its extremely small capacitance and inductance.They are used in a switiching devicde in computers also having switching time of the order of nanosecond.

1.7 Photo diode:

It is a two terminal semiconductor P-N junction diode which works in reverse bias region and respond to photon absorption.

Principle: when a reverse biased P-N junction diode is illuminated with light, additional electron holes are generated in both P and N regions. It results a very large change in minority carriers concentration and reverse current through the diode increases and varies linearly with the light flux. In this way we can detect light using a reverse biased P-N junction diode known as photo diode.

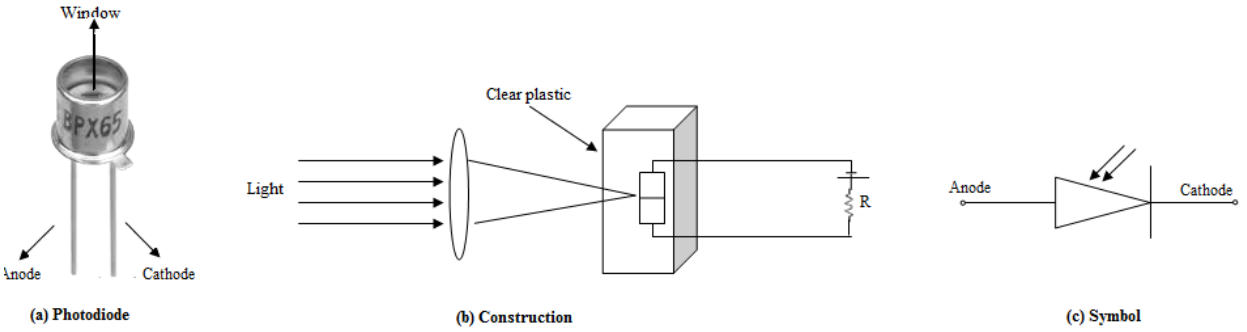


Figure 1.12

1.7.1 Constructionand symbol: Photo diode consists of a P-N junction embedded in a clear plastic capsule(Figure 1.12) radiation is allowed to fall upon one surface across the junction. The remaining sides other sides are either painted black or enclosed in a metallic case. Dimension of

photodiode is only of the order of few mm.The schematic symbols for a photo diode is represented in Figure 1.12(c).The inward arrows represent the incoming light.

1.7.2 Working: in reverse biased photodiode, a reverse saturation current flows due to thermally generated hole and electrons moving across the junction as minority carriers. When light is allowed to incident on the diode surface, temperature of the junction is increased and more and more additional hole – electron pairs are created and reverse saturation current increased.

1.7.3 Volt ampere characteristics: Figure1.13(a) shows the volt ampere characteristics curve for different illumination value. The graph clearly shows that for a given reverse biased voltage V_R the reverse current I_R increases as the illumination (E) on the pn junction of photo diode is increased.

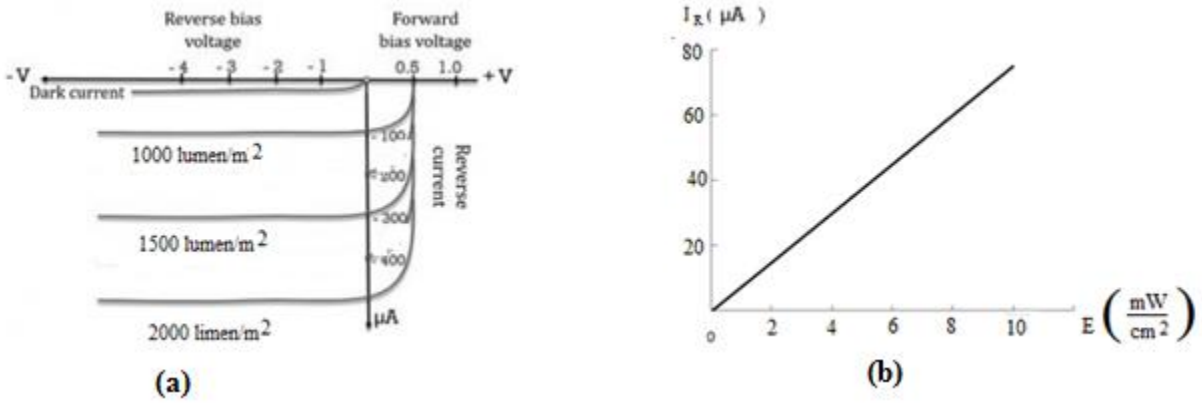


Figure 1.13

Figure1.13 (b) shows the graph between reverse current I_R and illumination E of a Photo diode, The graph is a straight line passing through the origin.

IR= mE
Where m=slope of the straight line
The quantity m is called the sensitivity of the photo diode.

1.7.4 Applications

(a) In alarm circuits
(b) Counter circuit in conveyer belt

(c) For light detection in light operated switches, reading of computer punched cards and tapes etc.
(d) In optical communication systems
(e) In instrumentation, control, automation and communication.

1.8 Solar cell:

A **solar cell** is an electrical device that converts light energy into electrical energy through the photovoltaic effect. It is a form of photoelectric cell, whose electrical characteristics – such as current, voltage, or resistance – vary when exposed to light.

Just like the cells in a battery, the cells in a solar panel are designed to generate electricity; but where a battery's cells make electricity from chemicals, a solar panel's cells generate power by capturing sunlight instead. They are sometimes called **photovoltaic (PV)** cells because they use sunlight ("photo" comes from the Greek word for light) to make electricity (the word "voltaic" is a reference to Italian electricity pioneer Alessandro Volta, 1745–1827).

1.8.1 Construction: A solar cell is basically a p-n junction diode, although its construction is little bit different from conventional p-n junction diodes (Figure 1.14). A very thin layer of p-type semiconductor is grown on a relatively thicker n-type semiconductor. After that a few finer electrodes on the top of the p-type semiconductor layer are applied.

These electrodes do not obstruct light to reach the thin p-type layer. Just below the p-type layer there is a p-n junction. We also provide a current collecting electrode at the bottom of the n-type layer. We encapsulate the entire assembly by thin glass to protect the **solar cell** from any mechanical shock.

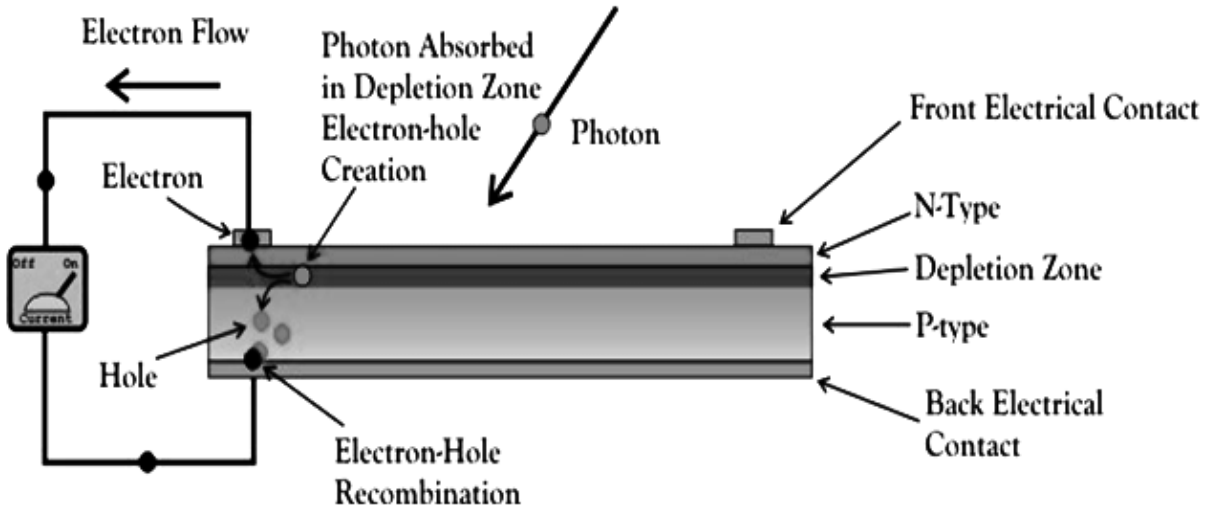


Figure 1.14

The materials which are used for this purpose must have band gap close to 1.5ev. Commonly used materials for manufacturing solar cells are silicon(Si),Gallium arsenide (GaAs), Cadmium telluride (CdTe),Copper indium selenium(CuInSe2) etc.

Generally the selection of material used to construct the solar cell is based on following criterion

1. It must have band gap from 1ev to 1.8ev.
2. It must have high optical absorption.
3. It must have high electrical conductivity.
4. The raw material must be available in abundance and the cost of the material must be low.

1.8.2 Working Principle of Solar Cell

We can think of light as a bundle of photons, so a beam of sunlight is like a fire hose shooting trillions upon trillions of photons our way. When a solar cell is placed in its path and catches these energetic photons ,It converts them into a flow of electrons—an electric current. Each cell generates a few volts of electricity,.

Actually When light reaches the p-n junction, the light photons can easily enter in the junction, through very thin p-type layer. The light energy, in the form of photons, supplies sufficient energy to the junction to create a number of electron-hole pairs. The incident light breaks the thermal equilibrium condition of the junction. The free electrons in the depletion region can quickly come to the n-type side of the junction.

Similarly, the holes in the depletion can quickly come to the p-type side of the junction. Once, the newly created free electrons come to the n-type side, cannot further cross the junction because of barrier potential of the junction.

Similarly, the newly created holes once come to the p-type side cannot further cross the junction became of same barrier potential of the junction. As the concentration of electrons becomes higher in one side, i.e. n-type side of the junction and concentration of holes becomes more in another side, i.e. the p-type side of the junction, the p-n junction will behave like a small battery cell. A voltage is set up which is known as photo voltage. If we connect a small load across the junction, there will be a tiny current flowing through it.

1.8.3 Advantages of Solar Cell

1. No pollution associated with it.
2. It must last for a long time.
3. No maintenance cost.

Disadvantages of Solar Cell

1. It has high cost of installation.
2. It has low efficiency.
3. During cloudy day, the energy cannot be produced and also at night we will not get solar energy.

1.8.4 Uses of Solar Generation Systems

1. It may be used to charge batteries.
2. Used in light meters.
3. It is used to power calculators and wrist watches.
4. It can be used in spacecraft to provide electrical energy.

1.9 IMPATT diode:

The IMPATT diode or IMPact ionisation Avalanche Transit Time diode is an RF semiconductor device that is used for generating microwave radio frequency signals.

It is an active solid-state device that operates by a reverse bias adequate to cause avalanche breakdown. This is a high-power diode and a very powerful microwave source that is used in high-frequency electronics and microwave devices. They may be operated at frequencies up to about 350 GHz when manufactured with silicon.

Dynamic negative resistance shown by the IMPATT diode characterstics is required for microwave oscillation and amplification applications. This is due to the following two reasons:

Impact Ionization avalanche effect: This causes the carrier current to lag behind the ac voltage by 90 degrees.

Transit time effect: This cause a further time delay and causes the external current to lag behind the ac voltage by a further 90 degrees.

The summation of delay involved in generating avalanche current multiplication along with delay due to transit time through drift space provides the necessary 180° phase difference between the applied voltage and the resulting current in an IMPATT diode.

1.9.1 Construction and working

These devices can be classified as follows:

Single drift devices: Devices such as P^+NN^+, N^+PP^+, P^+NIN^+, and N^+PIP^+ come under this category. Consider the P^+NN^+ device. In this device, when the P^+N junction is reverse biased, it causes an avalanche breakdown. This causes the P+ region to inject electrons into the NN^+ region. These electrons move with a saturated velocity. However, the holes injected from the NN^+ region do not drift. Hence, these are called ***single drift devices***.

Double drift devices: The example of a double drift device is P^+PNN^+. In this device, when the PN junction is biased near an avalanche breakdown, electrons drift along the NN^+ region and holes drift along the PP+ region. Hence, they are called ***double drift devices***.

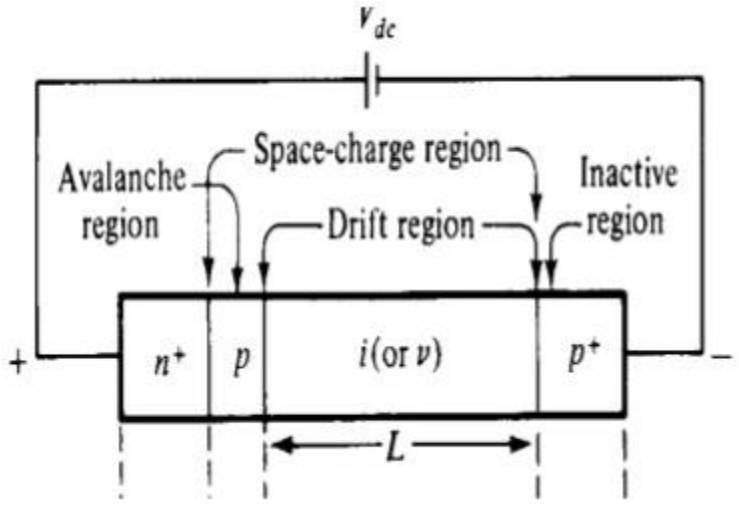


Figure 1.15 Construction of IMPATT diode

1.9.2 Principle of Operation of IMPATT Diode

To understand the operation of an IMPATT diode, here we consider the N^+PIP^+ diode (Fig.. Let V_b be the reverse bias breakdown voltage that is applied to the IMPATT device. Assume that a sinusoidal waveform $V_1 \sin \omega t$ is superimposed on V_{dc}, resulting in a total device voltage V (t) = ($V_{dc} + V_1 \sin\omega t$) as shown in the figure 1,16 below.

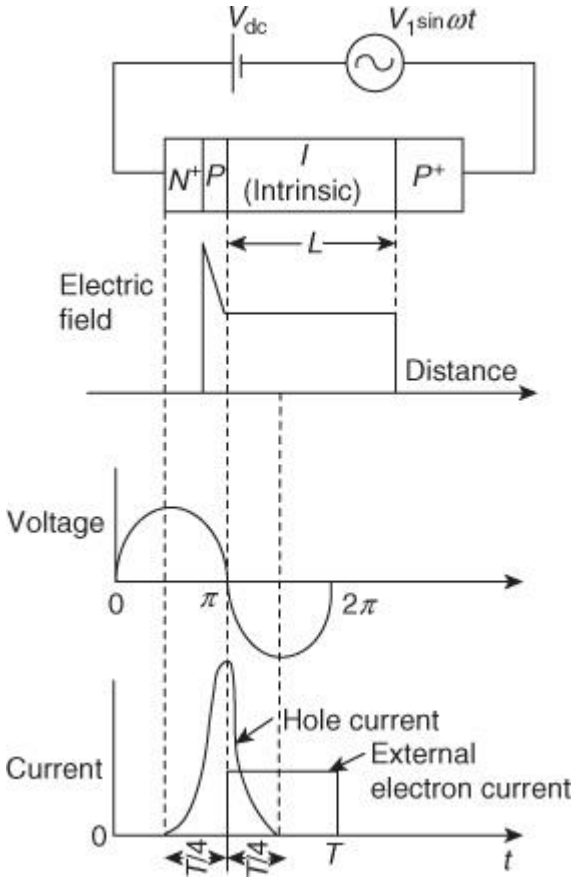


Figure 1.16 IMPATT diode operation

1.9.3 Working of IMPATT diode

Initially, the device contains a few thermally generated free electrons. When $V_{(t)} > V_b$ breakdown occurs at the N^+P junction, these electrons gain energy from the applied voltage and knock off electrons in the valence band to the conduction band. As a result, a new electron-hole pair is created. An electron-hole pair generated because of such impact ionization is called a secondary electron-hole pair.

These secondary electrons again pick up sufficient energy and generate more secondary electron-hole pairs. Therefore, as long as $V_{(t)} > V_b$, the number of carriers increases exponentially, even beyond the voltage maximum irrespective of the magnitude of V(t).

This is because of the sufficient number of secondary electron-hole pairs presence. This exponential increase continues until the sine wave crosses zero and then drops exponentially until the sine wave reaches its negative peak. This avalanche current (generated holes) is injected into the I-region and drifts toward the P^+ region with saturated velocity along the depletion region. The electrons move toward the positive terminal. In this way, this current will have a one-quarter period (T/4) delay or a 90° phase shift with regard to the applied signal voltage.

To achieve the desired 180° phase shift between input voltage and external current, additional T/4 delay is essential. This is made available by the hole drift along the depletion region. It is the property of semiconductor materials that the drift velocity tends to be constant at high field strengths. Since the holes move at the constant velocity v_d, the device length may be chosen to provide the necessary delay for a 180° phase shift between the device voltage and current, which is given by

$$l = v_d \frac{T}{4}$$

Equivalent Circuit:

The IMPATT diode equivalent circuit is as shown in the figure 1.17 below. It is composed of two parts that are the avalanche and drift regions, and a loss resistance (R_s). One part of the equivalent circuit is the avalanche region it consists of a resonant circuit, with an avalanche inductance (L_a) and a capacitance (C_a). The avalanche capacitance is given by:

$$c_a = \epsilon_s \frac{A}{w_a}$$

where,

- w_a is the width of the avalanche region,
- ε_s = permittivity of the dielectric, and

- A is the area.

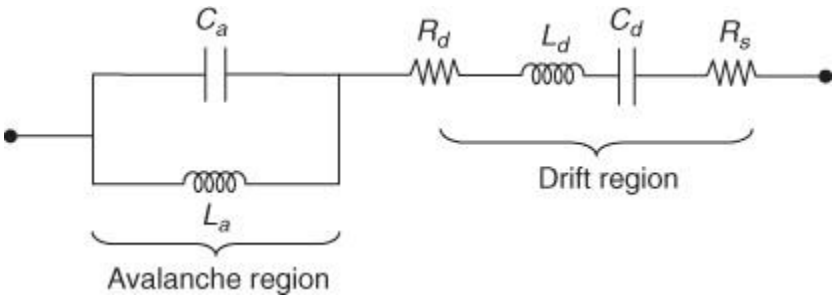


Figure 1.17 Equivalent circuit of IMPATT diode

The IMPATT diode exhibits negative resistance for frequencies higher than the avalanche resonant frequency (f_a), and is given by

$$f_a = \frac{1}{L_a C_a}$$

1.9.4 Characteristics of IMPATT Diode

- IMPATT diode operates in reverse bias. It exhibits a negative resistance region due to the impact of avalanche and transit time effects.
- The phase difference between voltage and current is 180°. Here 90° phase delay is due to the avalanche effect, and the remaining 90° is due to transit time effect.
- It is a narrow-band amplifier that provides output power in the millimeter-wave frequency range.
- At low frequencies, their power output is inversely proportional to frequency. At high frequencies, their power output is inversely proportional to the square of the frequency.
- They are often used in the design of oscillators and amplifiers when the high output power is required. They provide higher output power than Gunn diodes.
- IMPATT diodes are manufactured in Si, GaAs, and InP. They can be operated up to 350 GHz when manufactured in Si.

- These diodes are of low cost, reliable, and compact. They are moderately efficient milliwatt power sources.
- These are noisier than Gunn diodes. Therefore, they are rarely used for local oscillators in receivers.

1.9.5 Performance characteristics

- Theoretical, $\eta = 30\%$ ($< 30\%$ in practice) and 15% for Si, 23% for GaAs
- Frequency: 1 to 300 GHz
- Maximum output power for a single diode: 5W in X band to 6.5 W at 30 GHz
- Several diodes combined: 40 W in X band
- Pulsed powers = 4 kW

Disadvantages of IMPATT diode

- In terms of noise figure an IMPATT diode is not good as in comparison with the TWT amplifier or Gunn diode oscillator or klystron tube. Because the avalanche is a high noise process, so the IMPATT is very noisy diode, the value of noise figure is 30 dB.
- In IMPATT diode matching is difficult because of the low value of their negative resistance.
- It is sensitive to operational conditions.
- It has large electronic reactance, which can cause detuning or burn out the device if proper care is not taken.

1.9.6 Applications of IMPATT Diode

- IMPATT diodes are used as microwave oscillators in microwave generators, in modulated output oscillators.

- They are used in microwave links, continuous-wave radars, and electronic countermeasures.
- IMPATT diodes are also used as amplification with negative resistance. In police radars, low power transmitters, and intrusion alarm devices are used the high-Q IMPATT diodes. In frequency modulated telecommunication transmitters and continuous wave Doppler radar transmitters are used the low-Q IMPATT diodes.

1.10 Clipping circuits:

Clipping circuits are kind of waveform circuits which change the input waveform by removing or flipping a portion of the applied input wave. Clipping circuits are widely used in radar, digital as well as in another electronic system. They can remove signal voltages above or below specified level. Important kind of diode clippers are i) Positive or negative clipper ii) Biased clipper and iii) Combination clipper

1.10.1 Positive and negative clipper: A positive clipper is that clipping circuits which removes the positive half cycle of the input voltage just like a half wave rectifier as shown in the figure the output voltage has clipped of the positive half cycle. Similarly A negative clipper removes the negative half cycle(Figure 1.18).

1.10.1.A) Working of circuit: During the positive half cycle of the input voltage the diode is forward biased therefore it conducts and the voltage across the diode, which in the on conditions behaves as a short circuit ,will be equal to the input voltage .hence voltage drop across the load resistance R_L will be zero hence output voltage during positive half cycle is zero .Also during the negative half cycle of the input voltage the diode now becomes reverse biased and behaves as an

open hence there will be no potential drop across the diode and input voltage will be developed across load resistance and is equal to $-V_m$.

Negative clipper: Just like positive clipper the working of the negative clipper can also be explained likewise. The only change to be done is to reverse the polarities of the diode so that now the diode will clip out only the negative half of the input voltage.

Working of the Negative clipper Now during the positive half cycle of the input voltage diode is reverse biased and acts like open circuit there the voltage across the diode will be zero and across R_L it will be approximately equal to the input voltage . Similarly during the negative half cycle of the input voltage the diode is forward biased and behaves as a short circuit and conduct therefore the voltage across the diode during the negative half cycle is maximum and across the load R_L it is zero ,hence output voltage during negative half cycle is zero.

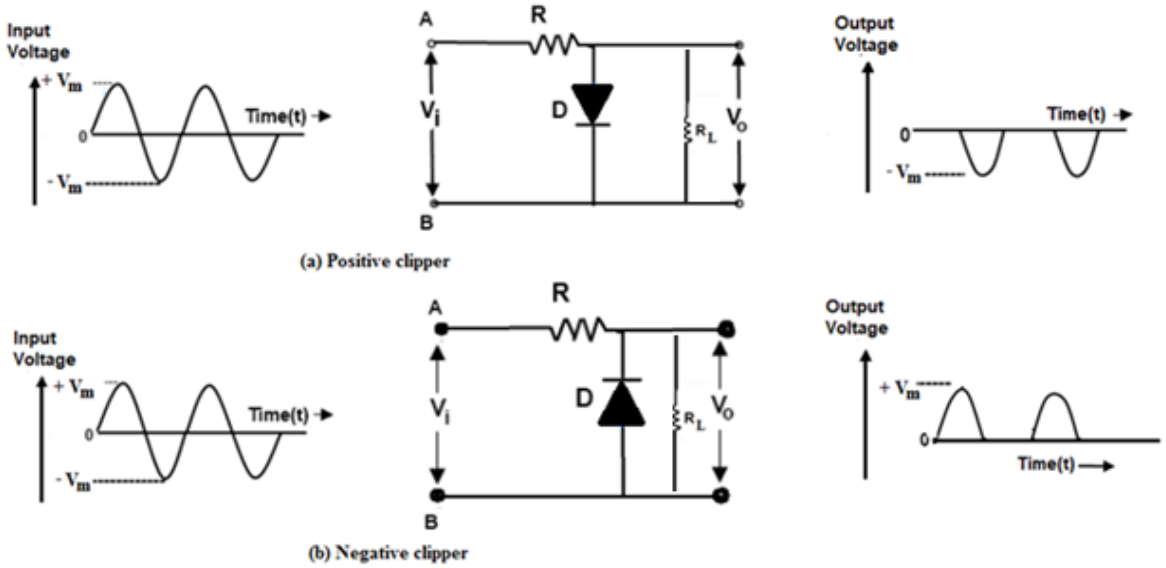


Figure 1.18

1.10.2 Biased clipper: In case we want to remove only a small portion of positive or negative half cycle of the signal voltage, biased clipper is used. For it we use a suitable battery of V volts and

with the polarities of batteries as shown in fig ,portion of positive half cycle will be clipped however the negative half cycle will remain same across the load. Such a clipper is called biased positive clipper (Figure 1.19).

Action of the circuit: The diode will be forward biased so long as input voltage is greater than +V volt. When input voltage is greater than the supply voltage i.e. +V volt,the diode behaves as a short and the output is equal to +V volt .The output will stay at +V volt so long as the input voltage is greater than +V volt. But during the period the input voltage is less than the +V volt , the diode is reverse biased and behaves as open circuit there for most of the input voltage applied across the output. In this way positive clipper removes input voltage above +V volt while during the negative half cycle of the input voltage diode is reverse biased there for almost entire negative half cycle appears across the load.

Similarly if it is desired to clip a portion of negative have cycle of the input voltage, same like we do in the negative clipper circuit ,we will reverse the polarities of the diode and the battery and in this case the circuit will act as a negative clipper in which positive half remains same but a portion of negative half is clipped depending on the value of V.

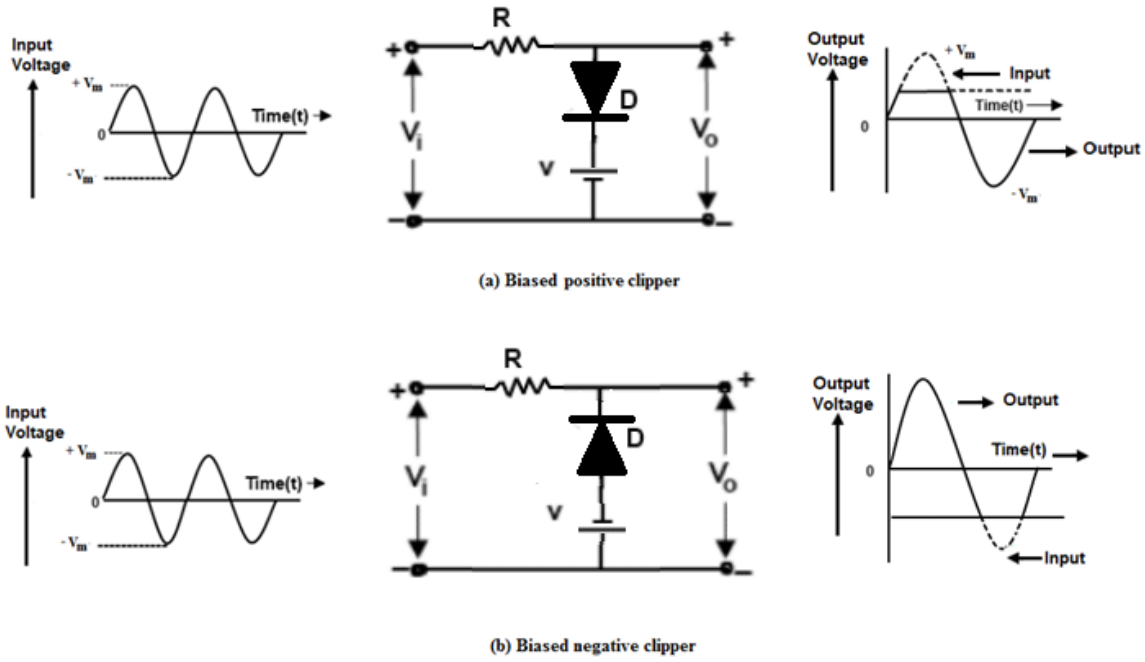


Figure 1.19

1.10.3 Combination clipper: Combination clipper is a combination of biased positive and negative clippers in which a portion of both positive as well as negative half cycle of the input voltage can be removed. Here we use two diodes D_1 and D_2 and two batteries V_1 and V_2 for removing the portion of positive half cycle as well as of negative half cycle.

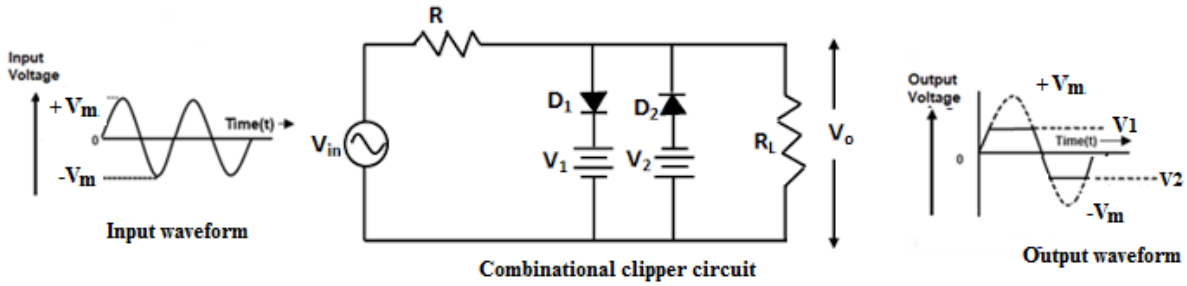


Figure 1.20

When positive half cycle of the input voltage is greater than + V_1, diode D_1 conducts while diode D_2 remains reverse biased therefore a voltage V_1 appears across the load. output will remain at +V_1 volt as long as the input voltage exceeds + V_1 volts .On the other hand during the negative

half cycle of the input diode D_2 will be forward biased and conduct so output will be fixed at $-V_2$ volt .Diode D_1 will be reverse biased as long as the input voltage is greater than $-V_2$ volt. Between $+V_1$ and $-V_2$ neither diode is on therefore in this condition most of the input voltage will be appeared across the load. Obviously the value of $+V_1$ and $-V_2$ will be less than $+V_m$ and $_ V_m$.

1.11 Comparator:

A comparator is a device which is used to sense when an arbitrary varying signal reaches some threshold or reference level. Comparators find application in many electronics systems: for example, they may be used to sense when a linear ramp reaches some defined voltage level, or to indicate whether or not a pulse has an amplitude greater than a particular value. Provided that suitable output limiting is provided, comparator outputs may be used to drive logic circuits.

1.11.1 Circuit diagram and Working The non-linear circuits to perform the operation of clipping may also be used to perform the operation of comparison. The basic difference between the two is that in comparator there is no interest in reproducing any part of the signal waveform. For example, the comparator output may consist of an abrupt departure from source quiescent level which occurs at the time the signal attains the reference level but is otherwise independent of the signal. Or the comparator output may be a sharp pulse which occurs when signal and reference are equal. If we assume that ramp signal is applied to the input, as shown in Figure 1(a) the output Figure 1(b) is constant VR volts until the ramp signal reduces a value equal to VR volts until the ramp signal reduces a value equal to VR volts then the diode conducts and the input signal appears at the output.

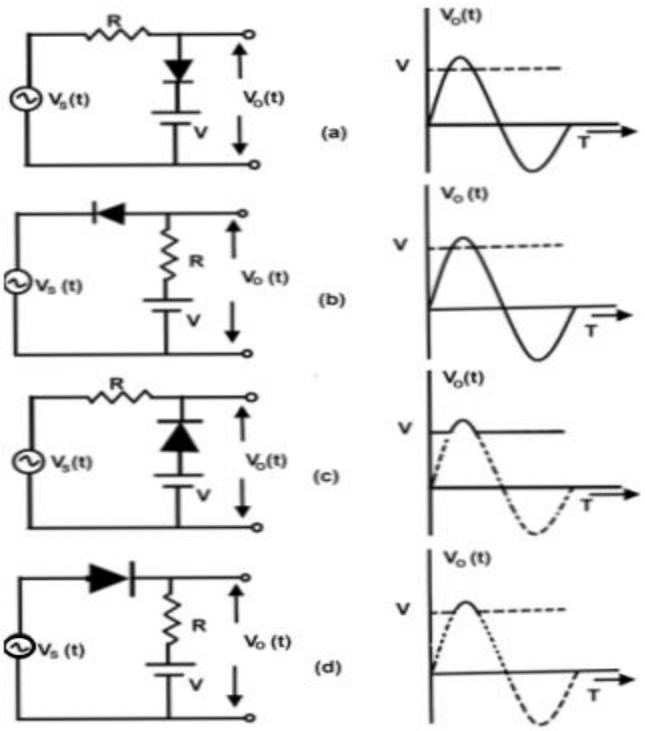


Figure 1.21

In a circuit a clipper was important that the portion of the wave form passed by the diode was not distorted. The exact time t1 at which the diode began conducting was of secondary importance. Now this circuit will be considered as a voltage comparator, (since it compares the varying signal voltage with the reference voltage and hence the name voltage comparator) and of primary concern is the time at which the input signal voltage reaches the reference level VR. The shape of the output waveform is of secondary importance. A diode used for this purpose called pick-off diode. Similarly with an increasing ramp at its input the circuit of Figure 1(c) will be continue to operate as a comparator. Its response will be same as shown in Figure 2(b). The diode of this circuit is then referred to as a breakaway diode. The other two circuits shown in Figure 1 (a) and (b) will act as comparators with a decreasing ramp. Their response is shown in Figure 2 (c) and (d).

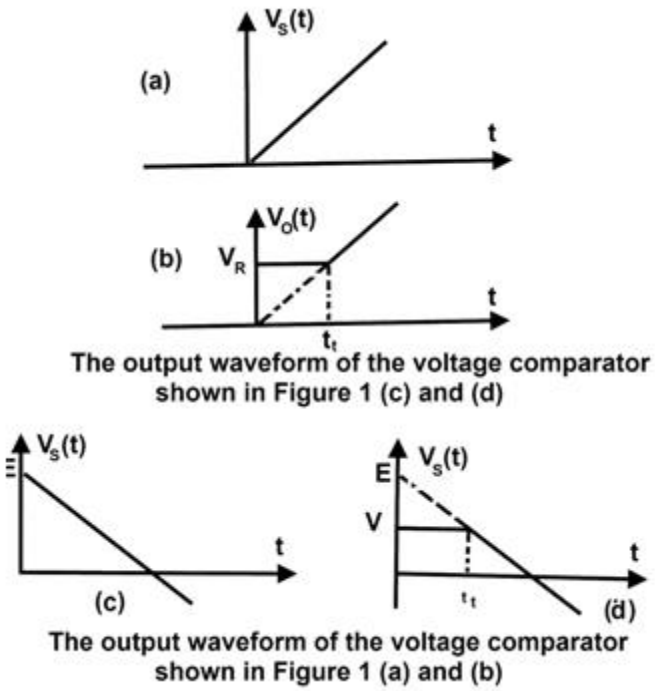


Figure 1.22

1.12 Voltage regulator:

A voltage regulator is a circuit that creates and maintains a fixed output voltage, irrespective of changes to the input voltage or load conditions. It works as a shield for protective devices from damage. It can regulate both AC or DC voltages, depending on its design.

Basically, there are two types of Voltage regulators: Linear voltage regulator and Switching voltage regulator.

- There are two types of linear voltage regulators: Series and Shunt.
- There are three types of switching voltage regulators: Step up, Step down, and Inverter voltage regulators.

Both types regulate a system's voltage, but linear regulators operate with low efficiency and switching regulators operate with high efficiency. In high-efficiency switching regulators, most of the input power is transferred to the output without dissipation.

1.12.1 Zener Diode as Voltage Regulator

A zener diode can be used as a voltage regulator or voltage stabilizer, to provide a constant voltage from a source even though the input voltage V_i and load resistance R_L may vary over a wide range. As shown in Figure 1.23 the zener diode of zener voltage V_Z is connected reversely across the load resistance R_L across which constant output voltage V_O is required.The series resistance R is used to absorb the output voltage fluctuations, so as to maintain constant output voltage across R_L . When the circuit is properly designed, the output voltage E_O remains constant

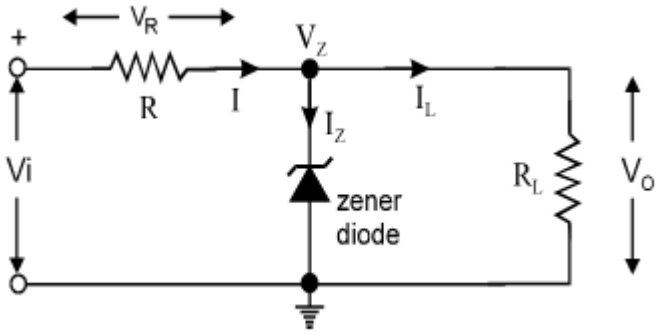


Figure 1.23

Case 1: Input voltage V_i Variable and Load R_L constant

Suppose the input voltage V_i increases, since the zener is in the breakdown region, the zener diode is equivalent to a battery of voltage V_Z and the output voltage remains constant at V_Z ($V_O = V_Z$). The excess voltage is dropped across R. This will cause an increase in the value of total current I. The zener will conduct the increase of current in I, while the load current remains constant.Hence the output voltage remains constant irrespective of the change in input voltage E_i

Case 2: Input voltage V_i Constant and load R_L Vaiable

Now suppose the input voltage V_i is constant but R_L decreases.Since the zener diode is in breakdown region , voltage across it will remain constant at V_Z. As the output voltage V_O is equal to the zener voltage, So V_O will also remain constant at V_Z.When R_L decreases ,in order to

maintain V_O constant, current through the load resistance I_L will increase. Since V_i is constant, total current I is also constant. So the increase in load current I_L will come from a decrease in zener current I_Z

1.13 Frequency dependence of semiconductor device:

As the junction capacitance is a reactive component and varies with frequency. It affects the use of semiconductor devices particularly at high frequency.Junction capacitance, lead inductance ,skin effect and transit time effect are the primary cause which restricts the constructional changes in normal semiconductor devices.

1.14 Application of semiconductor devices:

- They are used in the designing of logic gates and digital circuits.
- These are used in microprocessors.
- They are also used in analog circuits such as rectifiers,voltage multipliers etc.
- Used in high voltage applications.
- Used in different wave shaping circuits such as clipping and clamping circuits.
- Zener diode is used in voltage regulators widely.

1.15 Summary

This chapter discusses the different types of PN junction diodes, their construction , symbol,working and application. Invention of semiconductor devices brings revolutionary changes in electronic industry .

1.16 Glossary:

Semiconductors: Semiconductors are materials that are neither good conductors nor good insulators means conductivity of such substances lies in between conductor and insulator. Infect at absolute zero temperature they are perfectly insulators. Conductivity of intrinsic semiconductor is too less to be of any practical use however incorporating trivalent or pentavalent impurity and

converting intrinsic semiconductor into p type or n type semiconductor makes a revolution in electronic industry.

Homo and hetrojunction devices

A homojunction is a junction between the same materials with the same crystalline structure (e.g. silicon with silicon or germanium with germanium) while a hetrojunction is a junction between different materials or between the same materials, but with different crystal structure. (e.g silicon with germanium or nickel with gallium arsenide.

Forward and reverse bias In forward bias positive terminal of the battery is connected to P type and negative terminal is connected to N type while in reverse bias positive terminal of the battery is connected to N type and negative terminal is connected to P type.Diode conducts only when it is forward bias.

Tunneling effect crossing of a higher potential barrier by subatomic particle is called tunnel effect. It is a quantum mechanical effect.

Solar cell A **solar cell** is an electrical device that converts light energy into electrical energy through the photovoltaic effect.

Clipping circuits Clipping circuits are kind of waveform circuits which change the input waveform by removing or flipping a portion of the applied input wave.

Comparator A comparator is a device which is used to sense when an arbitrary varying signal reaches some threshold or reference level.

A comparator is a device which is used to sense when an arbitrary varying signal reaches some threshold or reference level.

Voltage regulator A voltage regulator is a circuit that creates and maintains a fixed output voltage, irrespective of changes to the input voltage or load conditions.

1.17 Reference books:

1. Principles of electronics by V.K.Mehta

2. Basic Electronics by B.L.Thereja

3. Basic Electronics by D.C.Tayal

1.18 Suggested readings:

1. Electronic devices and circuits by Jacob Milliman and C.C.Halkais

2. The Feynman Lectures on Physics by Richard Feynman

3. Electronic devices and circuit theory by R.L.Boylestad and Louis N

1.19 Terminal Questions:

1.19.1 Short answer type questions

1. Differentiate between zener breakdown and avalanche breakdown?

2. What is tunneling? Write application of tunnel diode.

3. What is light emitting diode? Why it is called so?

4. Why silicon is preferred over germanium for fabrication of semiconductor devices?

5. Discuss the effect of temperature on reverse saturation current of P-N junction diode.

1.19.2 Long answer type questions

1. Discuss the construction, working and V-I characteristics of P-N junction diode? How does an actual diode differ from an ideal diode?

2. Discuss construction, working and V-I characteristics of Zener diode?

3. Define voltage regulation. How zener diode used as a voltage regulator in power supply system.

4. Describe the construction and working of a tunnel diode. Draw and explain its V-I characteristics.

5. Write short notes on,

a) Solar cell
b) IMPATT diode
c) Photo diode
d) Clipping circuits

.

1.19.3 Numerical questions

1. Under large reverse bias voltage, the current flowing through a P-N junction diode at room temperature is 20μA**.**Calculate the forward current for the voltage of 0.1 volt. **(Ans. 915.4 μA)**

2. A varactor diode has a capacitance of 20 PF when when a reverse voltage of 9 volt is applied across it. Find the diode capacitance when reverse bias voltage is decreased to 4 volt.

(Ans. 30 PF)

3. Calculate the maximum current handled by zener diode having a breakdown voltage of 6 volt with a maximum power dissipation of 364 milliwaatts.? **(Ans. 60 mA)**

4. In a negative shunt clipper shown in figure below has a peak input voltage of 6 volt, resistance R=1 Kω and load resistance R_L=2 Kω. What is the peak output voltage from this circuit?

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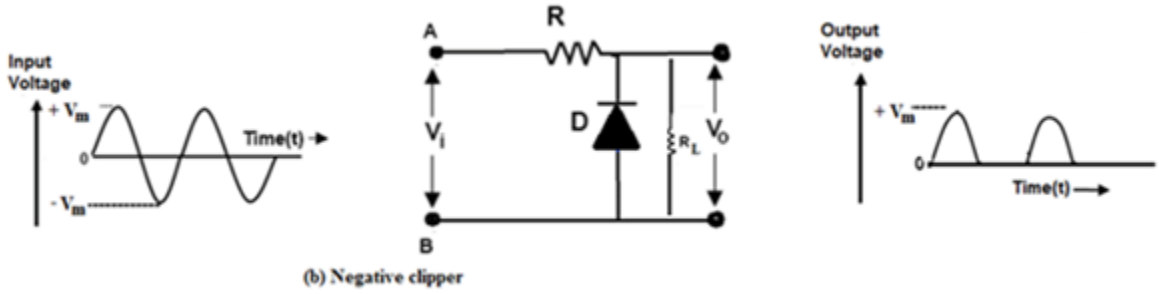


(b) Negative clipper

(Ans. 4 volt)

5. Calculate the value of series resistance required to limit the current through a LED to 10 mA with a forward voltage drop of 1.6V. LED is connected to a 5V supply.

(Ans. 340 Ω)

UNIT 2 TRANSISTOR AND AMPLIFIER

Structure

2.1 INTRODUCTION

Semiconductors are materials that are neither good conductors nor good insulators means conductivity of such substances lies in between conductor and insulator. Infect at absolute zero temperature they are perfectly insulators.

Using semiconductor materials different electronic components are made that uses the electronic properties of semiconductor materials, like silicon, germanium, and gallium arsenide.

Semiconductor devices have almost replaced vacuum tubes in different electronic applications. They are manufactured for both discrete devices and integrated circuits. Because of their reliability, compactness, low cost and wide range of current and voltage handling components semiconductor devices becomes the key element in most of the daily use electronic instruments, industrial control instruments, computing and data processing equipment as well communication devices too.

A transistor is a semiconductor device used to amplify or switch electronic signals and electrical power. Transistors are one of the basic building blocks of modern electronics.

2.2 OBJECTIVES

After study of unit the student will be able

i. To study the classification of transistor devices.
ii. To understand the construction, working, advantages and disadvantages of different transistor.
iii. To describe construction and working of amplifier.

2.3 TRANSISTOR

A Bipolar Junction Transistor is a semiconductor device consisting of two P-N Junctions connecting three terminals called the Base, Emitter and Collector terminals. The arrangement of the three terminals affects the current and the amplification of the transistor. The behavior of Bipolar junction transistors is also very different for each circuit configuration. The three different circuit configurations produce different circuit characteristics with regards to input impedance, output impedance and gain. These characteristics affect whether the transistor exhibits voltage gain, current gain or power gain. One of the primary operations of a bipolar junction transistor is to amplify the signal of the current. Bipolar junction Transistors are able to regulate the current so that the current magnitude is proportional to the biased voltage applied at the base terminal of the transistor. The application of Bipolar Junction Transistors can be found in devices that utilize analog circuits such as computers, mobile phones and radio transmitters.

As shown in figure 1, in PNP transistor the emitter is P-type, the base is N-type and the collector is P-type. In NPN transistor the emitter is N-type, the base is P-type and the collector is N-type. The Figure also shows the circuit symbols for transistors. The arrows show the direction of conventional current (+ ve charge or hole movement) between the emitter E and base B.

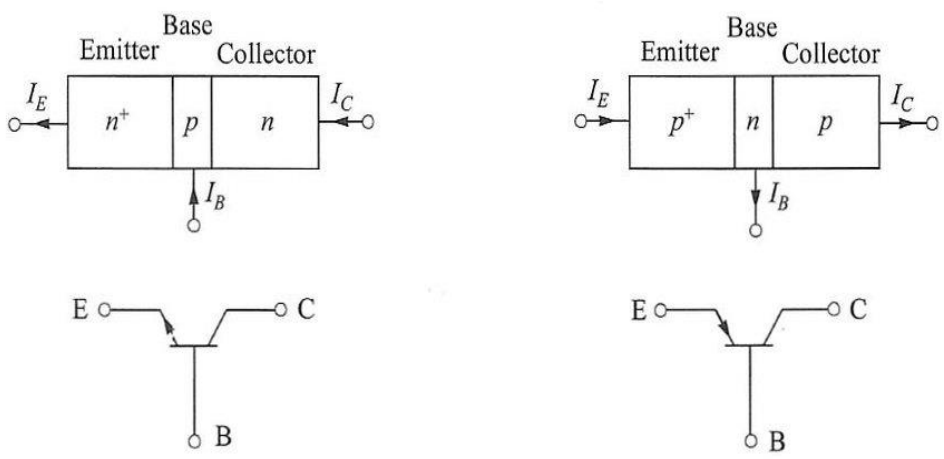


Figure: 1

Bipolar Junction Transistors have three semiconductor regions. The three regions are the emitter region (E), base region (B), and the collector region (c) and these regions are differently doped depending on the type of bipolar transistor it is. The two types of bipolar transistors are the PNP Transistor, whose three regions are p type, n type, and p type respectfully, and NPN Transistor, whose regions are n type, p type, and n type respectfully. Both types of transistors have one P-N junction between the collector region and base region and another P-N junction between the base region and emitter region. The base region is always the structure's center connection with the emitter and collector regions connected on either side. Both types of transistors also have the same principle of operation, with the single difference being in the polarity of power and biasing for each type.

Bipolar Junction Transistors ability to amplify a signal, through the regulation of current, allows for the transfer of an input signal from one circuit to another, regardless of the different level of resistance in each circuit. The amount of current flowing through the transistor is proportional to the magnitude of the biasing voltage applied to the base terminal. This allows the transistor to act like a current-controlled switch. Depending on whether the bipolar transistor is PNP or NPN, the controlled current will flow from the collector to the emitter or from the emitter to the collector while the smaller controlling current will flow from base to emitter or from emitter to base respectively.

The transistor contains a maximum allowed current that is able to restrict the amount of current as it passes from terminal to terminal. Depending on the order of the terminals in the transistor, the transistor will act as either a conductor or an insulator when in the presence of a controlled current. This ability to change between these two states, insulator or conductor, enables the transistor to act like a switch or as an amplifier of small amplitude signals applied to the base depending on the structure and order of the three semiconductor regions.

Structure

Bipolar Junction Transistors contain three doped extrinsic semiconductor regions each connected to a circuit. The transistor is not symmetrical due to the different doping ratios of the emitter, collector and base regions. The base region consists of a lightly doped materials that exhibits high resistivity. The base is located between the heavily doped emitter region and the lightly doped collector region. The collector engulfs the emitter region which eliminates the ability for electrons injected into the base region to escape the base region without being collected. The emitter region is heavily doped to increase the current gain of the transistor.

For high current gain, a high ratio of carriers injected by the emitter to those injected by the base is needed. Increasing the emitter injection efficiency results in the majority of the carriers injected into the emitter-base junction coming from the emitter region. The high doping ratio of the emitter and collector regions, also means the collector-base junction is reverse biased. The collector-base junction can therefore have a high magnitude reverse bias voltage applied before the junction breaks down. For the transistor as a whole, the fundamental difference between the NPN Transistor and the PNP Transistor is current directions and voltage polarities of the transistor junctions. Making sure these two are always opposite each other ensures the transistors are properly biased.

NPN Bipolar Transistor

A NPN Bipolar Junction Transistor has a P-doped semiconductor base in between an N-doped emitter and N-doped collector region. NPN bipolar transistors are the highest used bipolar transistors due to the ease of electron mobility over electron hole mobility.

For this type of transistor, large magnitude collector and emitter currents get produced through the amplification of a small current which enters through the base. This small current only gets amplified when the transistor becomes active. In this active state, a positive potential difference is found between both the base region to the collector region and the emitter region to the base region which results in current that gets carried by electrons, between the collector and emitter regions. The construction and terminal voltages for a NPN Transistor are shown in Figure 3 below.

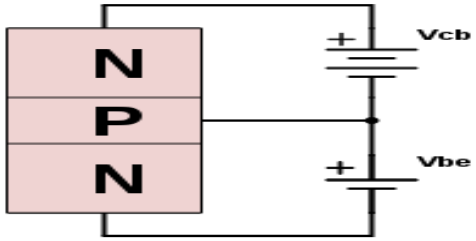


Figure 3: Transistor schematic

For a bipolar NPN transistor to conduct the Collector is always more positive with respect to both the Base and the Emitter. The voltage between the Base and Emitter (V_{BE}), is positive at the Base and negative at the Emitter. The Base terminal is always positive with respect to the Emitter. Another way to display a NPN Transistor is shown in Figure 4 below.

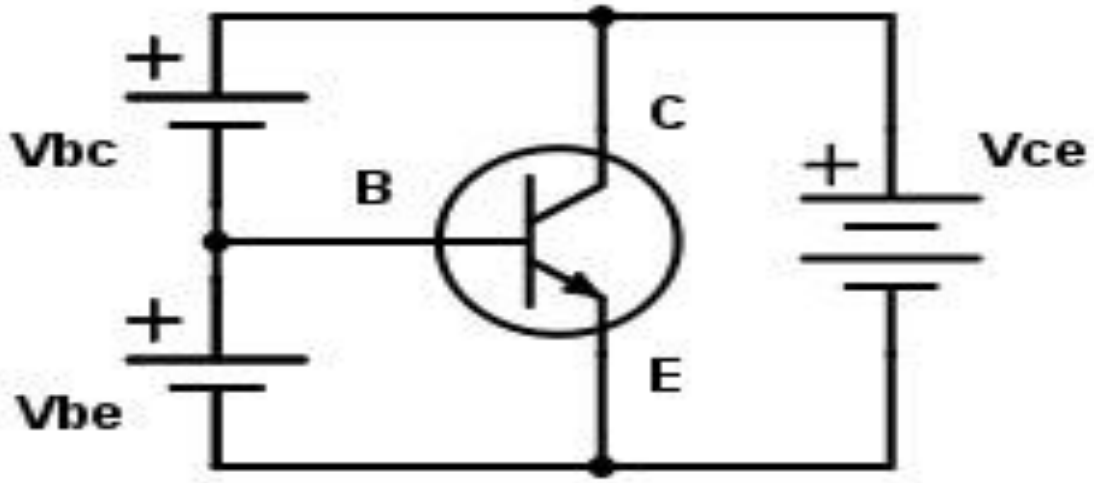


Figure 4 NPN Bipolar Transistor circuit

The current flowing out of the transistor must be equal to the currents flowing into the transistor as the emitter current is given as

$$Ie = Ic + Ib$$

Note: “Ic” is the current flowing into the collector terminal, “Ib” is the current flowing into the base terminal and “Ie” is the current flowing out of the emitter terminal.

Since the physical construction of the transistor determines the electrical relationship between these three currents, (Ib), (Ic) and (Ie), any small change in the base current

(Ib), will result in a much larger change in the collector current (Ic). The ratio of the collector current to the emitter current is called α.

$$\alpha = Ic/Ie$$

The current gain of the transistor from the Collector terminal to the Emitter terminal, Ic/Ie, is a function of the electrons diffusing across the junction. The current gain of the transistor from the Collector terminal to the Base terminal is signified by β.

$$\beta = Ic/Ib$$

NPN transistors are good amplifying devices when the Beta value is large. Beta values normally range between 20 and 200 for most general purpose transistors. Therefore if a transistor has a Beta value of 50, then for every 50 electrons flowing between the emitter-collector terminals one electron will flow from the base terminal.

By combining the expressions for both α, and β the current gain of the transistor can be given as:

$$\beta = \alpha /(1- \alpha)$$

As seen from the equations above, electron mobility between the Collector and Emitter circuits is the only link between these two circuits. This link is the main feature of transistor action. Since transistor action is constituted by initial electron movement through the base region, the amplifying properties of the transistor comes from the consequent control the Base exerts on the current between the Collector and Emitter. As long as the flow of the biasing current into the base terminal is steady, the base region can be treated as a current control input.

2.3.1. Transistor Characteristics

The graph representing the relationships between the current and the voltage of any transistor of any configuration is called Transistor Characteristics. Any two-port network which is analogous to transistor configuration circuits can be analyzed using three types of characteristic curves. They are

- **Input Characteristics:** The curve describes the changes in the values of input current with respect to the values of input voltage keeping the output voltage constant.
- **Output Characteristics:** The curve obtained by plotting the output current against output voltage keeping the input current constant.

- **Current Transfer Characteristics:** This characteristic curve describes the variation of output current in accordance with the input current, keeping the output voltage constant.

There are three configurations of transistor circuits: (1) Common- base configuration (ii) Common- emitter configuration (iii) Common- collector configuration. The word common is associated with the electrode that is common to both the input and the output circuits. This common electrode is usually grounded. Hence the three method of connection are also called the grounded-base, grounded-emitter and grounded-collector configuration.

Common Emitter (CE) Configuration of Transistor

In CE Configuration, the Emitter terminal of the transistor will be connected common between the output and the input terminals as shown in Figure 5.

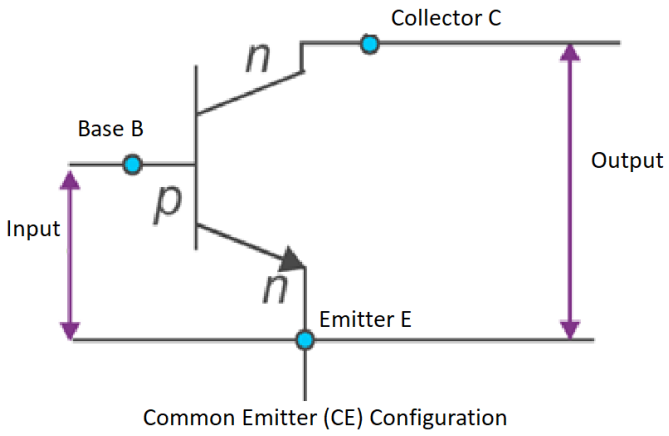


Figure: 5

The transistor characteristic under Common Emitter configuration is as follows:

Input Characteristics - The base current I_B is measured as the base voltage V_{BE} is varied for a constant value of collector voltage V_{CE}. Then, I_B is plotted as a function of base voltage V_{BE}. This gives an Input Characteristics curve as shown in Figure 6. Two curves are drawn in Fig. for V_{CE1}=0 and V_{CE2}=10 volt. It is seen that the base current increases non-linearly with increase in base voltage. Also, the input characteristics are slightly dependent upon the collector-voltage V_{CE}. The input resistance is defined as

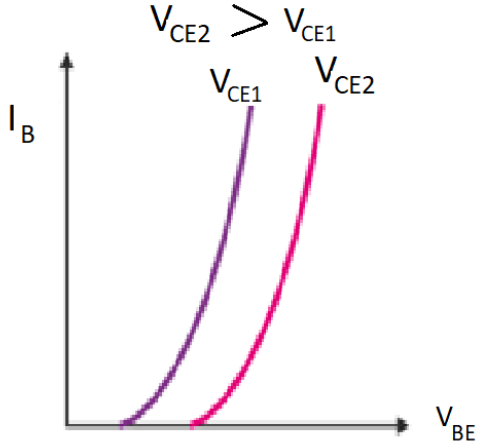


Figure 6

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_B} \quad \textbf{at constant } V_{CE}$$

Output Characteristics - To obtain the output characteristics, the collector current I_C is measured as the collector voltage V_{CE} is varied for a constant value of the base current I_B. In this manner, a family of curves is obtained as shown in Figure 7.

It is seen from the curve that for a very small V_{CE}, the collector current I_C varies rapidly with V_{CE}. But for the values of V_{CE} about 0.5 volt, it is decided almost entirely by I_B, and is almost independent of V_{CE}. There is a small collector current even when the base current I_B is zero. This is due to the intrinsic conduction inherent in semiconductors and is highly temperature-dependent. The output resistance is defined as

$$R_{out} = \frac{\Delta V_{CE}}{\Delta I_C} \quad \textbf{at constant } I_B$$

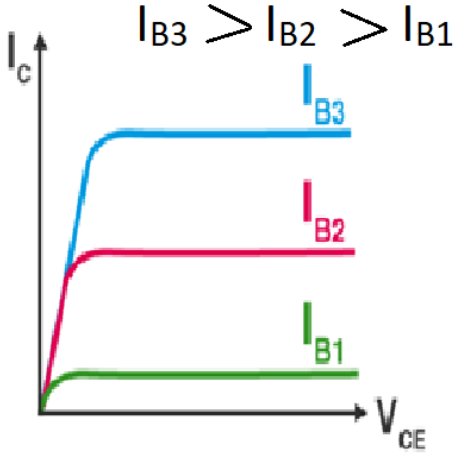
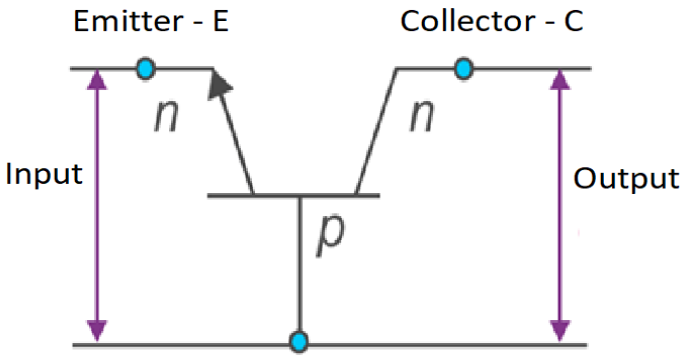


Figure 7

Common Base (CB) Configuration of Transistor

In CB Configuration, the base terminal of the transistor will be connected common between the output and the input terminals as shown in Figure 8.



Common base (CB) Configuration **Figure 8**

The curve showing the variation of the emitter current I_E with emitter voltage V_{BE} keeping collector Base voltage (V_{CB}) constant are the 'input' characteristics; while those showing the variation of the collector current I_C with collector voltage V_{CB} keeping the emitter current (I_E) constant are the 'output' characteristics.

Input Characteristics - To draw the inputcharacteristics, the collector voltage V_{CB} is first made to zero. The emitter voltage V_{BE} now increased from zero onwards and the emitter current I_E is noted. A graph between V_{BE} andI_E is plotted as shown in Figure 9 (V_{CB1} = 0 V and V_{CB2} = 40V)

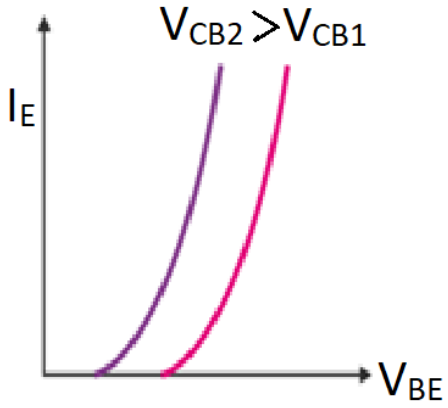


Figure **9**

It is seen from these curves that the emitter currentI_E increased rapidly with small increments in the emitter voltage V_{BE} and reaches several milliamp for about ;V_{BE}100= V. The input resistance is given by

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_E}$$ **at constant** $V_{BE,}$

For a small signal-voltage applied on the emitter, input resistance is very low. The curves also suggest that the emitter current is almost independent of the collector to base voltage V_{CB}.

Output Characteristics - **T**o obtain the output characteristics, the collector current I_C is measured as the collector voltage V_{CB} is varied for a constant value of the emitter current I_E. In this manner, a family of curves can be obtained as shown in Figure 10.

It is seen from these curves that the entire variation in the collector current takes place at very low values of collector voltage. When the collector voltage is about 1 volt, it collects all the charge carriers that diffuse into the base- collector junction. Hence, further increase in collector voltage does not produce appreciable increase in collector current. In other words the collector current becomes practically independent of collector voltage. This current is always a little less than the corresponding emitter currents due to the small percentage of charge carriers lost in the thin base due to recombinations of hole with electrons. The output resistance is given by

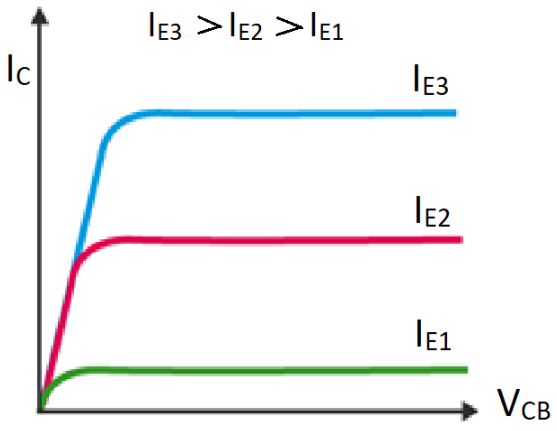


Figure 10

$$R_{out} = \frac{\Delta V_{CB}}{\Delta I_B}$$ **at constant** I_E

Common Collector (CC) Configuration of Transistor

In CC Configuration, the Collector terminal of the transistor will be connected common between the output and the input terminals as shown in Figure 11. Sometimes common collector configuration is also referred to as emitter follower, voltage follower, common collector amplifier, CC amplifier, or CC configuration. This configuration is mostly used as a voltage buffer.

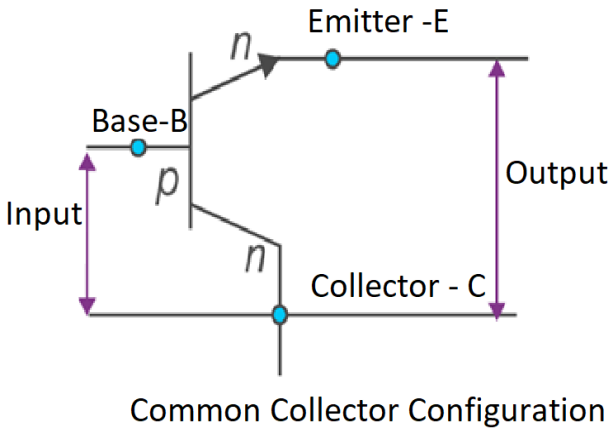


Figure 11

Input Characteristics - To determine the input characteristics, the output voltage V_{EC} is kept constant and the input voltage V_{BC} is increased from zero volts to different voltage levels. For each level of input voltage V_{BC}, the corresponding input current I_B is noted. A curve is then drawn between input current I_B and input voltage V_{BC}. Now the output voltage V_{CE} is again fixed to different voltage levels and the same process is repeated to obtain different curves between input current I_B and input voltage V_{BC} at constant output voltage V_{EC}. A graph between V_{BC} and I_B is plotted as shown in Figure 12.

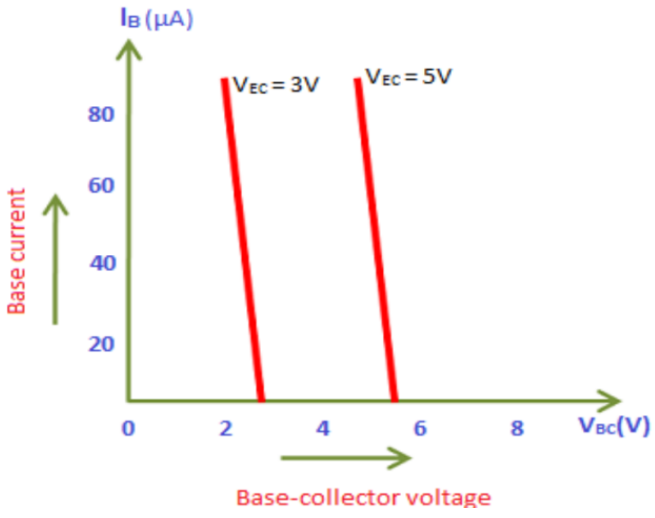


Figure 12

Output Characteristics - To determine the output characteristics, the input current I_B is kept constant at zero μA and the output voltage V_{EC} is increased from zero volts to different voltage levels. For each level of output voltage V_{EC}, the corresponding output current I_E is noted. A curve is then drawn between output current I_E and output voltage V_{EC} at constant input current I_B (0 μA).

Next, the input current (I_B) is kept constant at 20 μA and a curve is then drawn between output current I_E and output voltage V_{EC}. This process is repeated for higher fixed values of input current I_B (i.e. 40 μA, 60 μA, 80 μA and so on) as shown in Figure 13

In common collector configuration, if the input current or base current is zero then the output current or emitter current is also zero. As a result, no current flows through the transistor. So the transistor will be in the cutoff region. If the base current is slightly increased then the output current or emitter current also increases. So the transistor falls into the active region. If the base current is heavily increased then the current flowing through the transistor also heavily increases. As a result, the transistor falls into the saturation region. The curves and the three regions are shown in the figure 13.

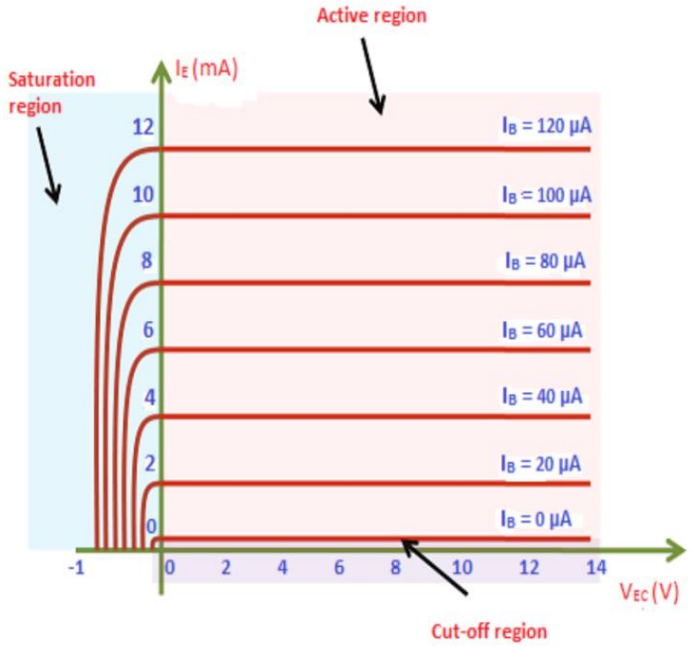


Figure 13

2.4. TRANSISTOR AS AN AMPLIFIER:

Amplifier is the generic term used to describe a circuit which produces and increased version of its input signal. Transistors are mainly used for amplification of signals. The signal may have proper frequency and waveform but if its amplitude is small it cannot be used to operate certain circuits or devices which require definite levels of amplitude of the input signal for proper operation. Thus the amplification of the input signals becomes important. An amplifier is a device that produces an enlarged version of an input signal. Almost no electronic signal can work without amplifier.

The transistor amplifier circuit is shown in the Figure 14. The emitter and base of the transistor are connected in forward biased and the collector base region is in reverse bias. The input signal or weak signal is applied across the emitter base and the output is obtained to the load resistor R_C which is connected in the collector circuit. The DC voltage V_{EE} is applied to the input

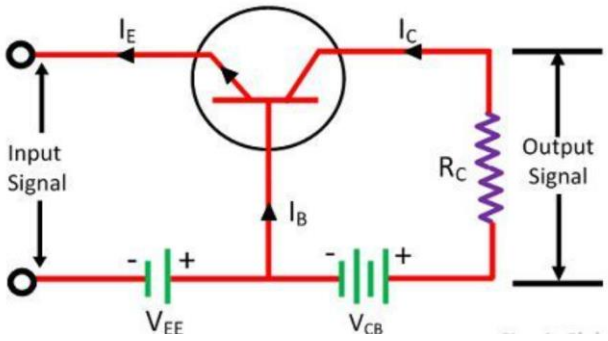


Figure 14

circuit along with the input signal to achieve the amplification. The DC voltage V_{EE} keeps the emitter-base junction under the forward biased condition regardless of the polarity of the input signal and is known as a bias voltage.

When a weak signal is applied to the input, a small change in signal voltage causes a change in emitter current (or we can say a change of 0.1V in signal voltage causes a change of 1mA in the emitter current) because the input circuit has very low resistance. This change is almost the same in collector current because of the transmitter action.

In the collector circuit, a load resistor R_C of high value is connected. When collector current flows through such a high resistance, it produces a large voltage drop across it. Thus, a weak signal (0.1V) applied to the input circuit appears in the amplified form (10V) in the collector circuit.

There are many forms of electronic circuits classed as amplifiers, from Operational Amplifiers and Small Signal Amplifiers up to Large Signal and Power Amplifiers. The classification of an amplifier depends upon the size of the signal, large or small, its physical configuration and how it processes the input signal, which is the relationship between input signal and current flowing in the load.

2.5. Performance of Amplifier

As the common emitter mode of connection is mostly adopted, let us first understand a few important terms with reference to this mode of connection.

2.5.1. Input Resistance

As the input circuit is forward biased, the input resistance will be low. The input resistance is the opposition offered by the base-emitter junction to the signal flow. By definition, it is the ratio of small change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage.

Input resistance, $R_i = \Delta V_{BE} / \Delta I_B$

Where R_i = input resistance, V_{BE} = base-emitter voltage, and I_B = base current.

2.5.2. Output Resistance

The output resistance of a transistor amplifier is very high. The collector current changes very slightly with the change in collector-emitter voltage. By definition, it is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the resulting change in collector current (ΔI_C) at constant base current.

Output resistance, $R_o = \Delta V_{CE} / \Delta I_C$

Where R_o = Output resistance, V_{CE} = Collector-emitter voltage, and I_C = Collector-emitter voltage.

2.5.3. Effective Collector Load

The load is connected at the collector of a transistor and for a single-stage amplifier, the output voltage is taken from the collector of the transistor and for a multi-stage amplifier, the same is collected from a cascaded stages of transistor circuit. By definition, it is the total load as seen by the a.c. collector current. In case of single stage amplifiers, the effective collector load is a parallel combination of R_C and R_o.

Effective Collector Load, $R_{AC} = R_C // Ro$

In a multi-stage amplifier (i.e. having more than one amplification stage), the input resistance R_i of the next stage also comes into picture.

2.5.4. Current Gain

The gain in terms of current when the changes in input and output currents are observed, is called as Current gain. By definition, it is the ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B).

Current gain, $\beta = \Delta I_C / \Delta I_B$

The value of β ranges from 20 to 500. The current gain indicates that input current becomes β times in the collector current.

2.5.5. Voltage Gain

The gain in terms of voltage when the changes in input and output currents are observed, is called as Voltage gain. By definition, it is the ratio of change in output voltage (ΔV_{CE}) to the change in input voltage (ΔV_{BE}).

Voltage gain, $A_V=\Delta V_{CE}/\Delta V_{BE}$

2.5.6. Power Gain

The gain in terms of power when the changes in input and output currents are observed, is called as Power gain. By definition, it is the ratio of output signal power to the input signal power.

Power gain, $A_P=(\Delta I_C)^2\times R_{AC}(\Delta I_B)^2\times Ri$

= Current gain × Voltage gain

2.6. Classification

The type or classification of an Amplifier is given in the following table.

Classification of Signal Amplifier

Type of Signal	**Configuration**	**Classification**	**Operation Frequency**
Small Signal	Common Emitter	Class A Amplifier	Direct Current (DC)
Large Signal	Common Base	Class B Amplifier	Audio Frequencies (AF)
	Common Collector	Class AB Amplifier	Radio Frequencies (RF)
		Class C Amplifier	VHF*, UHF* and SHF*Frequencies

*Very high frequency, Ultra high frequency, Super high frequency

Amplifiers can be thought of as a simple box or block containing the amplifying device, such as a Bipolar Transistor, Field Effect Transistor or Operational Amplifier, which has two input

terminals and two output terminals (ground being common) with the output signal being much greater than that of the input signal as it has been "Amplified".

An ideal signal amplifier will have three main properties: Input Resistance or (R_{IN}), Output Resistance or (R_{OUT}) and amplification known commonly as Gain or (A). No matter how complicated an amplifier circuit is, a general amplifier model can still be used to show the relationship of these three properties.

Ideal Amplifier Model – It is the model shown in Figure 15

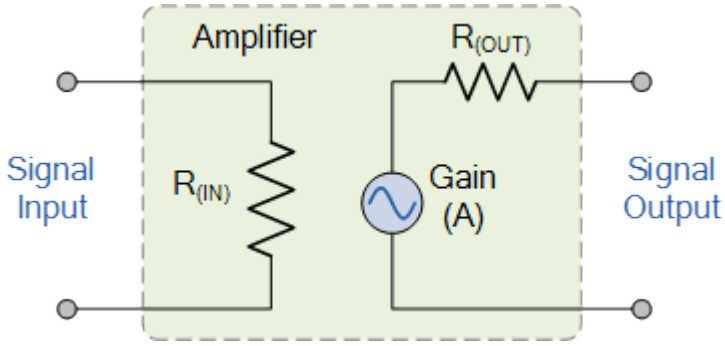


Figure 15

The amplified difference between the input and output signals is known as the Gain of the amplifier. Gain is basically a measure of how much an amplifier "amplifies" the input signal. For example, if we have an input signal of 1 volt and an output of 50 volts, then the gain of the amplifier would be "50". In other words, the input signal has been increased by a factor of 50. This increase is called Gain.

Amplifier gain is simply the ratio of the output divided-by the input. Gain has no units as its a ratio, but in Electronics it is commonly given the symbol "A", for Amplification. Then the gain of an amplifier is simply calculated as the "output signal divided by the input signal". There are three different kinds of amplifier gain which can be measured and these are: *Voltage Gain* (Av), *Current Gain* (Ai) and *Power Gain* (Ap) depending upon the quantity being measured with examples of these different types of gains are given below.

The power gain (Ap) or power level of the amplifier can also be expressed in **Decibels**, (**dB**). The Bel (B) is a logarithmic unit (base 10) of measurement that has no units. Since the Bel is too large a unit of measure, it is prefixed with *deci* making it **Decibels** instead with one decibel being one tenth (1/10th) of a Bel. To calculate the gain of the amplifier in Decibels or dB, we can use the following expressions.

- Voltage Gain in dB: $a_v = 20*\log(Av)$
- Current Gain in dB: $a_i = 20*\log(Ai)$
- Power Gain in dB: $a_p = 10*\log(Ap)$

Note that the DC power gain of an amplifier is equal to ten times the common log of the output to input ratio, where as voltage and current gains are 20 times the common log of the ratio. Note however, that 20dB is not twice as much power as 10dB because of the log scale.

Also, a positive value of dB represents a **Gain** and a negative value of dB represents a **Loss** within the amplifier. For example, an amplifier gain of +3dB indicates that the amplifiers output signal has "doubled", (x2) while an amplifier gain of -3dB indicates that the signal has "halved", (x0.5) or in other words a loss.

The -3dB point of an amplifier is called the **half-power point** .

Example 1

Determine the Voltage, Current and Power Gain of an amplifier that has an input signal of 1mA at 10mV and a corresponding output signal of 10mA at 1V. Also, express all three gains in decibels, (dB).

The Various Amplifier Gains:

$$A_v = \frac{\text{Output Voltage}}{\text{Input Voltage}} = \frac{1}{0.01} = 100$$

$$A_i = \frac{\text{Output Current}}{\text{Input Current}} = \frac{10}{1} = 10$$

$$A_p = A_v \times A_i = 100 \times 10 = 1{,}000$$

Amplifier Gains given in Decibels (dB):

$$a_v = 20 \log A_v = 20 \log 100 = 40 \text{ dB}$$

$$a_i = 20 \log A_i = 20 \log 10 = 20 \text{ dB}$$

$$a_p = 10 \log A_p = 10 \log 1000 = 30 \text{ dB}$$

Then the amplifier has a Voltage Gain, (Av) of 100, a Current Gain, (Ai) of 10 and a Power Gain, (Ap) of 1,000

Generally, amplifiers can be sub-divided into two distinct types depending upon their power or voltage gain. One type is called the **Small Signal Amplifier** which include pre-amplifiers,

instrumentation amplifiers etc. Small signal amplifies are designed to amplify very small signal voltage levels of only a few micro-volts (μV) from sensors or audio signals.

The other type are called **Large Signal Amplifiers** such as audio power amplifiers or power switching amplifiers. Large signal amplifiers are designed to amplify large input voltage signals or switch heavy load currents as you would find driving loudspeakers.

Power Amplifiers

The **Small Signal Amplifier** is generally referred to as a "Voltage" amplifier because they usually convert a small input voltage into a much larger output voltage. Sometimes an amplifier circuit is required to drive a motor or feed a loudspeaker and for these types of applications where high switching currents are needed **Power Amplifiers** are required.

As their name suggests, the main job of a "Power Amplifier" (also known as a large signal amplifier), is to deliver power to the load, and as we know from above, is the product of the voltage and current applied to the load with the output signal power being greater than the input signal power. In other words, a power amplifier amplifies the power of the input signal which is why these types of amplifier circuits are used in audio amplifier output stages to drive loudspeakers.

The power amplifier works on the basic principle of converting the DC power drawn from the power supply into an AC voltage signal delivered to the load. Although the amplification is high the efficiency of the conversion from the DC power supply input to the AC voltage signal output is usually poor.

The perfect or ideal amplifier would give us an efficiency rating of 100% or at least the power "IN" would be equal to the power "OUT". However, in reality this can never happen as some of the power is lost in the form of heat and also, the amplifier itself consumes power during the amplification process. Then the efficiency of an amplifier is given as:

Amplifier Efficiency

$$Efficiency\ (\eta) = \frac{Power\ delivered\ to\ the\ Load}{Power\ taken\ from\ the\ Supply} = \frac{P_{OUT}}{P_{IN}}$$

Ideal Amplifier

We can know specify the characteristics for an ideal amplifier from our discussion above with regards to its **Gain**, meaning voltage gain:

- The amplifiers gain, (A) should remain constant for varying values of input signal.
- Gain is not be affected by frequency. Signals of all frequencies must be amplified by exactly the same amount.

- The amplifiers gain must not add noise to the output signal. It should remove any noise that is already exists in the input signal.
- The amplifiers gain should not be affected by changes in temperature giving good temperature stability.
- The gain of the amplifier must remain stable over long periods of time.

Electronic Amplifier Classes

The classification of an amplifier as either a voltage or a power amplifier is made by comparing the characteristics of the input and output signals by measuring the amount of time in relation to the input signal that the current flows in the output circuit.

The transistor to operate within its "Active Region" some form of "Base Biasing" is required. This small Base Bias voltage added to the input signal allowed the transistor to reproduce the full input waveform at its output with no loss of signal. However, by altering the position of this Base bias voltage, it is possible to operate an amplifier in an amplification mode other than that for full waveform reproduction. With the introduction to the amplifier of a Base bias voltage, different operating ranges and modes of operation can be obtained which are categorized according to their classification. These various mode of operation are better known as **Amplifier Class**.

Audio power amplifiers are classified in an alphabetical order according to their circuit configurations and mode of operation. Amplifiers are designated by different classes of operation such as class "A", class "B", class "C", class "AB", etc. These different amplifier classes range from a near linear output but with low efficiency to a non-linear output but with a high efficiency.

No one class of operation is "better" or "worse" than any other class with the type of operation being determined by the use of the amplifying circuit. There are typical maximum conversion efficiencies for the various types or class of amplifier, with the most commonly used being:

- Class A Amplifier – has low efficiency of less than 40% but good signal reproduction and linearity.
- Class B Amplifier – is twice as efficient as class A amplifiers with a maximum theoretical efficiency of about 70% because the amplifying device only conducts (and uses power) for half of the input signal.
- Class AB Amplifier – has an efficiency rating between that of Class A and Class B but poorer signal reproduction than Class A amplifiers.
- Class C Amplifier – is the most efficient amplifier class but distortion is very high as only a small portion of the input signal is amplified therefore the output signal bears very little resemblance to the input signal. Class C amplifiers have the worst signal reproduction.

Need for CE Configuration

We usually employ CE configuration for transistors as amplifiers because it provides large values of current gain, voltage gain and power gain. Moreover, there is a phase-shift of 180

degrees between input and output. It implies the output signal will be an inverted amplified version of the signal given in the input.

A transistor amplifier in order to function properly must have the following things;

- High input impedance.
- High gain.
- High slew rate.
- High bandwidth.
- High efficiency.
- High stability.
- High linearity.

Numericals

Q1. Consider a CE- transistor made to work as an amplifier. The audio signal voltage across the collector resistance of 2 KΩ is 2 volts. Suppose the current amplification factor of the transistor is 100 and base resistance is 1 KΩ, determine the input signal voltage and base current?

Sol**:** Given $R_C = 2\ K\Omega = 2000\ \Omega$; $V_C = 2V$; $\beta_{ac} = 100$; $R_B = 1K\Omega = 1000\ \Omega$

Collector current, $I_c = V_c/R_c = 2/2000 = 1$ mA

$I_B = V_B/R_B = V_B/1000 = V_B$ mA

$\beta_{ac} = 100 = I_C/I_B = 1/V_B$

$V_B = 1/100 = 0.01$ V

Therefore, $I_B = V_B$ m A = 0.01 / 1000 = 10 * 10^{-6} A = 10 μA.

Q2. 2 amplifiers are connected in a series (cascaded). The voltage gain of the first amplifier is 10 and the second has 20 voltage gain. The input signal is given as 0.01 V. Calculate the output of the AC signal?

Sol: Total voltage gain is $A_V = A_{V1} * A_{V2} = \Delta V_o / \Delta V_i$

$\Delta V_o = \Delta V_i * A_{V1} * A_{V2} = 0.01 * 10 * 20 = 2V$

Transistor at low frequencies and equivalent circuits:

The transistor can be employed as an amplifying device, that is, the output ac power is greater than the input ac power. The factor that permits an ac power output greater than the input ac power is the applied DC power. The amplifier is initially biased for the required DC voltages and currents. Then the ac to be amplified is given as input to the amplifier. If the applied ac exceeds the limit set by dc level, clipping of the peak region will result in the output. Thus, proper (faithful)

amplification design requires that the dc and ac components be sensitive to each other's requirements and limitations. The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.

BJT Transistor modeling:

• A model is an equivalent circuit that represents the AC characteristics of the transistor.

• A model uses circuit elements that approximate the behavior of the transistor.

• There are two models commonly used in small signal AC analysis of a transistor:

(i) r_e model

(ii) Hybrid Equivalent model

2.7. Switching behaviour of a Transistor & Applications

Basically transistor is a type of semiconductor device. These devices consist of three terminals. The interaction among the two terminals will be in such a way that two junctions are formed in it. These junctions and altogether the terminals are responsible for the generation of the current either the current controlled or the respective voltage-controlled devices are designed.

The basic application one can see frequently is in use is the device working as a switch. The basic concept behind its functioning is dependent on the operating modes of it. A device that prefers a low value of the voltage of DC can be switched either ON or OFF by using transistors.

Transistor as a Switch

The transistors played a prominent role by replacing themselves with vacuum tubes.This leads to an improvement in efficiency and compression in size. The main functionality of the transistor can be observed either by making it be used for amplification or to the basic application in the digital circuitry of switching. The main reason behind using this transistor for the purpose of the switch is that the current at the base controls the current present at the collector directly. If the current at the base exceeds the minimum cut-off value of voltage then the behavior of the transistor is like a close switch otherwise it will remain in open switch condition as shown in Figure 16.

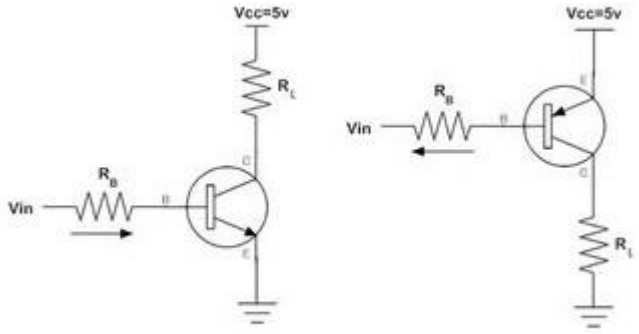


Figure 16

Transistor as Switch

By the application of bias to the base of the transistor both the types in the bipolar junction transistor can be used as switches. The areas at which the operation of the switch is preferred is either it should be completely in the region called saturation or the cut-off operating region as we have already discussed. The main theme behind using these regions is that switch mode should be completely ON or OFF. At the cut-off region the base current will be at zero. As the input is zero the collector current will also be at zero by keeping the voltage at a maximum at the collector. This is for N-P-N transistor whereas for P-N-P transistor the value of the voltage at the emitter must be negative. As there is no flow of carriers in this condition the width of the region called depletion increases stating that no current flow is evident at this condition. This type of region is referred to as the cut-off region.

Next condition in which switch is operated is saturation here the currents at the base and the collector is at maximum by keeping the voltage at the collector as a minimum. This operating condition makes the transistor to operate at fully ON mode. This is for N-P-N transistor whereas for P-N-P the emitter voltage value must be kept positive with respect to that of the base.

This operation of the transistor is known as a single pole single throw (SPST). This indicates that when the zero of the signal applied to the base the transistor will be ON otherwise it will be OFF.

N-P-N Transistor as a Switch

Once the voltage has been applied to the region of base based on it the operation of the switching is performed. Similar to the condition of the diode there exist the cut-in voltage. Between the region of the emitter and the base, the voltage applied must reach the cut-in voltage. If its crosses it the transistor is said to be ON otherwise OFF. Once the transistor is in ON condition the current generated tends to flow from source to the load. The load can be either the led or the resistor, load depends based on the requirement.

P-N-P Transistor as a Switch

The operating conditions of the P-N-P and N-P-N transistor differ in the application positive or the negative voltages. But the criteria of the operation remain the same. If it is in ON condition the flow of current is observed otherwise it is OFF. The load here is connected to the respective ground of the transistor and then the transistor P-N-P switches power. In this case, the terminal base is connected to the ground.

Applications of Transistor as switch

The applications of the transistor used as a switch are as follows:

1. The most frequently used practical application that is used for the transistor as a switch is functioning of LED.
2. The relay operation can be controlled by making the necessary changes in the circuit so that any external device is connected with respect to the relay and gets controlled.
3. The dc motors can be controlled and monitored by using this concept of transistors. In order to turn ON the motor and OFF it this application is used. By varying the values of the frequencies of transistor the speed of the motor can be varied.
4. One of the examples of these switches is light-bulb. It facilitates to switch on the light provided a bright environment and switches off based on the dark environment. It is done by using a light-dependent resistor (LDR).
5. A component called thermistor that senses the surrounding temperature can be monitored by using this switching technique. The thermistor is referred to as a resistor. This resistance tends to increase when the sensed temperature is low and a decrease in the resistance is observed when the sensed temperature is high.

There are many applications in the practical world regarding relays, motors, etc., in every practical involvement plays a major role in switching the devices. This can be either for the alternating supply or the direct supply. Nowadays in the curiosity of providing comfortable and secure living the design of automation systems or the fire detection systems this switching technique of the devices plays a dominant role. Can you explain the basic purpose of usage of relays in the automation circuits?

2.8. Biasing Schemes of a transistor -

Transistor Biasing is the process of setting a transistor's DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor. Transistor biasing can be accomplished by various techniques that give rise to different kinds of biasing circuits. However, all of these circuits are based on the principle of providing the right amount of base current, $I_{B,}$ and, in turn, the collector current, I_C from the supply voltage, V_{CC} when no signal is present at an input. Moreover, the collector resistor R_C has to be chosen so that the collector-emitter voltage, $V_{CE,}$ remains greater than 0.5V for transistors made of germanium and greater than 1V for the transistors made of silicon. Biasing circuits most commonly used are

1. Fixed Base Bias or Fixed Resistance Bias
2. Collector Feedback Bias
3. Emitter Bias
4. Voltage Divider Bias

1. Fixed Base Bias or Fixed Resistance Bias - The biasing circuit shown in the Figure 22. It has a base resistor R_B connected between the base and the V_{CC}. Here the base-emitter junction of the transistor is forward biased by the voltage drop across R_B, which is the result of I_B flowing through it. From the figure, the mathematical expression for I_B is obtained as –

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

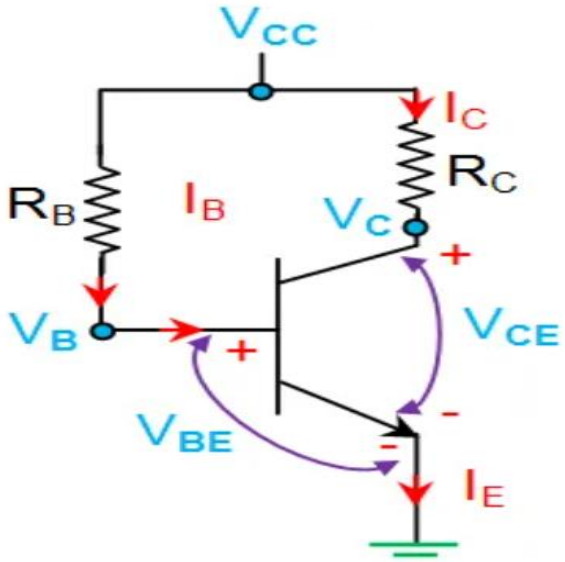


Figure 17

Here the values of V_{CC} and V_{BE} are fixed, while the value for RB is constant once the circuit is designed. This leads to a constant value for I_B, resulting in a fixed operating point due to which the circuit is named fixed base bias. This kind of bias results in a stability factor of (β+1), leading to inferior thermal stability.

2. Collector Feedback Bias

In this circuit as shown in Figure 18, the base resistor R_B is connected across the collector and the base terminals of the transistor. This means that the base voltage, V_B, and the collector voltage, V_C are inter-dependent because

$$V_B = V_C - I_B R_B$$

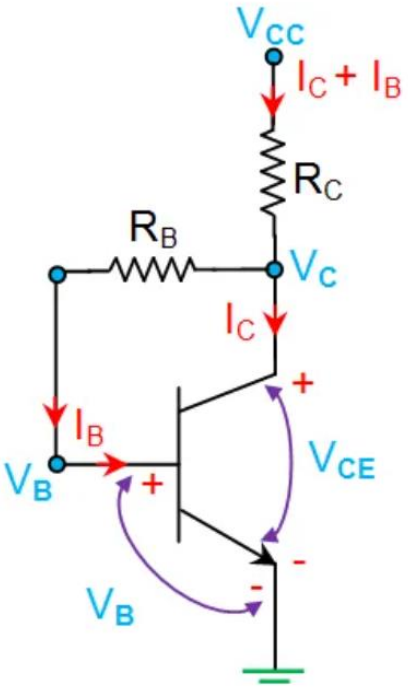


Figure 18

where

$$V_C = V_{CC} - (I_B + I_C)R_C$$

From these equations, it is seen that an increase in I_C decreases V_C, which results in a reduced I_B, automatically reducing I_C. This indicates that, for this type of biasing network, the Q-point (operating point) remains fixed irrespective of the variations in the load current causing the transistor to always be in its active region regardless of β value. This kind of relatively simple bias has a stability factor that is less than (β+1), which results in better stability when compared to fixed bias.

3. Emitter Bias –

This biasing network uses two supply voltages, V_{CC} and V_{EE}, equal but opposite in polarity as shown in Figure 24. Here V_{EE} forward biases the base-emitter junction through R_E while V_{CC} reverse biases the collector-base junction. Moreover

$$V_E = -V_{EE} + I_E R_E \ , \quad V_C = V_{CC} - I_C R_C \ , \ V_B = V_{BE} + V_E \ , \quad I_C = \beta\, I_B, \quad I_E \approx I_C$$

in this kind of biasing, I_C can be independent of both β and V_{BE} by choosing $R_E >> R_B/\beta$ and $V_{EE} >> V_{BE}$, respectively, which results in a stable operating point.

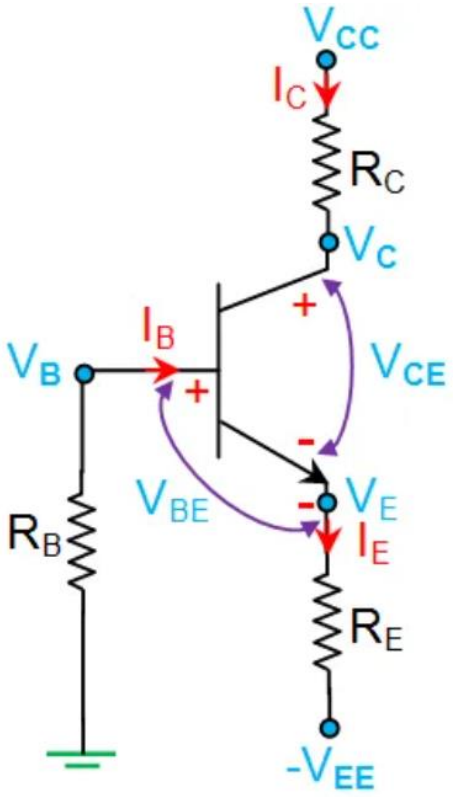


Figure 19

4. Voltage Divider Bias

This type of biasing network as shown in Figure 20 employs a voltage divider formed by the resistors R_1 and R_2 to bias the transistor. This means that the voltage developed across R_2 will be the base voltage of the transistor, which forward biases its base-emitter junction. In general, the current through R_2 will be fixed to be 10 times the required base current, I_B (i.e., $I_2 = 10I_B$). This is done to avoid its effect on the voltage divider current or the changes in β. Further, from the circuit, one gets

$$I_B = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$V_E = I_E R_E$$

$$V_B = I_2 R_2 = V_{BE} + V_E$$

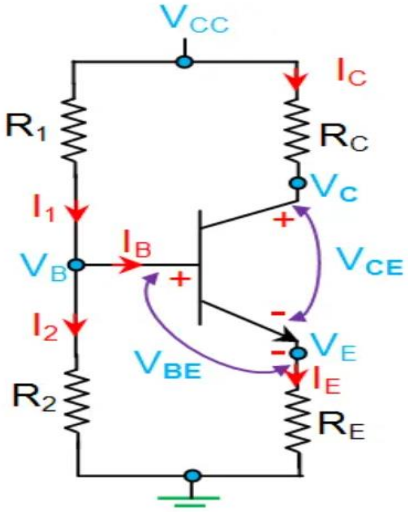


Figure 20

In this kind of biasing, I_C is resistant to the changes in both β as well as $V_{BE,}$ which results in a stability factor of 1 (theoretically), the maximum possible thermal stability. As I_C increases due to a temperature rise, I_E increases, causing an increase in the emitter voltage $V_{E,}$ reducing the base-emitter voltage V_{BE}. This results in the decrease of base current $I_{B,}$ which restores I_C to its original value. The higher stability offered by this biasing circuit makes it most widely used despite providing a decreased amplifier gain due to the presence of R_E.

2.9. Feedback in amplifiers –

Principle of Feedback Amplifier

A feedback amplifier generally consists of two parts. They are the amplifier and the feedback circuit as shown in Figure 21. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure.

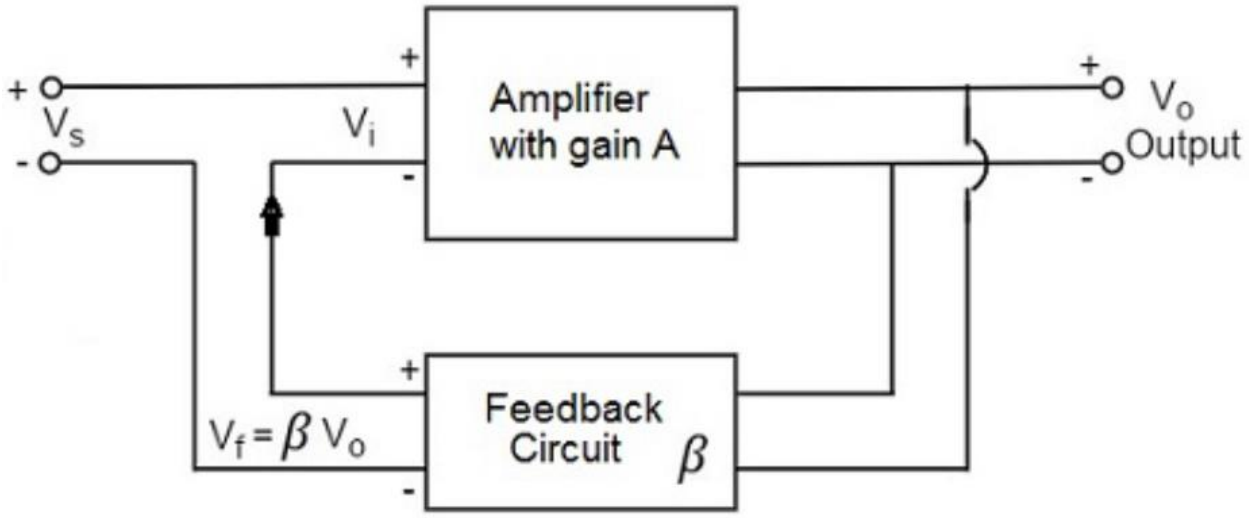


Figure 21

From the above figure, the gain of the amplifier is represented as A. The gain of the amplifier is the ratio of output voltage V_o to the input voltage V_i. the feedback network extracts a voltage $V_f = \beta V_o$ from the output V_o of the amplifier. This voltage is added for positive feedback and subtracted for negative feedback, from the signal voltage V_s. Now,

$V_i = V_s + V_f = V_s + \beta V_o V_i = V_s + V_f = V_s + \beta V_o$

$V_i = V_s - V_f = V_s - \beta V_o$

The quantity $\beta = V_f/V_o$ is called as feedback ratio or feedback fraction.

Let us consider the case of negative feedback. The output V_o must be equal to the input voltage $(V_s - \beta V_o)$ multiplied by the gain A of the amplifier.

Hence,

$$(V_s - \beta V_o)\, A = V_o \quad (V_s - \beta V_o)\, A = V_o$$

Or

$$AV_s - A\beta V_o = V_o$$

Or

$$AV_s = V_o\,(1 + A\beta)$$

Therefore,

$$\frac{V_O}{V_S} = \frac{A}{1 + A\beta}$$

Let A_f be the overall gain (gain with the feedback) of the amplifier. This is defined as the ratio of output voltage V_o to the applied signal voltage V_s, i.e.,

$$A_f = \frac{Output\ voltage}{Input\ signal\ voltage} = \frac{V_O}{V_S}$$

The equation of gain of the feedback amplifier, with positive feedback is given by

$$A_f = \frac{A}{1 - A\beta}$$

These are the standard equations to calculate the gain of feedback amplifiers.

Types of Feedbacks

The process of injecting a fraction of output energy of some device back to the input is known as Feedback. It has been found that feedback is very useful in reducing noise and making the amplifier operation stable. Depending upon whether the feedback signal **aids** or **opposes** the input signal, there are two types of feedbacks used.

Positive Feedback

The feedback in which the feedback energy i.e., either voltage or current is in phase with the input signal and thus aids it is called as Positive feedback. Both the input signal and feedback signal introduces a phase shift of 180^o thus making a 360^o resultant phase shift around the loop, to be finally in phase with the input signal.Though the positive feedback increases the gain of the amplifier, it has the disadvantages such as

- Increasing distortion
- Instability

It is because of these disadvantages the positive feedback is not recommended for the amplifiers. If the positive feedback is sufficiently large, it leads to oscillations, by which oscillator circuits are formed. This concept will be discussed in OSCILLATORS tutorial.

Negative Feedback

The feedback in which the feedback energy i.e., either voltage or current is out of phase with the input and thus opposes it, is called as negative feedback. In negative feedback, the amplifier introduces a phase shift of 180^o into the circuit while the feedback network is so designed that it produces no phase shift or zero phase shift. Thus the resultant feedback voltage V_f is 180^o out of phase with the input signal V_{in}. Though the gain of negative feedback amplifier is reduced, there are many advantages of negative feedback such as

- Stability of gain is improved
- Reduction in distortion
- Reduction in noise
- Increase in input impedance
- Decrease in output impedance
- Increase in the range of uniform application

It is because of these advantages negative feedback is frequently employed in amplifiers.

2.10 Numericals

Q3. The overall gain of a multistage amplifier is 140. When negative voltage feedback is applied, the gain is reduced to 17.5. Find the fraction of the output that is fedback to the input.

Sol:

$$A_v = 140, \quad A_{vf} = 17.5$$

Let m_v be the feedback fraction. Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

or $$17.5 = \frac{140}{1 + 140 m_v}$$

or $$17.5 + 2450 m_v = 140$$

$$\therefore \quad m_v = \frac{140 - 17.5}{2450} = \mathbf{\frac{1}{20}}$$

Q4. When negative voltage feedback is applied to an amplifier of gain 100, the overall gain falls to 50.
(i) Calculate the fraction of the output voltage fedback.

(ii) If this fraction is maintained, calculate the value of the amplifier gain required if the overall stage gain is to be 75.

Sol:

(*i*) Gain without feedback, $A_v = 100$

Gain with feedback, $A_{vf} = 50$

Let m_v be the fraction of the output voltage fedback.

Now $$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

or $$50 = \frac{100}{1 + 100\, m_v}$$

or $$50 + 5000\, m_v = 100$$

or $$m_v = \frac{100 - 50}{5000} = \mathbf{0.01}$$

(*ii*) $A_{vf} = 75\,; \quad m_v = 0.01\,; \quad A_v = ?$

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

or $$75 = \frac{A_v}{1 + 0.01\, A_v}$$

or $$75 + 0.75\, A_v = A_v$$

$\therefore$ $$A_v = \frac{75}{1 - 0.75} = \mathbf{300}$$

UNIT 3: FET and MOSFET

Outline of unit 3

3.1 Objectives:

After study of unit the student will be able

i) To understand the family of FET and MOSFET

ii) To understand the construction and symbol of FET and MOSFET

iii) To understand the characteristics of FET and MOSFET

iv) To explain the use of FET and MOSFET as an amplifier

v) To describe Depletion and enhancement mode

vi) To describe Q point and load line

3.2 Introduction

In bipolar junction transistor current conduction takes place by both holes and electrons. However because of low input impedance and considerable noise level, another device named FET is increasingly gained popularity in electronics market. It is a three terminal semiconductor device like BJT in which the current is controlled by an applied electric field. Unlike BJT It is a unipolar device because the current is carried by one type of carriers, specially the majority carriers. Figure 3.1 shows the different members of FET family which will be discussed in detail in the chapter.

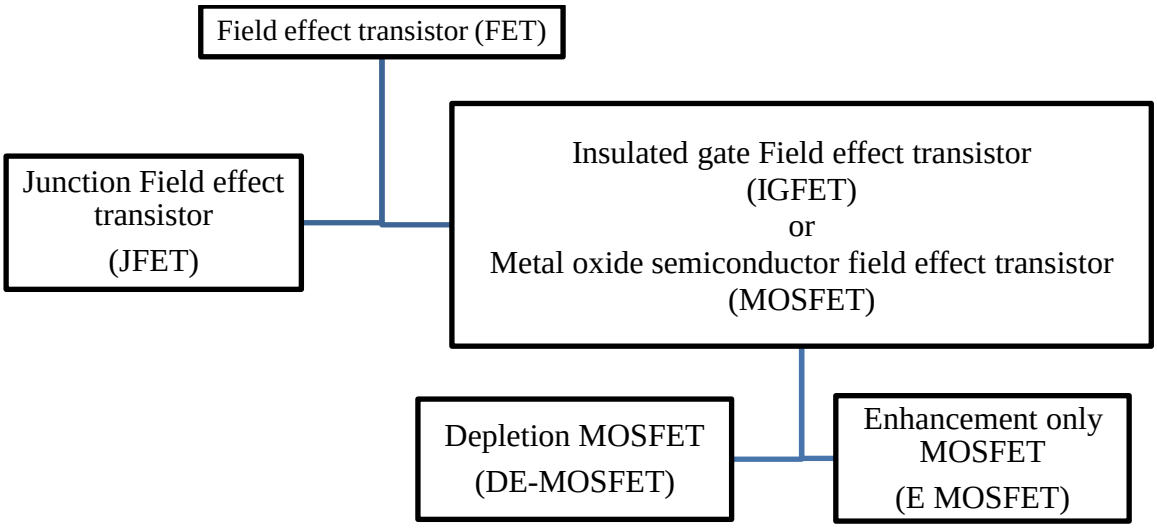


Figure 3.1 FET family

3.2.1 Difference between FET and BJT

a) The FET is a voltage controlled device like vacuum tubes while BJT is a current controlled device.
b) The FET exhibits a high input impedance as the gate source terminal is reverse biased, while a BJT exhibits low input impedance as emitter base junction is forward biased. This exhibits a high degree of isolation between input and output. Loading effect is low.
c) FET is a unipolar device while BJT is a bipolar device.
d) The FET is less noisy and has a better thermal stability in comparison to BJT.
e) The FET is simpler to fabricate and occupies less space in integrated form.

The main disadvantage of the FET is lower gain-bandwidth product in comparison with BJT. Also MOSFET is very susceptible to overload voltages.

3.3 Junction Field Effect transistor (JFET)

3.3.1 Basic construction and symbol of JFET: JFET consists of a P type or N type silicon bar consists of two PN junctions at the both sides are connected internally and a common terminal called GATE is taken out. As shown in Figure 3.2(a) and (b) the terminal through which the majority carriers inter is called SOURCE and the terminal through which the majority carrier leave the bar is called DRAIN. The region of Nor P type semiconductor material between two gate regions is called the channel though which the majority charge carriers move from source to drain. Hence If the bar is of n type, it is called N-channelJFET and if the bar is of p type is, It is called P-channelJFET.

*From the Figure 3.2 it seems as if there are three doped material regions However in reality the Gate material surrounds the channel like a belt surrounding the waist and leaves the bar as conducting channel for the charge carriers.

Thus a JFET has essentially three terminals SOURCE, GATE and DRAIN with a conducting channel which are analogous to emitter, base and collector of BJT respectively.

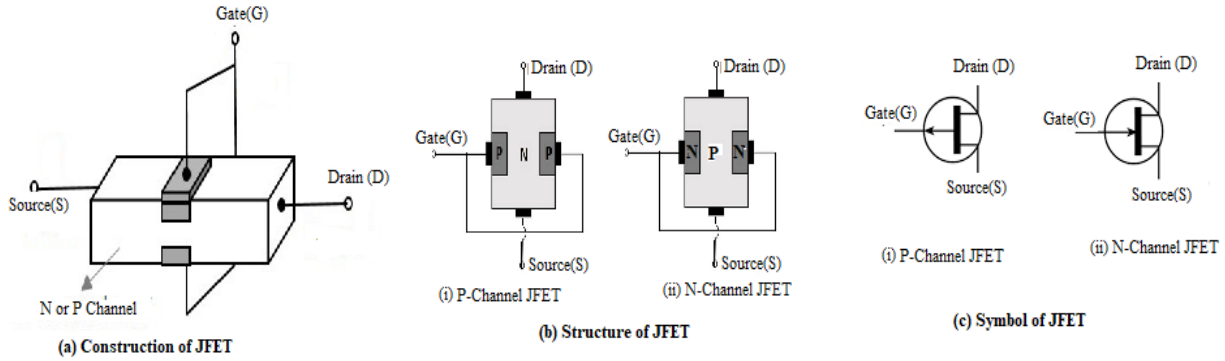


Figure 3.2 Construction and symbol of JFET

Schematic symbol of JFET: As shown in Figure 3.3(c) the vertical line in the symbol may be thought as channel and source and drain D connected to the line. Direction of the arrow to the gate indicates the direction of gate current flow hence for N-channelFET arrow at the gate junction point into the device and in P-channelit is away from the device.

3.3.2 JFET polarities: As shown in Figure 3.3**,** for the proper functioning of JFET the voltage between source and gate is such that the gate is always reverse biased, i.e. gate terminal is connected to –ve terminal of battery in N-channelJFET while gate is connected to + terminal of battery in P-channelJFET, also the source and drain terminals are interchangeable, i.e. any of two end can be used as Source and other as drain.

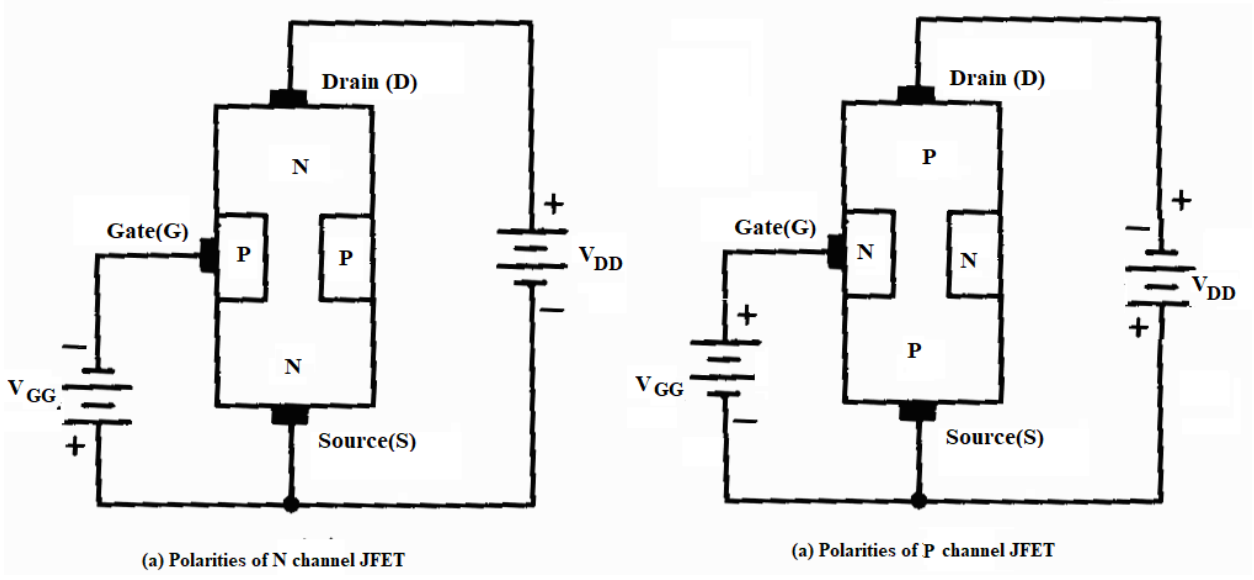


Figure 3.3 Polarities of JFET

Therefore in JFET

1. Gate is reverse biased means JFET has High input impedance.
2. Drain is biased such that the drain current flows from source to drain.
3. In all JFETs, source current I_S is equal to the drain current i.e. $I_s=I_d$

3.3.3 Principle and working of JFET:

Principle: The PN junction formed by P type gate and N type channel at two sides form two depletion layers. The current conduction by charge carriers (I.e. electron for N channel) is through the channel between the depletion layers and moves out of the drain. Now as the reverse voltage V_{GS} increases, the depletion layer will be wider and the conducting channel will be narrower.. Reduced channel width means greater channel resistance and decreased drain current. Thus JFET operates on the principle that the width and the resistance of this channel as well as drain current can be controlled by the changing the reverse input voltage $V_{GS.}$ Thus JFET is a voltage controlled device.

Working: The working of JFET can be explained as under

(i) When no bias is applied on the gate (i.e. $V_{GS} = 0$) as well drain (i.e. $V_{DS} = 0$),the depletion layer around the PN junction are of equal thickness and symmetrical (Figure 3.4(a)).

(ii) When a voltage V_{DS} is applied between drain and source and no bias is applied on the gate (i.e. $V_{GS} = 0$) drain current starts flowing causes a uniform voltage drop across the channel resistance from terminal D to terminal S which results greater reverse biases at the drain end then that of source end .hence the wedge shaped depletion layer formed and channel becomes narrower at the drain end.(Fig.)The size of the depletion layer formed determines the width of the channel hence the magnitude of drain current (Figure 3.4(b)).

(iii) However at a certain value of V_{DS} , current becomes constant at its maximum value is called pinch off region. In pinch off region the channel resistance increases in proportion to increase in V_{DS} and so keeps the drain current almost constant and the reverse bias required by the gate channel junction is supplied entirely by the voltage drop across the channel resistance due to flow of I_{DSS} and not by the external bias

because V_{GS} = 0.and the width of channel remains constant in this region. (Figure 3.4(c)).

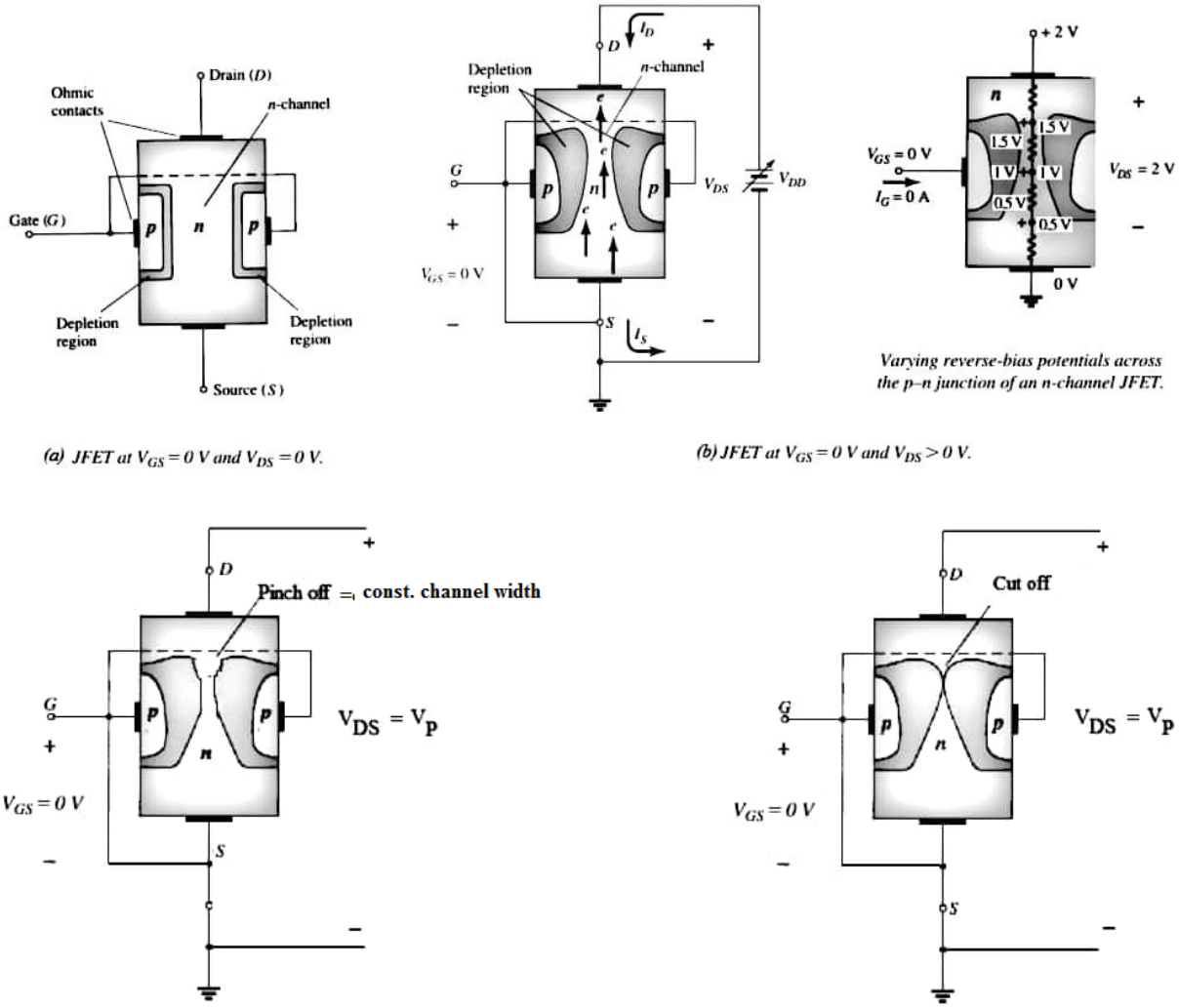


Figure 3.4 Working of JFET

(iv) When a voltage V_{DS} is applied between drain and source and a reverse voltage V_{GS} is applied between the gate and the source (Figure 3.4(d)) the width of the depletion layer is increased subsequently the width of conducting channel is decreased, hence the drain current is reduced. If the reverse bias is further increased, at certain value depletion layer meet at the center and the drain current I_D is cutoff completely.

*****Cut off voltage ($V_{GS(OFF)}$) will always have the same magnitude as pinch off voltage (V_P).

i.e. $V_{GS(OFF)} = - V_P$

**There is a distinct difference between V_P and $V_{GS(OFF)}$. Pinch off voltage (V_P) is the minimum drain-source voltage at which the channel width becomes constant which results constant drain current. While $V_{GS(OFF)}$ is the gate source voltage where the channel is completely cutoff and the drain current becomes zero.

3.3.4 JFET parameters: The performance of JFET can be determined using certain parameters named as i) Amplification factor ii) A.C. drain resistance, iii) Mutual or transconductane.

i) Amplification factor (μ): Amplification factor of JFET indicates the effectiveness of gate voltage to control drain current in comparison with drain voltage.e.g. If JFET has amplification factor 20 then it means gate voltage is 20 times more effective to control drain current in comparison with drain voltage.

It is defined as the ratio of change in drain to source voltage to the change in gate to source voltage at constant drain current.

Therefore Amplification factor (μ) = $\frac{\Delta V_{DS}}{\Delta V_{GS}}$ at constant I_D.

Since μ is the ratio of two voltages, It has no units.

ii) A.C. drain resistance or dynamic drain resistance (r_d)=It is the a.c. resistance between drain and source terminals when JFET is working in pinch off region. It is given by the slope of drain characteristics in pinch off region and measured in ohms.

Mathematically A.C**.** drain resistance is defined as the ratio of drain to source voltage to the chance in drain current at constant gate source voltage.

Therefore A.C. drain resistance (r_d) = $\frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}.

Typical value of r_d range from 100 KΩ to 1 MΩ in For JFET and from 10 KΩ to 100 KΩ for MOSFET. The reciprocal of a.c. drain resistance is called the drain or channel conductance.

iii) Mutual or Transconductane (gm): Transconductane measures the control of gate voltage over drain current.

Transcondcance of FET is defined as the ratio of change in drain current to the change in gate source voltage at constant drain to source voltage.

Transconductane (g_m) = $\frac{\Delta V_{GS}}{\Delta I_D}$ at constant V_{DS}.

Its unit is mho or Siemens(S) and simply the slope of transfer characteristic of JFET.

Typical value of g_m range from 0.1 to 20 mS for JFET as well as MOSFET.

Relation among JFET parameters

We know $(\mu) = \frac{\Delta V_{DS}}{\Delta V_{GS}}$

Multiplying both numerator and denominator on R.H.S. by ΔI_D, we get

$$(\mu) = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D}$$

Rearranging the term $(\mu) = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = r_d \times g_m$

i.e. amplification factor = a.c. drain resistance × transconductance

All these parameters and their relation resembles with parameter of transistor.

3.3.5 Biasing of junction field effect transistor:

For the proper functioning of JFET, Gate terminal of JFET should always be reverse biased. This can be achieved by inserting a battery in the gate circuit or by a circuit known as biasing circuit. Biasing circuit method is preferred because batteries are costly and also needs frequent replacements.

Various bias methods for a JFET are discussed below:

i. ***Fixed bias:*** As shown in Figure 3.5 (a) in this method JFET is biased by a battery V_{GG} to ensure that gate is always negative w.r.t. source during all parts of the signal.

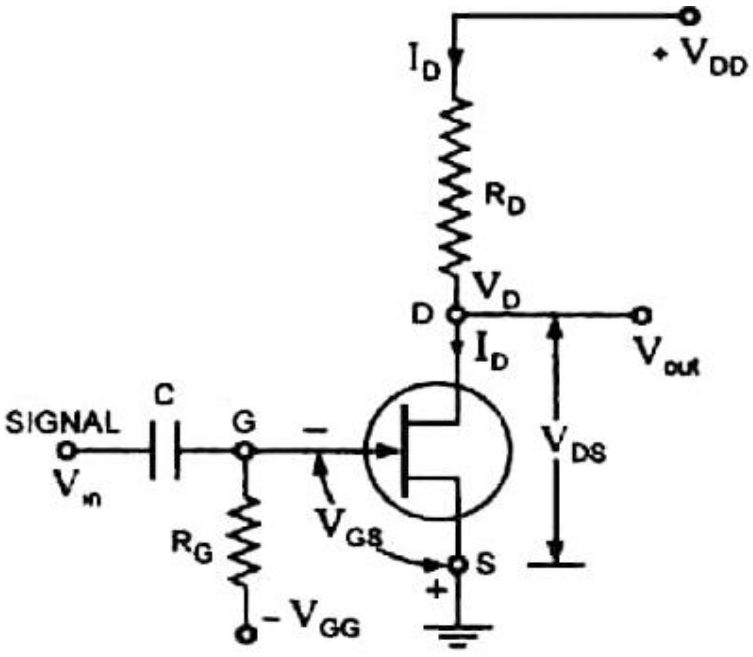


Figure 3.5 (a) Fixed bias method of JFET

Since the input impedance of JFET is very high therefore no gate current flows. Hence there will

be no voltage drop across R_g.

Hence $V_{GS}=V_{GG}$

Now drain current $I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(OFF)}}\right)^2$

The value of V_{DS} is given by :

$$V_{DS} = V_{DD} - I_D r_D$$

Thus the d.c. values of I_D and V_{DS} can be determined. Since V_{GG} is fixed value of dc supply and the, magnitude of gate to source voltage VGS is also fixed, hence the circuit is called fixed bias circuit.

ii. Self bias: It eliminates the requirement of two dc power supplies. Only drain supply is used and a resistance R_S known as bias resistance is connected in the source terminal (Figure 3.5(b)). A potential drop across R_S is developed due to the dc component of I_D flowing through it, which reduces the gate source reverse voltage required for JFET operation. Since the gate G is grounded through resistance R_G, gate current and the gate voltage will be Zero.

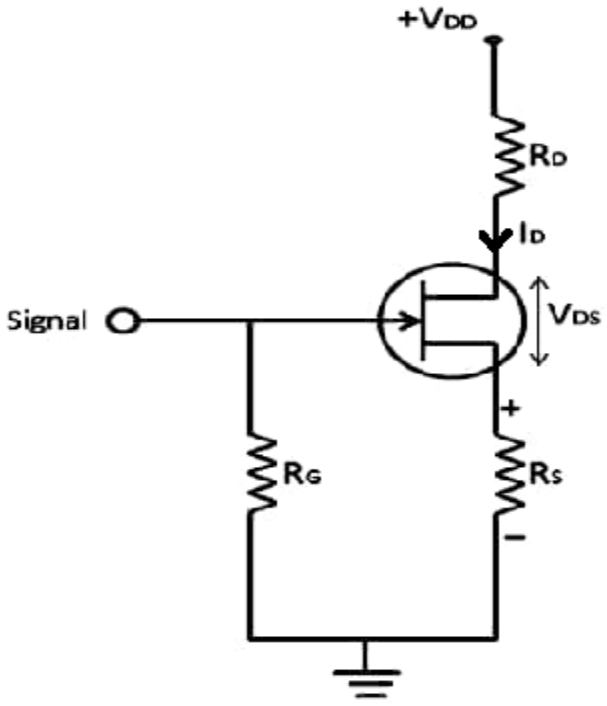


Figure 3.5 (b) self bias method of JFET

Therefore the voltage on the source to ground $V_S=I_DR_S$

So that gate to source voltage (or gate bias)

$V_{GS}=V_G-V_S=0-I_DR_S=-I_DR_S$

Thus the voltage V_{GS} keeps gate voltage negative with respect to source. As no external source is required for biasing the gate hence the method is known as self bias.

3. Potential divider method: Figure 3.5 (c) shows the potential divider method. Here resistance R_1 and R_2 form a potential divider across drain supply V_{DD}.The voltage V_2 across R_2 provides the necessary bias.

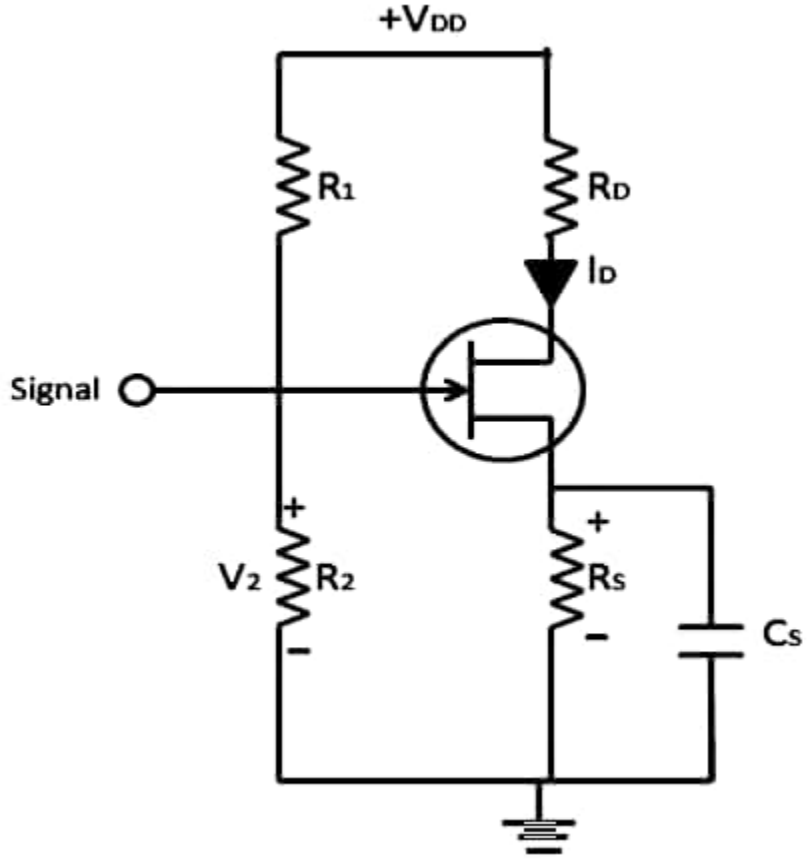


Figure 3.5 (c) Potential divider method of JFET

The voltage at the gate to ground is given by

$$V_G = \frac{R_1}{R_1 + R_2} V_{DD}$$

If I_D is the drain current and R_S is the resistance connected with the source terminal then the voltage on the source to ground is

$$V_S=I_DR_S$$

Now $V_2= V_{GS}+V_S =V_{GS}+I_DR_S$

Or gate to source voltage or gate bias $V_{GS}= V_2-I_DR_S$

The circuit is so designed that I_DR_S is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage.

The capacitor C_S connected across R_S again acts as bypass capacitor.

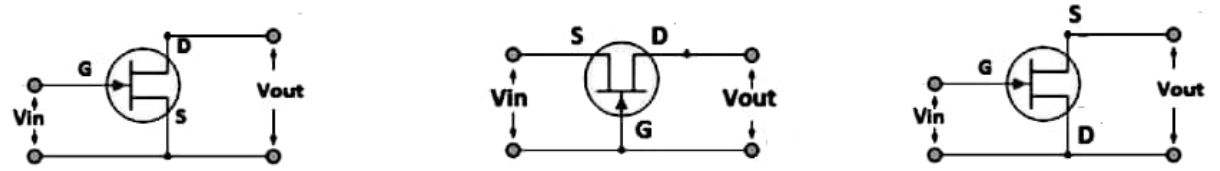
The operating point can be find as following.$I_D = \frac{V_2 - V_{GS}}{R_S}$

And $V_{DS} = V_{DD} - I_D(R_D + R_S)$

Because of Good stability of operating point this method of circuit biasing is widely used in JFET circuit.

3.3.6 JFET configuration: As JFET is a three terminal device SOURCE, GATE and DRAIN terminals. However we need four terminals two for input and two for output to connect JFET in electronic circuit. To overcome this difficulty one terminal of the JFET common to both input and terminals (Figure 3.6) . Accordingly a JFET can be configured in the following three ways:

i. Common source configuration
ii. Common gate configuration
iii. Common drain configuration.



(a) Common source Configuration (b) Common gate configuation (c) Common drain configuration

Figure 3.6 Different JFET configuration

We generally use common source connection as this connection provides high input impedance, good voltage gain and moderate output impedance. However in this configuration output is 180^0 out of phase with the input signal.

Example 3.1. For an N channel JFET, given that μ= 40, r_d=10 KΩ, ΔV_{GS}= - .5V.Find the values of (i) Δ V_{DS} ,(ii) r_d) (iii g_m .

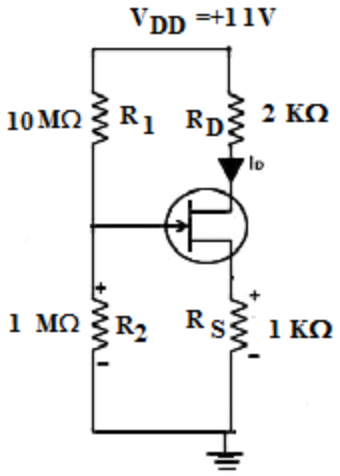
Solution $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ $\quad \therefore \Delta V_{DS} = \mu \times \Delta V_{GS} = 40 \times .5\, V = 20\, V$

Also $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ $\quad \therefore \Delta I_D = \frac{\Delta V_{DS}}{r_d} = \frac{20\, V}{10\, k\Omega} = 2mA$

Now $\mu = r_d \times g_m$ $\quad \therefore g_m = \frac{\mu}{r_d} = \frac{40}{10\, K\Omega} = 4 \times 10^{-3}\, Mho$

Ans. $(i)\Delta V_{DS} = 20\,V, (ii)\ \Delta I_D = 2mA, (iii) g_m = 4 \times 10^{-3}\ Mho$

Example 3.2. From the figure, calculate the value of I_D and V_{GS} for the JFET with voltage-divider bias. Given V_{DS}=7V



Solution: $I_D = \frac{V_{DD}-V_{DS}}{R_D} = \frac{11V-7V}{2\ K\Omega} = 2\ mA$

Now $V_S = I_D R_S = (2\ mA)(1\ K\Omega) = 2\ \text{V}$

$$V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2 = \frac{11\ V}{(10.5+1)M\Omega} \times 1M\Omega = 1\ V$$

$$\therefore\ V_{GS} = V_G - V_S = 1 - 2 = -1\ V$$

Ans. $I_D = 2\ mA$ **and** $V_{GS} = -1\ V$

3.4 Static and dynamic characteristics for smaller drain voltages

Drain and transfer characteristics are the two important characteristics of JFET. Figure 3.7 represents the circuit diagram to obtain these two characteristics by using N-channelJFET connected in the common source mode.

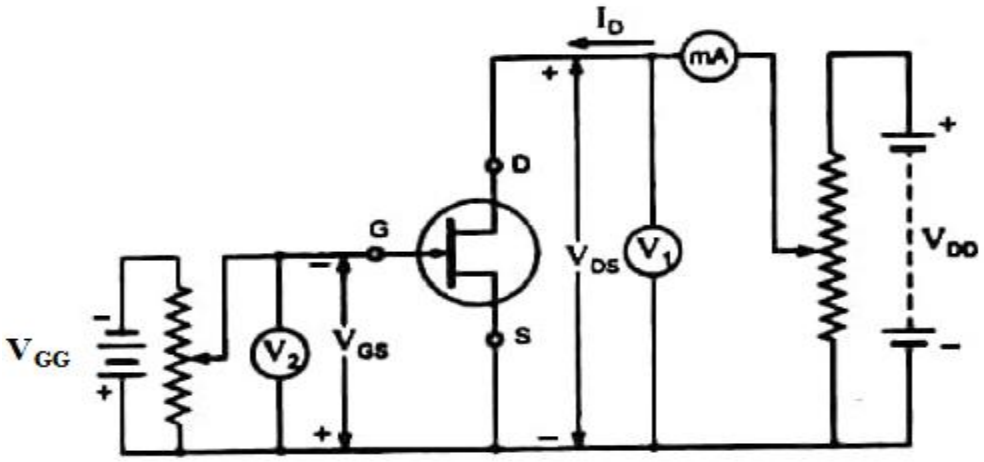


Figure 3.7 Circuit diagram to study characteristics of JFET

3.4.1 Output or drain characteristics of JFET: It is a curve drawn between drain current (I_D) and drain to source voltage (V_{DS}) for fixed gate source voltage (V_{GS}). The circuit diagram for obtaining the drain or output characteristic of JFET is shown in the Figure 3.7. where V_{GG} is the

gate bias supply and V_{DD} is the drain source supply .keeping gate source voltage at some fixed value, the drain source voltage is changed in steps and corresponding drain current is noted. Different drain characteristics can be drawn by setting gate source voltage at different fixed value (Figure 3.8(b)).

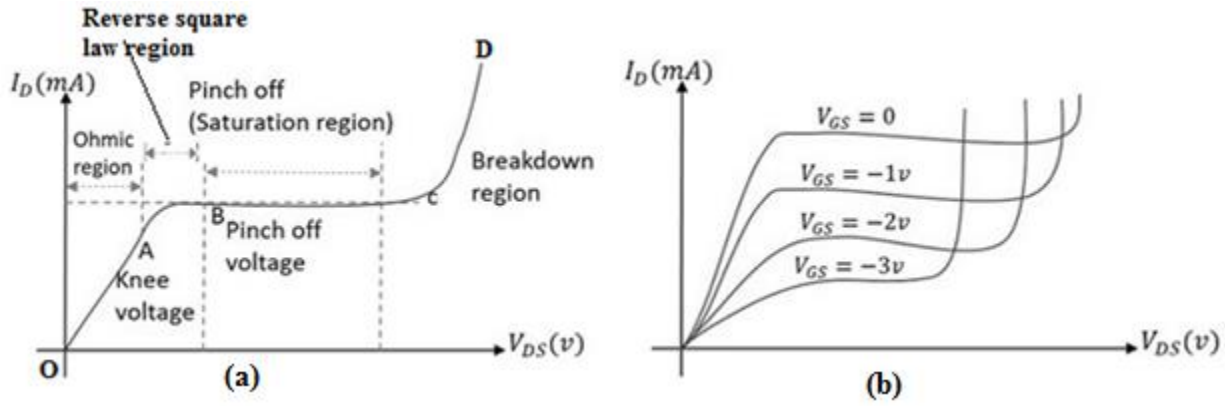


Figure 3.8 Drain characteristics of JFET

As shown in Figure 3.8(a) the drain characteristics with V_{GS}=0 can be sub divided in the following regions

i. **Ohmic region (OA Curve)**: Drain current varies linearly with drain source voltage and obeys Ohm's law. at this region JFET behaves like an ordinary resistance till point A (knee point).

ii. **Reverse square law region (AB curve)**: In this region, drain current increases with the increase in drain source voltage following reverse square law. With the increase in drain current I_D, the ohmic voltage drop between the source and channel region reverse biases the gate junction a non uniform way. it is more at the drain end than that of at a source end. With the increase in drain source voltage V_{DS}, the conducting portion of the channel (effective width of channel) decreases more at the drain end. At the drain source voltage, corresponding to the point B (Pinch off point),the channel width is reduced to a minimum value. The drain to source voltage at which the channel pinch off occurs is called pinch off voltage.

iii. **Pinch off region (BC curve)** the region in which drain current becomes constant at its maximum value is called pinch off region. It is also known as saturation region or constant current region. In this region JFET operates as a constant current device and it is normal operating region of the JFET when used as an amplifier.

The drain current in the pinch off region with V_{GS} =0 is referred to the drain source saturation current (I_{DSS})

Drain current I_D at a given gate source voltage V_{GS} in the pinch off region is given by Shockley's equation: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$

Where $V_{GS(off)}$ is cut off gate source voltage.

iv. **Breakdown region (CD curve)** after pinch off voltage the channel width become so narrow that depletion layer almost touch each other .the drain current passes through the small passage between these layers .if drain source voltage is increased beyond. C JFET enters the Breakdown region where a small change in V_{DS} produce very large change in drain current because of Avalanche breakdown of reverse Biased Gate channel PN junction.

Thus the JFET at first behaves as a register then as a constant current source and finally constant voltage source.

Figure 3.8(b) shows the drain characteristics with different values of gate source voltage V_{GS}.

It is observed from the characteristic curves that when the negative gate bias voltage is increased the maximum saturation drain current becomes smaller because the conducting channel is now becomes narrower as well as the pinch off condition is reached at a lower value of drain current when compared with V_{GS}=0.

3.4.2 Transfer characteristics or mutual characteristics of JFET:

Transfer or mutual characteristics are drawn between drain current and gate source voltage for a

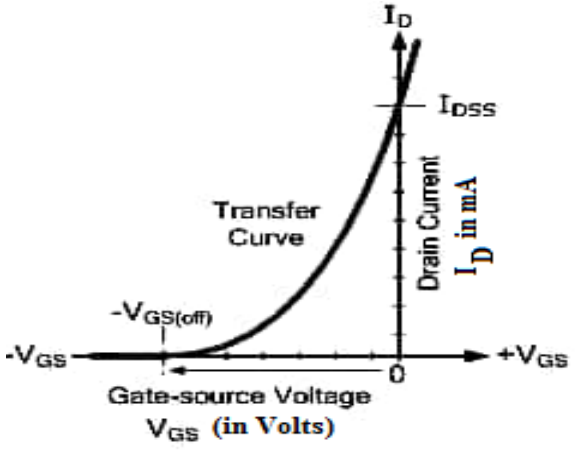


Figure 3.9 Transfer characteristics of JFET

fixed value of drain source voltage. For this V_{DS} is kept fixed while V_{GS} is very in steps and corresponding drain current is noted. This curve resembles with the mutual characteristic of a vacuum triode or transistor. It is observed from the transfer characteristic curve (Figure 3.9) ,as gate source voltage increases, the reverse bias of gate hence drain current decreases.

Value of gate-source voltage when drain current becomes zero is called gate-source cutoff voltage and the point is called cut off point. gate-source cutoff voltage on the transfer characteristic is equal to the Pinch off voltage .The upper end of the curve is shown by the drain current value equal to I_{DSS}, while the lower end by a voltage equal to $V_{GS(off)}$.

Note: A P-channelJFET operates in the same way and have the similar characteristics as an N-channelJFET except that channel carriers are holes instead of electrons and polarities of V_{GS} and V_{DS} are reversed.

Example 3.3. A JFET has a drain current of 5 mA, If I_{DSS}=20 mA and $V_{GS(off)}$ = - 5 V.Find the value of (i) V_{GS} and (ii)V_P

Solution: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$

$5mA = 20\ mA\left(1 - \frac{V_{GS}}{-5}\right)^2$ hence $\left(1 + \frac{V_{GS}}{5}\right)^2 = \frac{1}{4}$ or $\left(1 + \frac{V_{GS}}{5}\right) = \frac{1}{2}$

Or $\frac{V_{GS}}{5} = -\frac{1}{2}$ or $V_{GS} = -2.5\ V$

And $V_p = -V_{GS} = 2.5V$

Ans. (i) $V_{GS} = -2.5$ V (ii) $V_{DS} = 2.5$ V

3.5 Load line and Q point:

Similar to transistor the dc load line is drawn upon the output characteristics of the FET. As shown in Figure 3.10, the drain source voltage V_{DS} at any instant is given by the equation:

$V_{DS}=V_{DD}-I_DR_D$

where V_{DD} is drain supply voltage and I_DR_D is the voltage drop across R_D.

Let us consider two particular cases:

(i) When I_D=0, then $V_{DS}=V_{DD}$ …….cutoff point B

(ii) When V_{DS}=0, then $I_D=V_{DD}/R_D$ …….saturation point A

If we join cutoff and saturation point, we get the DC load line (Figure 3.10 (b))

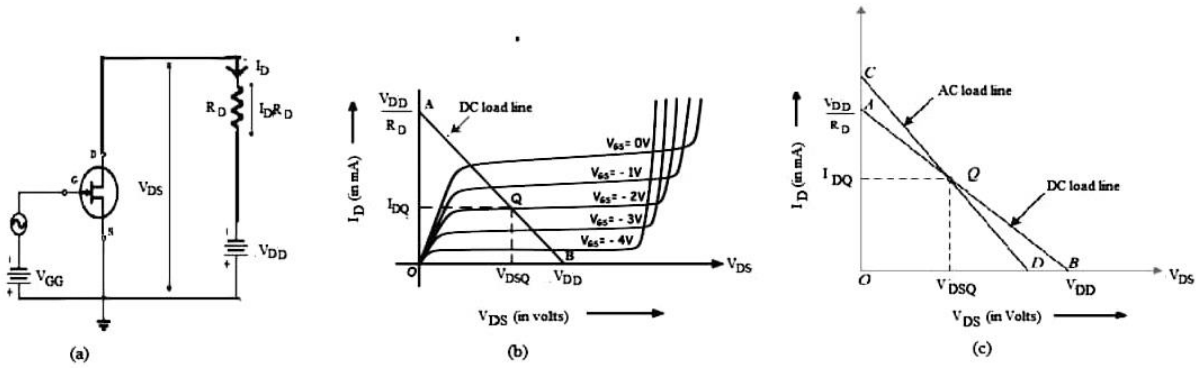


Figure 3.10 Load line and Operating point(Q point)

Q point or operating point defines the dc conditions (i.e. the value of I_D and V_{DS}) in the absence of input signal .Q point is selected such that maximum possible variations in output voltage is possible when the drain current is varied by an input signal. However when maximum possible voltage swing is not required the bias point may be at any convenient position in the load line. As shown in Figure 3.10(b). the Q point conditions are V_{DSQ} and I_{DQ}.

When an a.c. signal causes the change in output voltage and current of an amplifier, the Q point shifts up and down along a line. This line is known as AC load line.

The cutoff point (point C) of AC load line is given by

$$V_{DS(cutoff)}=V_{DSQ}+I_{DQ}R_A$$

Where R_{AC} is the a.c. load resistance.

Saturation point (point D) is given by $I_{D(sat)}= I_{DQ}+(V_{DSQ}/R_{AC})$

If we join cutoff (point C) and saturation poin t(point D, we get the AC load line.

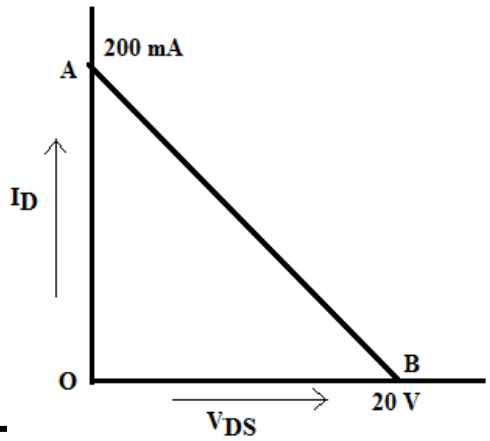
The slope of AC load line is given by

$$Y=-1/R_{AC}$$

.As seen in Figure 3.10 (c) maximum possible positive output voltage signal swing is $I_{DQ}R_{AC}$, while maximum possible negative signal swing is V_{DSQ}.So the peak signal capacity is limited to $I_{DQ}R_{AC}$ or V_{DSQ} whichever is smaller. Fig. b shows that dc and ac load lines intersect at the q point determined by biasing d.c. voltages and currents.a.c. load line is however steeper than dc load line.

Example 3.4. Draw the DC loadline for an N channel JFET which has drain supply voltage V_{DD} = 20 V, R_D=100 Ω.

Solution To draw DC loadline, We require two end points, Cut off point(max V_{DS}) and saturation point (max I_D).



(i) For cutoff point B,when I_D=0, then V_{DS}=V_{DD} Hence max V_{DS} = 20 V

(ii) For saturation point A When V_{DS}=0, then I_D=V_{DD}/R_D

Hence max I_D =20V/100Ω= .2 A or 200 mA

3.6 JFET amplifier:

Figure 3.11 shows the circuit diagram of JFET amplifier circuit. Input signal is applied between gate and source and amplified output is obtained in the drain source circuit. It is necessary to make input circuit reverse biased for the proper functioning of JFET as an amplifier. It is achieved by either inserting a battery V_{GG} in gate circuit or by using any of the biasing circuit discussed earlier.

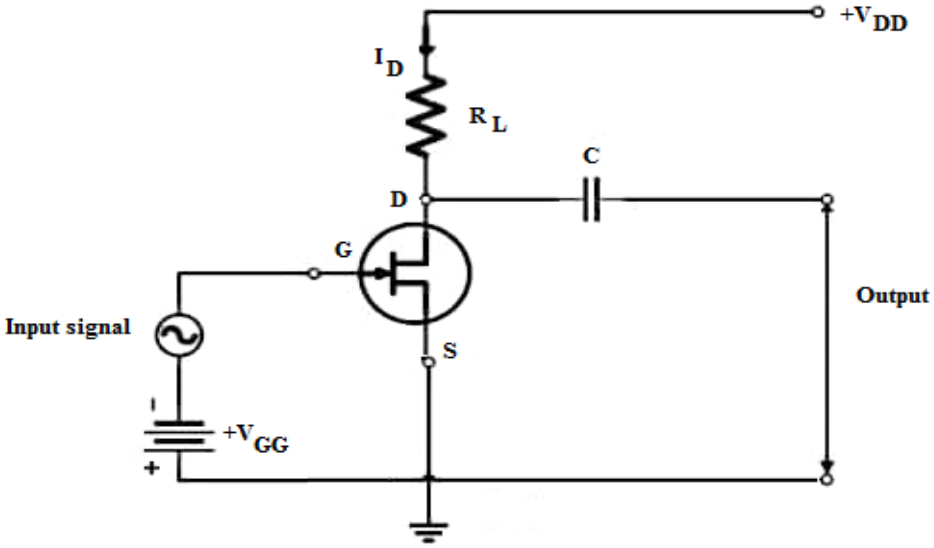


Figure 3.11 circuit diagram of JFET as an amplifier

Now a small change in the reverse bias on the gate produces comparatively large change in drain current. It makes JFET capable to amplify the strength of weak signal. During the positive half of

the signal, reverse bias on the gate decreases. This increases the channel width and hence the drain current also increases. On the other way during the negative half cycle of the signal, the reverse voltage on the gate increases. Consequently, the channel width as well as drain current decreases. We see that a small change in voltage at the gate produces a large change in drain current. these large variations in drain current produce a large output across the load R_L.In this way JFET acts as an amplifier. Also since an increase of gate voltage causes a decrease in the drain voltage,180^0 phase difference exists between the input signal at the gate and the output signal at the drain.

3.7 Advantages and applications of JFET

3.7.1 Advantages of junction field effect transistor JFET is a voltage controlled constant current device like pantode valve. It has a very high input impedance which permits high degree of isolation between input and output circuits i.e. lesser loading effect. It has negative temperature coefficient of resistance which avoids the risk of thermal Runaway. it has a very high power gain this eliminates the necessity of using driver stages. It also has the advantage of smaller size, easier fabrication, longer life, lesser noise and high efficiency.

However disadvantages of JFET are relatively small gain bandwidth product, lesser voltage gain because of smaller transconductance, higher cost and greater susceptibility to damage in handling in comparison to BJT.

3.7.2 Applications of junction field effect transistor

The high input impedance and low noise level, lesser loading effect make JFET far superior to the bipolar transistor and make it ideal device for use in every application in which transistors can be used.

1. Because of their high input impedance JFET are widely used as input amplifiers in oscilloscopes, and other measuring and testing equipments.
2. They are used in RF amplifiers in FM tuners, mixer circuits in FM and TV receivers and other communication equipments because of their low noise level and intermodulation distortion.
3. They are used as voltage variable resistors (VVR) in operational amplifiers and tone controller etc. as it is a voltage controlled device.

4. Because of their very small size, they are widely used in digital circuits in computers, LSI and memory circuits.
5. They are also used in low frequency amplifiers in hearing aids and inductive transducers, buffer amplifier, analog switch, current limiter etc. are some other important applications of JFET.

3.8 Metal oxide semiconductor FET (MOSFET) or Insulated gate FET (IGFET)

Metal oxide semiconductor FET (MOSFET) also known as Insulated gate FET (IGFET) is another important member of JFET family. It is also a semiconductor device like JFET having three terminals a Gate, Drain and Source available in both P-channel(PMOS) and N-channel(NMOS)type. However The main difference between JFET and MOSFET is that unlike P-N junction gate in JFET in MOSFET a metal gate electrode is separated from the semiconductor N-channelor P-channelby an insulating thin layer of silicon dioxide.

In JFET, for the proper functioning of JFET the gate of a JFET must be reverse-biased thus N-channelJFET can only have negative gate operation and P-channelJFET can only have positive gate operation, Such operation is called depletion mode as it depletes (the width biased in such a way so that the pn-junction is. However in MOSFET as the gate is insulated from channel hence such limitations is not required therefore it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve). So MOSFET are basically of two types.

1. Depletion Type
2. Enhancement Type

3.8.1 Depletion and enhancement mode

Depletion Type – When the gate is reverse biased and depletes (reduces) the channel width as well as the conductivity of channel is called depletion mode. In the depletion mode construction ,a channel is physically constructed between the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device “OFF”. The depletion mode- MOSFET is equivalent to a “Normally Closed” switch.

Enhancement Type – When the gate is biased such that it enhances (increases) the channel width as well as the conductivity of channel is called depletion mode.

the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode- MOSFET is equivalent to a "Normally Open" switch.

3.9 The Depletion MOSFET (DE-MOSFET)

3.9.1 Construction and symbol of DE-MOSFET

Figure 3.12 (a) shows the constructional detail of N-channelDE-MOSFET. It consists of a lightly doped N type semiconductor are diffused forming the source and drain of MOSFET. An N-channelis diffused between the source and drain. The type of impurity for the channel is same as for the source and drain.

For the construction of gate a thin layer of metal oxide (SiO_2)is deposition over a small portion of the channel small portion of the channel. A metallic gate(e.g. Al) is deposited over the SiO_2 layer. As SiO_2 is an insulator, therefore the gate is insulated from the channel. The metallic gate, semiconductor substrate and insulating SiO_2 layer form a parallel plate capacitor.

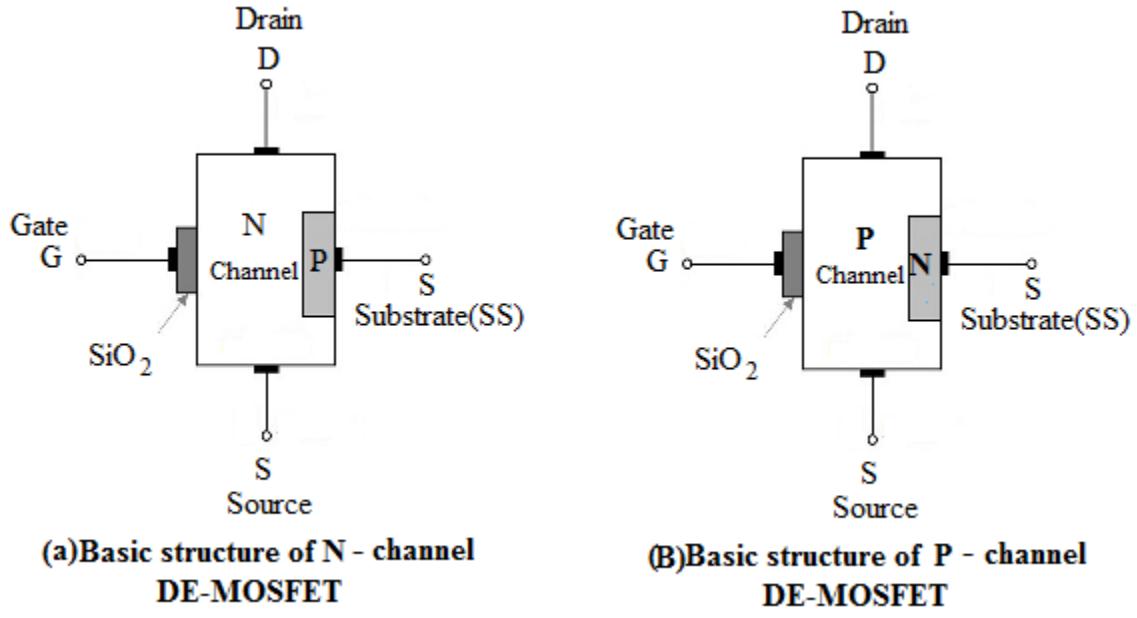


Figure 3.12 Basic structure of DE-MOSFET

Similarly for P-channelMOSFET a lightly doped N type substrate ,two heavily doped P region are formed at the two ends by the diffusion techniques to serve as source and drain and a P-channelwith insulated make gate (Figure 3.12(b)).

Figure 3.13 shows the schematic symbol of N-channeland P-channelDE- MOSFET. The thin vertical line just right to the gate terminal represents the channel. In N-channelDE-MOSFET the arrow is on the substrate and points towards the N-channel(Figure 3.13 (a))..Some MOSFET have four terminal for added control of drain current so a connection from the substrate is also taken out (Figure 3.13 (a) i) ,but in most of the MOSFET's the substrate is internally connected to the source by the manufacturer resulting to three terminal device (Figure 3.13 (a) ii).

In P-channelMOSFET arrowhead direction on the substrate is outwards from P-channel(Figure 3.13 (b)).

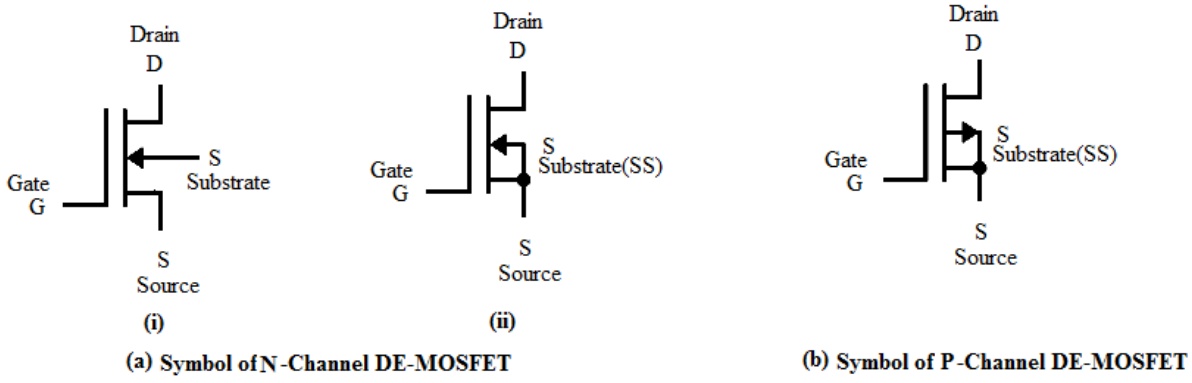


Figure 3.13 Symbol of DE-MOSFET

3.9.2 Circuit operation of DE- MOSFET: Figure 3.14 shows the depletion and enhancement mode in DE-MOSFET. The main drawback of JFET is that the gate must be reverse biased for proper functioning of the device, means by increasing the reverse bias we can only decrease the conductivity (i.e. increase the resistance of channel)from its zero bias. This type of operation is referred to depletion mode operation. So we can say JFET can only be operated in depletion mode operation.

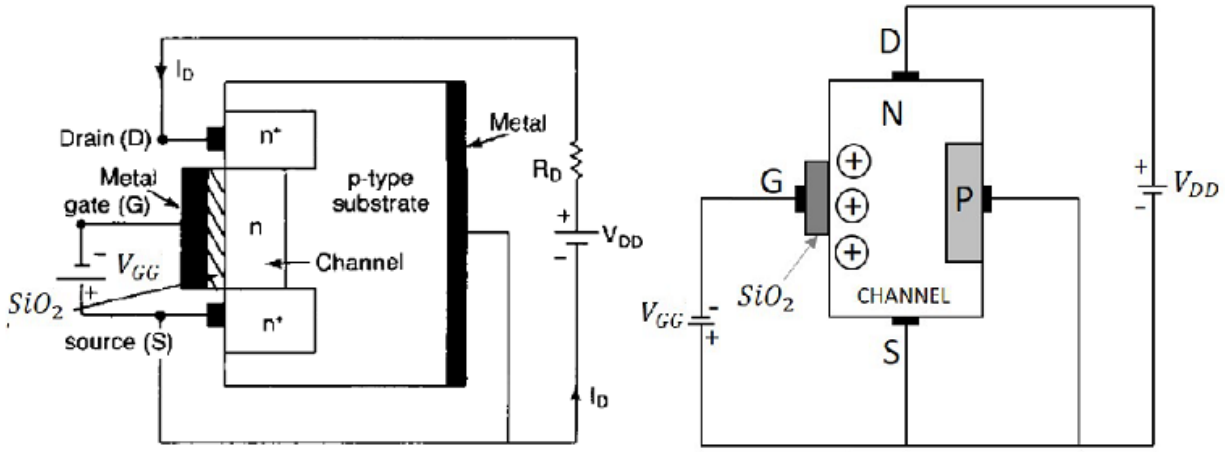
However MOSFET can be operated by the positive bias gate also means it enhance the conductivity of the channel, this is called Enhancement mode.

Circuit of N-channelDE-MOSFET

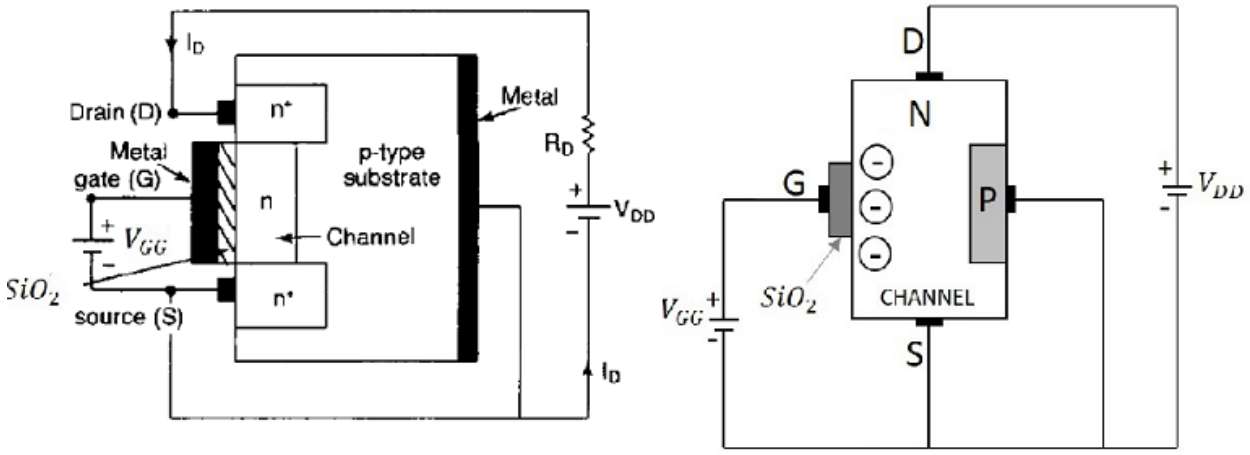
As discussed earlier in DE-MOSFET the gate is insulated from the channel, we can apply either negative or positive voltage to the gate, the negative gate operation is called depletion mode whereas positive gate operation is called enhancement mode.

Depletion mode In depletion mode the gate is negative with respect to source. Electron on gate repel the free electron in the N-channelleaving a layer of positive ions in a part of channel

(Figure 3.14(a)). In other way we can say due to capacitive action of MOSFET negatively charge gate induces the +ve charge on N-channel. So negative biased gate depletes (reduced) the electrons of N-channelhence termed as depletion mode. Therefore lesser number of free electrons are made available for current conduction through the N-channelis reduced or resistance of the channel is increased.The greater negative voltage applied to the gate causes the lesser current from source to drain.



(a) Depletion mode operation



(b) Enhancement mode operation

Figure 3.14 Working of DE-MOSFET

Thus by varying the negative voltage on the gate we can vary the resistance of the N-channelhence the current from source to drain. With negative voltage to the gate of N-channelMOSFET, the action of DE-MOSFET is same as JFET,

Enhancement mode: On the other hand when the gate is made positive with respect to source, a drain current will flow and the MOSFET is said to be operating in Enhancement mode. In this

mode of operation Gate attracts the negative charge carriers from the P substrate to the N-channeland thus the channel resistances reduces and drain current increases with increased positive potential in Gate (Figure 3.14(b)).

Thus by changing the positive voltage on the gate, we can change the conductivity of the channel.

3.10 Characteristics of depletion type MOSFET:

3.10.1 Drain characteristics of depletion type MOSFET: Figure 3.15 shows a set of drain characteristics for the N-channel DE-MOSFET. If we compare these curve with JFET drain characteristics curve we find that they are similar in nature except that DE- MOSFET can operate for both negative and positive gate voltages unlike JFET which operates only for negative gate voltage,

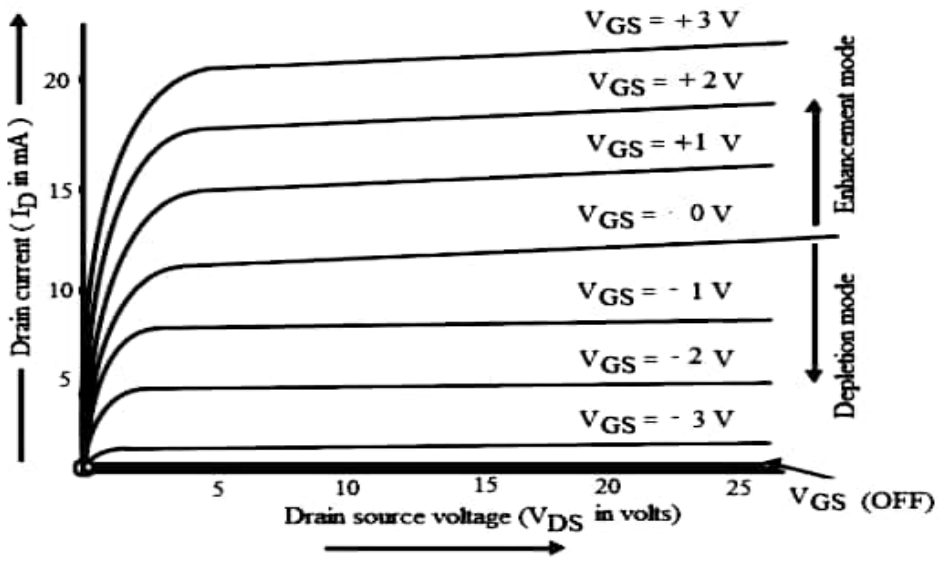


Figure 3.15 Drain characteristics of DE-MOSFET

It is clearly seen that N-channelMOSFET may be operated in either enhancement mode or the depletion mode .The enhancement mode occurs for positive values of V_{GS} while the depletion mode occurs for negative values of V_{GS} .Like JFET these drain curve again display an ohmic region, a constant current source region. MOSFET has two major applications, as a constant current source and as a voltage variable resister.

3.10.2 Transfer characteristics of depletion type MOSFET: Figure 3.16 shows the transfer or transconductance characteristic curve for the N-channelDE-MOSFET.The transfer characteristics give the variations of the drain current I_D with the gate to source voltage V_{GS} for a fixed value of V_{DS}.

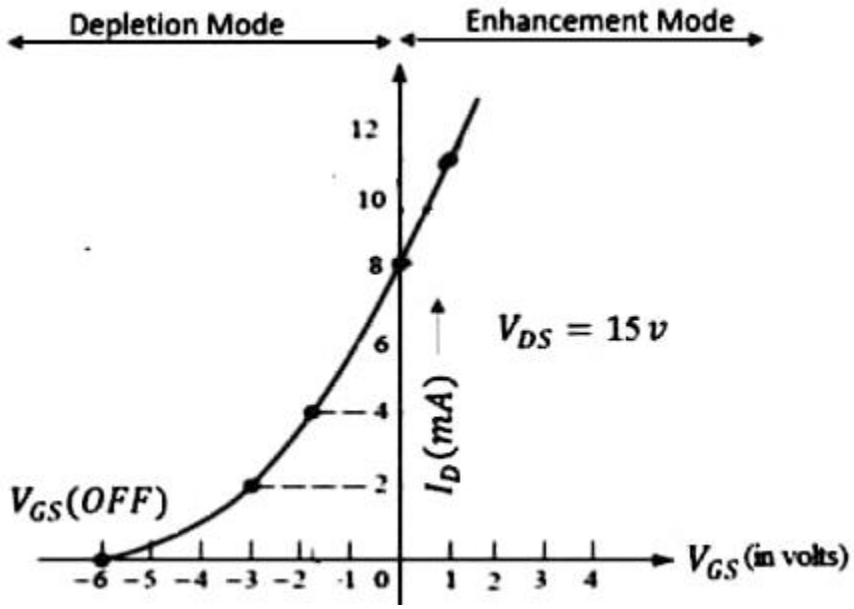


Figure 3.16 Transfer characteristic of DE-MOSFET

Again the curve is similar to that of transfer curve of JFET in the depletion region, but here the curve extends for the positive values of gate to source voltage also. The value IDSS represents the current from drain to source with V_{GS}=0.But even here the same basic formula used to determine the drain current at any point along the transfer characteristic i.e.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

The enhancement mode- MOSFET is equivalent to a “Normally Open” switch.

Example 3.5. For a certain DE-MOSFET,I_{DSS}=5 mA and $V_{GS(off)}$ = -6V.

(i)Is this an N-channelor a P-channelD-MOSFET?

(ii) Calculate I_D at V_{GS} = -3V.

(iii) Calculate I_D at V_{GS} = +3V

Solution: (i) Given $V_{GS(off)}$ = -8Vi,e.the device has a negative $V_{GS(off)}$,therefore it is N-channelDE-MOSFET.

(ii)$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = 5\ \left(1 - \frac{-3}{-6}\right)^2 = \frac{5}{4} = 1.25\ mA$

(iii) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = 5\ \left(1 - \frac{+3}{-6}\right)^2 = \frac{45}{4} = 11.25\ mA$

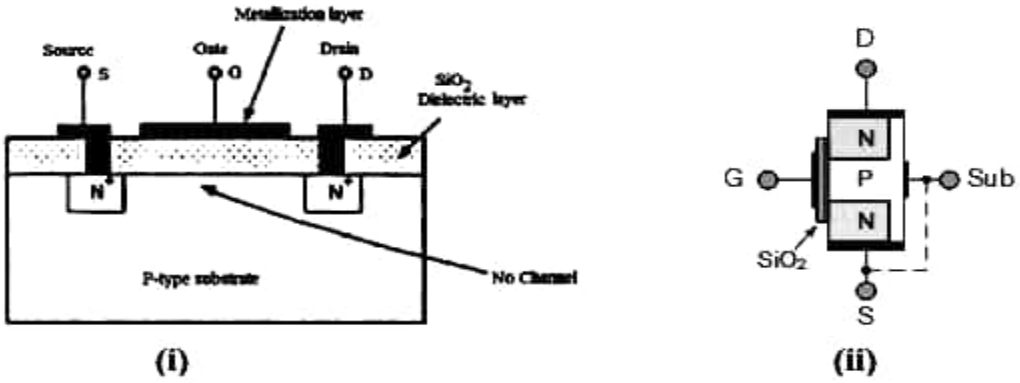
Ans. (i) $\mathrm{N-channel\ DE-MOSFET.}$ $(ii)\ I_D = 1.25\ mA$ (iii) $I_D = 11.25\ mA$

3.11 The ENHANCEMENT- ONLY MOSFETs (E –MOSFET)

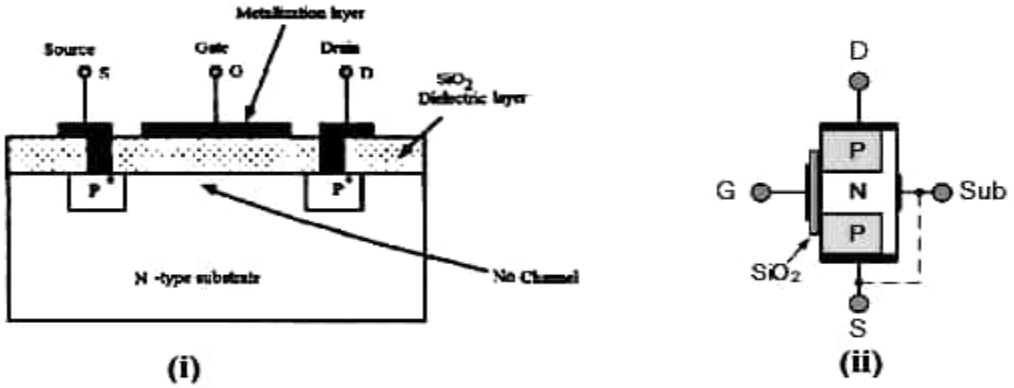
As the name signifies that E-MOSFET operates only in the enhancement mode and has no depletion mode , also It has no physical channel. The evolution of E-MOSFET has become very important in digital electronics and computers.

3.11.1 Construction and symbol of E-MOSFET

Figure 3.17(a) shows the constructional detail of N-channelE-MOSFET. Unlike DE-MOSFET here the lightly doped P type substrate extends all the way to the silicon dioxide (SiO_2) and no channels are doped between the source and the drain (both source and drain are made by two highly doped N regions diffused in the substrate).Channels are electrically induced in these MOSFET's when a positive gate-source voltage V_{GS} is applied to it. An insulating very thin layer of SiO_2 is deposited over SiO_2 , which serves the purpose of gate.



(a) Basic structure of N-channel MOSFET



(b) Basic structure of P-channel MOSFET

Figure 3.17 basic structure of E-MOSFET

Similarly for P-channelMOSFET a lightly doped N type substrate ,two heavily doped P region are formed at the two ends by the diffusion techniques to serve as source and drain . (Figure 3.17(b))

Figure 3.18 shows the schematic symbol of N-channeland P-channelE- MOSFET.

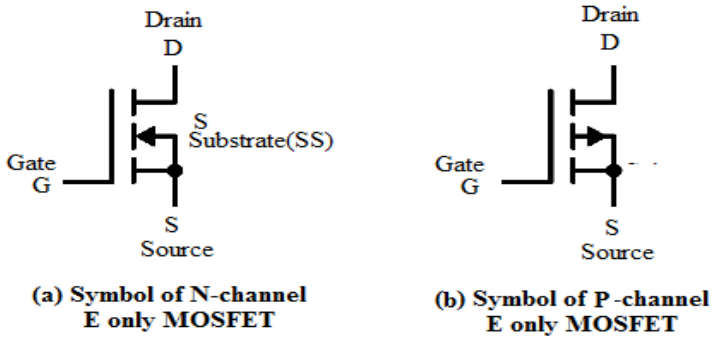


Figure 3.18 Symbol of E-MOSFET

In the figure the broken lines indicates that there is no conducting channel between drain and source. The arrow is on the substrate and points in the direction of channel which is created when the gate source voltage is increased above threshold voltage. In N-channelMOSFET arrowhead direction is inward direction and in P-channelarrow head is reversed i.e. in outward direction.

3.11.2 Circuit operation of E- MOSFET: Figure 3.19 shows the normal biasing polarities of N-channelE-MOSFET. It operates with large positive gate voltages only. When the gate to source voltage is zero, the positive drain voltage VDD force free electrons to move from source to drain but as no channel exists , substrate P type material restricts the electron to pass through it. Thus there is no drain current for VGS=0.Due to this region, the enhancement type MOSFET is also called normally-OFF MOSFET.

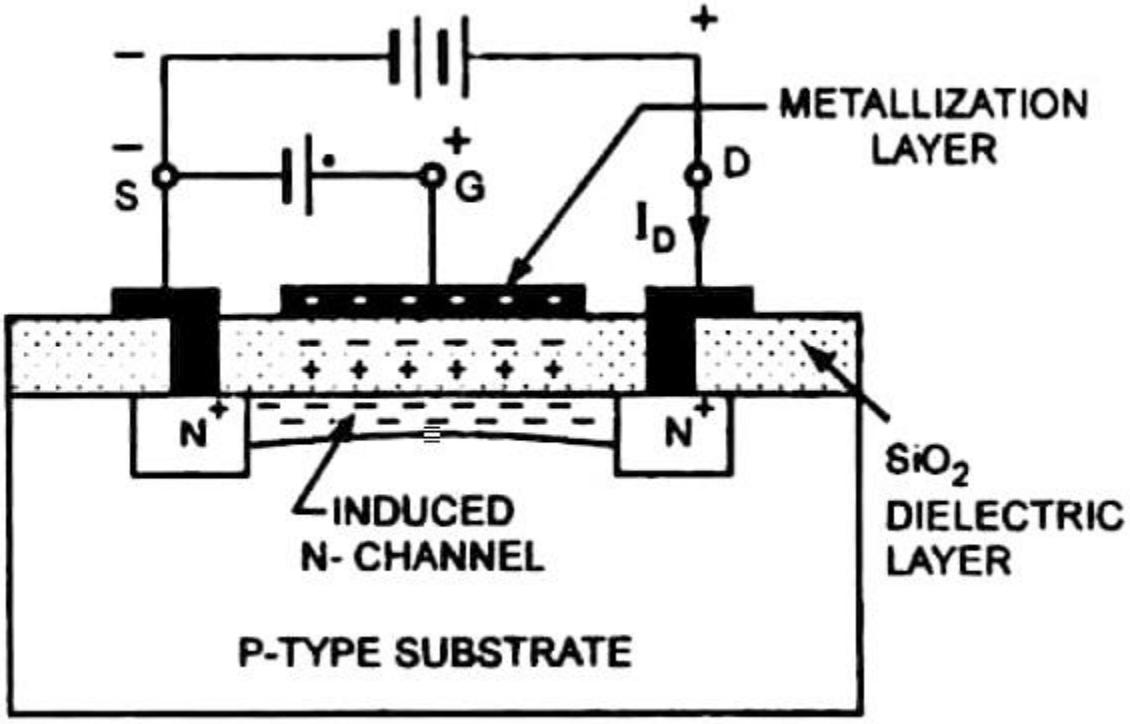


Figure 3.19 Biasing polarities of N channel E-MOSFET

When drain is applied with +ve voltage with respect to source and some positive potential is applied to gate, negative charge carriers within the substrate are attracted towards the positive

gate and accumulate close to the surface of substrate. As the gate voltage is increased, more and more electrons accumulate near th the gate. Since these electrons cannot flow across insulated layer of SiO2 to the gate,they accumulate at the surface os substrate just adjacent to SiO2 layer and form a N type channel (inversion layer) stretching from drain to source. And a drain current starts flowing. The minimum value of VGS which produces inversion layer is called threshold voltage (V_{GS}(th)).

The strength of the drain current depends upon the channel resistance, which in turn depends on the number of charge carriers attracted towards positive gate. Thus drain current is controlled by the gate potential. It can never operate with negative gate voltages.

3.12 Characteristics of enhancement type MOSFET:

3.12.1 Drain characteristics of enhancement type MOSFET: Figure 3.20 shows a set of drain characteristics for the N-channel E-MOSFET. It is clearly seen that almost no drain current flows unless the gate to source voltage (VGS) is less then threshold voltage.

However a small current does flow through the MOSFET below threshold voltage, due to presence of thermally generated electrons in the P type substrate. When the value of gate to source voltage (V_{GS}) kept above threshold voltage (V_{GS}(th)),a significant drain current flows.

An increase in positive gate voltage above the threshold voltage induces more electrons to the channel and drain current increases while channel resistance decreases.

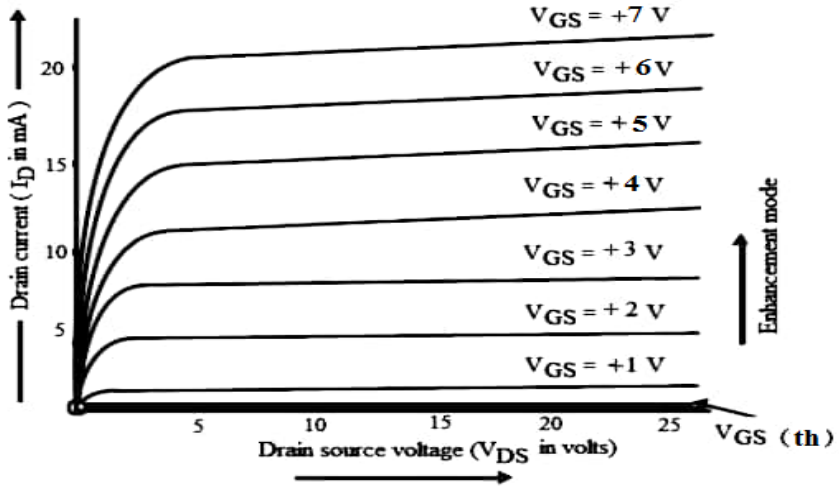
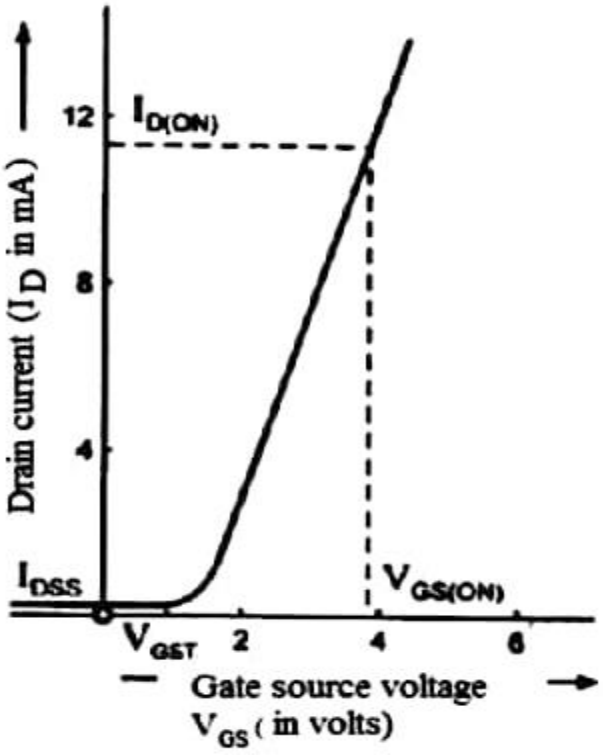


Figure 3.20 Drain characteristics of N channel E-MOSFET

The characteristics curves have almost vertical (Ohmic region) and almost horizontal parts(Constant current region).Thus E-MOSFET can be operated in either of these region i.e. it can be used as a variable voltage resistor(VVR) in ohmic region or as a constant current source in horizontal parts of characteristics.

3.12.2 Transfer characteristics of enhancement type MOSFET: Figure 3.21 shows the transfer or transconductance characteristic curve for the N-channelE-MOSFET. The transfer characteristics give the variations of the drain current I_D with the gate to source voltage V_{GS} for a fixed value of V_{DS}. The current I_{DSS} at $V_{GS} \leq 0$ is almost zero. When the V_{GS} is increased above threshold voltage the drain current increases slowly at first and then rapidly.



. **Figure 3.21 Transfer characteristics of N channel E-MOSFET**

The drain current at any point along the transfer characteristic is given by

$$I_D = K\left(V_{GS} - V_{GS(th)}\right)^2$$

Where K is a constant which is a property of device construction. Unlike DE-MOSFET or JFET in E-MOSFET ,I_{DSS} is not associated with formula as no drain current flows with V_{GS}=0 volt. 5.

Example 3.6. For an E-MOSFET, given $V_{DD} = 20\ V$, R_D=400 Ω, $I_{D(on)}$=96 mA at V_{GS}= 5 V and $V_{GS(th)}$ =1V.Determine the drain current and drain source voltage for V_{GS}=3V.

Solution

The drain current at any point along the transfer characteristic is given by

$$I_D = K\left(V_{GS} - V_{GS(th)}\right)^2$$

$$96 = K(5-1)^2 \quad Hence\ K = 6\ mA/V^2$$

Now Value of drain current for V_{GS}=3V is

$$I_D = K\left(V_{GS} - V_{GS(th)}\right)^2 = 6(3-1)^2 = 24\ mA$$

And Value of drain source voltage for V_{GS}=3V

$V_{DS} = V_{DD} - I_D R_D = 20\ -\ (24\text{mA})(400\Omega) = 10.4\ \text{V}$

Ans. $\boldsymbol{I_D}$ **=24 mA,** $\boldsymbol{V_{DS} = 10.4\ V}$

3.13 MOSFET amplifier

Like JFET, MOSFET can also be used as an amplifier. Figure 3.22(a) shows the common source N channel DE-MOSFET amplifier.DE-MOSFET can be operated either with positive or negative gate, so its operating point can be set at V_{GS}=0V (Figure 3.22 (b))The gate is at ground potential for DC and the source terminal is grounded, thus making V_{GS}= 0 V. The input signal is capacitively coupled to the gate terminal. When signal C_{in} is applied,V_{gs} varies above and below V_{GS}=0V i.e. Q point, producing a a change in drain current I_D and drain voltage V_{out}.

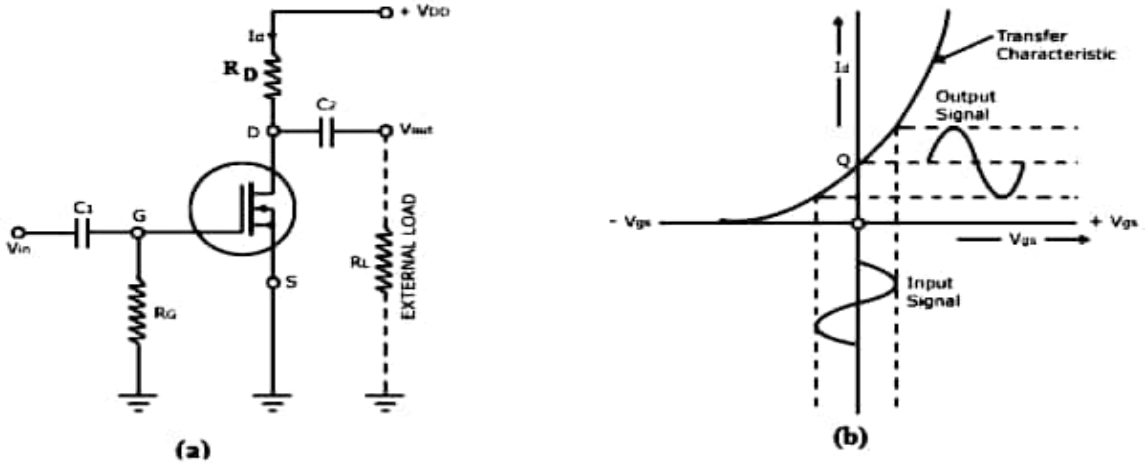


Figure 3.22 Common source N channel DE-MOSFET amplifier

A small change in gate voltage produces a large change in the drain current .During the positive half of input signal DE-MOSFET is in enhancement mode and increases drain current, while during the –ve half of input signal DE-MOSFET is in depletion mode and drain current decreases. This large variation in drain current produces a large AC output voltage across the resistance R_D. In this way DE-MOSFET acts as an amplifier. Figure 3.22(b) shows the amplifying action of DE-MOSFET on transfer curve.

Figure 3.23 (a) shows common source N-channelE-MOSFET amplifier using potential divider bias.

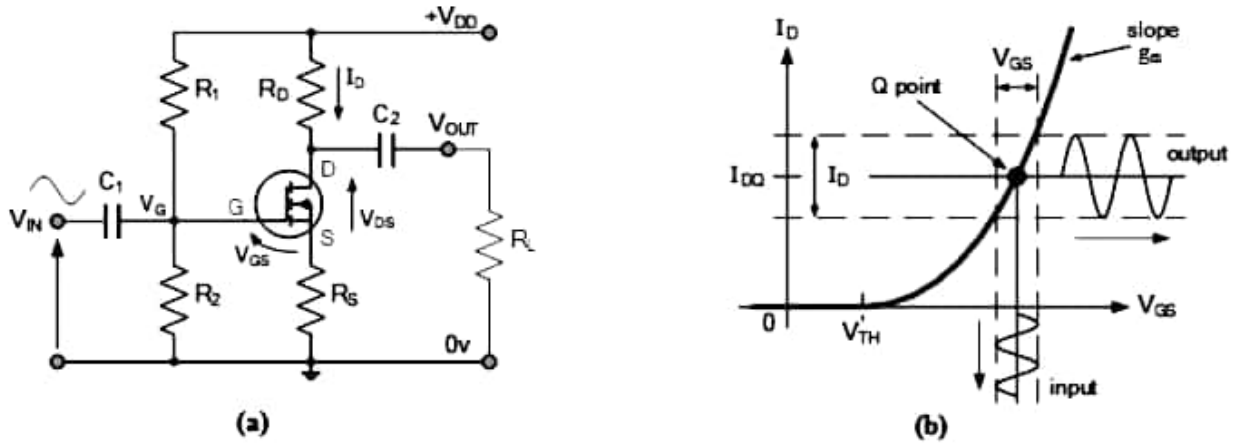


Figure 3.23 Common source N channel E-MOSFET amplifier

AC signal applied to the gate through coupling capacitor C, and the gate is biased with a positive voltage such that $V_{GS}>V_{GST}$.As illustrated in transfer curve of E-MOSFET ,a change in input signal produces a change in drain current I_D. Thus V_{DS} or V_{OUT} also varies as $V_{DS}=V_{DD}-I_DR_D$ as in JFET or DE-MOSFET circuit.

3.14 Summary

FET is a unipolar, voltage controlled device with high input impedance, negative temperature coefficients, and lower noise. It has three terminals named source, drain and gate with a conducting channel between source and drain . JFET is always operated with reverse biased gate. And drain current is controlled by changing the channel width using electric field or voltage. A small change

in gate source voltage produces a large change in drain current and hence a large voltage variation across load $R_{L,}$ which helps to use it as an amplifier. The curve drawn between drain current and drain to source voltage with constant gate to source voltahe is called drain characteristic while the curve drawn between drain current and gate to source voltage with constant drain to source voltage is called transfer characteristics. Minimum drain source voltage at which the drain current essentially becomes constant is called the pinch off voltage while minimum gate source voltage where the drain current becomes zero is called cutoff voltage. MOSFET is a field effect transistor in which the metal gate is insulated by a very thin oxide layer from the semiconductor channel. They are of two types DE-MOSFET and E-MOSFET.DE-MOSFET works in depletion mode as well as in enhancement mode while E-MOSFET works only in enhancement mode as E-MOSFET has no physical channel from source to drain. It is .only by the application ogf proper gate source voltage the device starts conducting. The minimum value of V_{GS} of proper polarity that turns on the E-MOSFET is called threshold voltage.

3.15 Glossary:

FET: Field effect transistors(FET) are voltage controlled device with high input impedance having 3 terminals, Source, gate and drain.

Shorted-gate drain current(I_{DSS}) or Zero bias current: Drain current when drain voltage is equal to pinch off voltage and V_{GS} =0

Pinch off voltage: Minimum drain source voltage at which the drain current essentially becomes constant.

Cut off voltage: Minimum gate source voltage where the drain current becomes zero.

Depletion mode: When the gate is reverse biased and depletes (reduces) the channel width as well as the conductivity of channel is called depletion mode.

Enhancement mode: When the gate is biased such that it enhances (increases) the channel width as well as the conductivity of channel is called depletion mode.

3.16 Reference books:

1. Principles of electronics by V.K.Mehta
2. Basic Electronics by B.L.Thereja
3. Electrical circuit and basic semiconductor electronics by Dr. J.P.Agarwal

3.17 Suggested readings:

1. Electronic devices and circuits by Jacob Milliman and C.C.Halkais
2. The Feynman Lectures on Physics by Richard Feynman
3. Electronic devices and circuit theory by R.L.Boylestad and Louis N

3.18 Terminal Questions:

3.18.1 Short answer type questions

1. Discuss advantages and disadvantages of FET over BJT?
2. Draw the circuit symbols of different JFET and MOSFET?
3. What do you understand by depletion mode and enhancement mode of MOSFET?
4. Define pinch off voltage of JFET? Differentiate between pinch off and cut off voltage in JFET.
5. What is meant by threshold voltage and drain source saturation current I_{DSS} of JFET.

3.18.2 Long answer type questions

1. Discuss the construction and working of a field effect transistors? Why they are named so? Also discuss the drain characteristic of JFET and effect of pinch off voltage on its depletion region.
2. Discuss different biasing method of JFET and compare them.
3. How a MOSFET differs with JFET? Explain. Discuss different JFET parameters and working of common source JFET amplifier.
4. Discuss the construction, working and characteristic curves of enhancement only MOSFET.
5. Discuss the construction, working and characteristic curves of depletion type MOSFET.

3.18.3 Numerical questions

1. When gate source voltage V_{gs} of a JFET changes from -2V to -1.5 V, the drain current changes from 1.5 mA to 2 V, calculate the value of transconductance? **(Ans. 1 mili mho)**

2. A JFET has a drain current 4 mA. If I_{DSS}=9 mA and $V_{GS(off)}$ = - 5V. Find the value of V_{GS} and V_p. **(Ans. V_{GS}= - 1.67 V and V_p =5 V)**

3. Determine the value of Rs required to self bias a P-channelJFET with I_{DSS}=20 mA,$V_{GS(off)=}$16V and V_{GS}=4 V **(Ans. 26.67 ohm)**

4. For a certain DE-MOSFET,I_{DSS}=10 mA and $V_{GS(off)}$ = -8V.

(i)Is this an N-channelor a P-channelD-MOSFET?

(ii) Calculate I_D at V_{GS} = -2V.

(iii) Calculate I_D at V_{GS} = +2V **(Ans.(ii) I_D=7.5 mA, (iii) I_D=12.5 mA,)**

5. For an E-MOSFET, given $I_{D(on)}$=500 mA at V_{GS}= 10 V and $V_{GS(th)}$ =1V.Determine the drain current for V_{GS}=5V. **(Ans. I_D=98.7 mA)**

UNIT-4: OPERATIONAL AMPLIFIER

Contents

4.1. Objectives

After finishing this chapter students will be able to know

- The Operational Amplifier
- Requirement of this electronic device
- Pin diagram of 741Op-Amp.

- Various applications of Op-Amp

4.2 INTRODUCTION

An operational amplifier, or Op-Amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, fiber circuits and many types of instrumentation circuits. An Op-Amp contains a number of differential amplifier stages to achieve a very high voltage gain.

Figure 4.1 shows a basic Op-Amp with two inputs and one output as would result using a differential amplifier input stage. Each input result in either the same or an opposite polarity (or phase) output, depending on whether the signal is applied to the plus (+) or the minus (-) input.

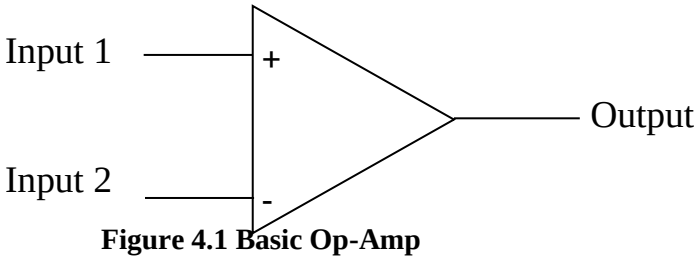
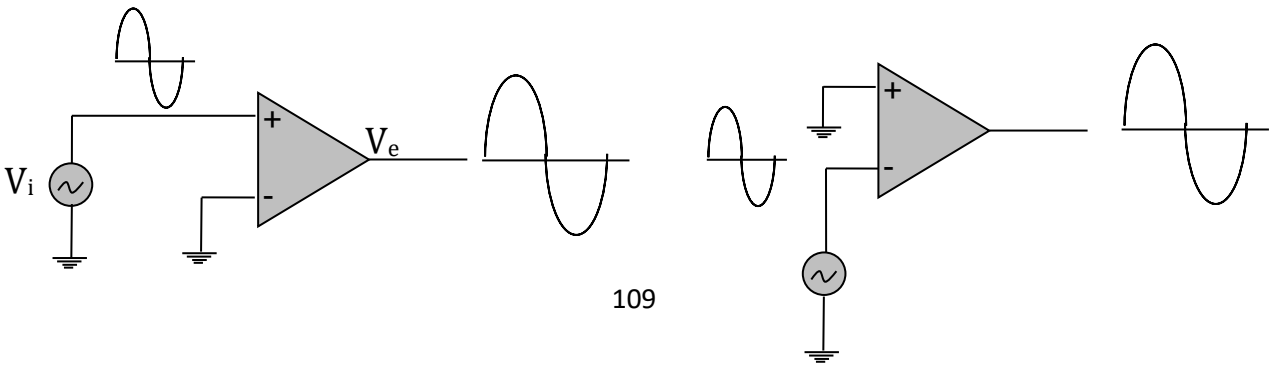


Figure 4.1 Basic Op-Amp

4.2.1Single-Ended Input

Single-ended input operation results when the input signal is connected to one input with the other input connected to ground. Figure 4.2 shows the signals connected



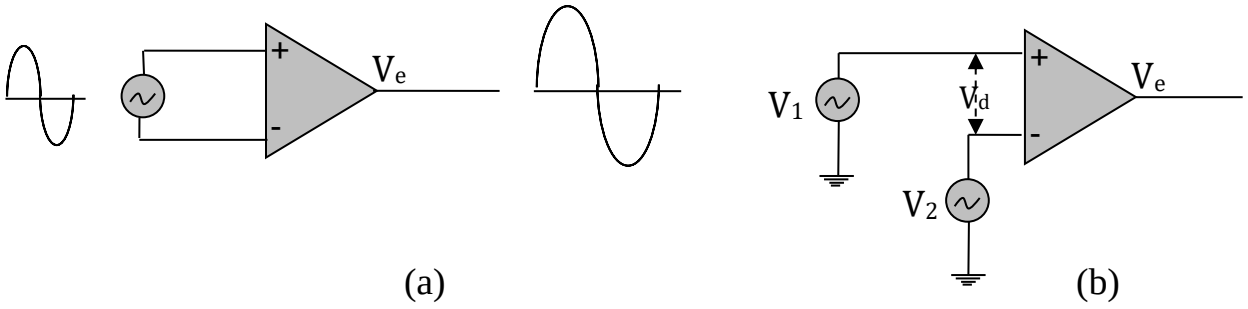
(a) (b)

F ended operations.

for this operation. In Fig. 4.2a, the input is applied to the plus input (with minus input at ground), which results in an output having the same polarity as the applied input signal. Figure 4.2b shows an input signal applied to the minus input, the output then being opposite in phase to the applied signal.

4.2.2 Double-Ended (Differential) Input

In addition to using only one input, it is possible to apply signals at each input-this being a double-ended operation. Figure 4.3a shows an input, V_d, applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs. Figure 4.3b shows the same action resulting when two separate signals are applied to the inputs, the difference signal being $V_{i_1} - V_{i_2}$.



(a) (b)

Figure 4.3 Double-ended (differential) operation.

4.2.3 Double-Ended Output

While the operation discussed so far had a single output, the Op-Amp can also be operated with opposite outputs, as Shown in Fig. 4.4. An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity. Figure 4.5 shows a single-ended input with a double-ended output. As

shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. Figure 4.6 shows the same operation with a single output measured

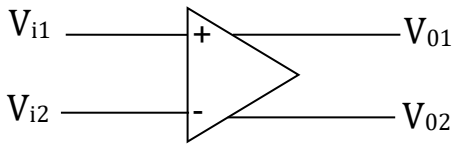


Figure 4.4 Double-ended output

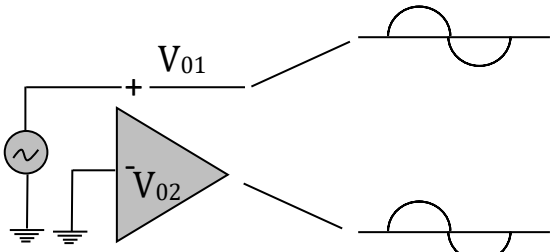


Figure 4.5 Double-ended output with single-ended input

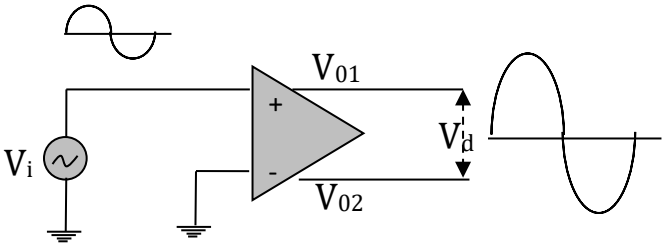


Figure 4.6 Double-ended output

between output terminals (not with to ground). This difference output signal is $V_{O_1} - V_{O_2}$. The difference output is also referred to as a *floating signal* since neither output terminal is the ground (reference) terminal. Notice that the difference output is twice as large as either $V_{O_1} or\ V_{O_2}$ since they are of opposite polarity and subtracting them results in twice their amplitude [i.e., 10 V - (-10V) = 20 V]. Figure 4.7 shows a differential input, differential output operation. The input is applied between the two input terminals and the output taken from between the two output terminals. This is fully differential operation.

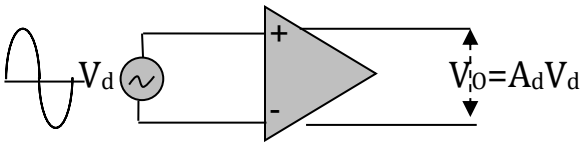


Figure 4.7 Differential-input, differential-output operation.

4.2.4 Common-Mode Operation

When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. 4.8. Ideally, the two inputs are equally amplified, and since they result in opposite polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

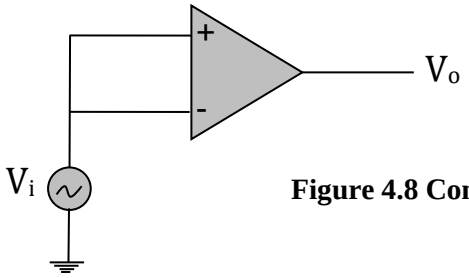


Figure 4.8 Common-mode operation.

4.2.5 Common-Mode Rejection

A significant feature of a differential connection is that the signals which are opposite at the inputs are highly amplified, while those which are common to the two inputs are only slightly amplified-the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs. Since noise (any unwanted input signal) is generally common to both inputs, the differential connection tends to provide attenuation of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature, referred to as common-mode rejection, is discussed more fully in the next section.

4.2.6 DIFFERNTIAL AND COMMON-MODE OPERATION

One of the more important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs, while only slightly amplifying signals that are common to both inputs. An

It should be clear that the desired operation will have A_d very large with A_c very small. That is, the signal components of opposite polarity will appera greatly amplified at the output, whereas the signal components that are in phase will mostly cancel out so that the common-mode gain, A_c, is very small. Ideally, the value of the

CMRR is infinite. Practically, the larger the value of CMRR, the better the circuit operation.

We can express the output voltage in terms of the value of CMRR as follows:

$Eq.(13.3): V_o = A_d V_d + A_c V_c = A_d V_d \left(1 + \frac{A_c V_c}{A_d V_d}\right)$

Using Eq. (13.4), we can write the above as

$$V_o = A_d V_d \left(1 + \frac{1}{CMRR}\frac{V_c}{V_d}\right) \quad (1)$$

Even when both V_d and V_c components of signal are present, Eq. (13.6) shows that for large values of CMRR, the output voltage will be due monthly to the difference signal, with the common-mode component greatly reduced or rejected. Some practical examples should help clarify this idea.

4.2.7 Virtual Ground

The output voltage is limited by the supply voltage of, typically, a few volts. A stated before, voltage gains are very high. If, for example, $V_o = -10V$ and $A_v = 20{,}000$, the input voltage would then be

$$V_i = \frac{-V_o}{A_c} = \frac{10\ V}{20{,}000} = 0.5\ mV$$

If the circuit has an overall gain (V_o/V_1) of, say, I, the value of V_1 would then be 10 V. Compared to all other input and output voltages, the value of V_i is then small and may be considered 0 V.

Note that although $V_i \approx 0$ V, it is not exactly 0 V. (The output voltage is a few volts due to the very small input V_i times a very large gain A_v.) The fact that $V_i \approx 0V$ leads to the concept that at the amplifier input there exists a virtual short circuit or virtual ground.

The concept of a virtual short implies that although the voltage is nearly $0V$, there is no current through the amplifier input to ground. Figure 13.14 depicts the virtual ground concept. The heavy line is used to indicate that we may consider that a short

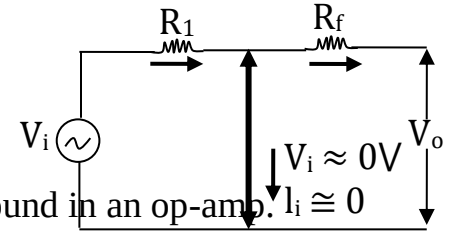


Figure 4.9 Virtual ground in an op-amp.

exists with $V_i \approx 0V$ but that this is a virtual short so that no current goes through the short to ground. Current goes only through resistors R_1 and R_f as shown.

Using the virtual ground concept, we can write equations for the current I as follows:

$$I = \frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

which can be solved for V_o/V_1:

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

The virtual ground concept, which depends on A, being very large, allowed a simple solution to determine the overall voltage gain. It should be understood that

although the circuit of Fig. 4.9 is not physically correct, it does allow an easy means for determining the overall voltage gain.

Special points: Why Operational Amplifier? BJT, JFET and MOSFET can amplify only AC not DC but Operational amplifier can amplify both AC as well as DC.

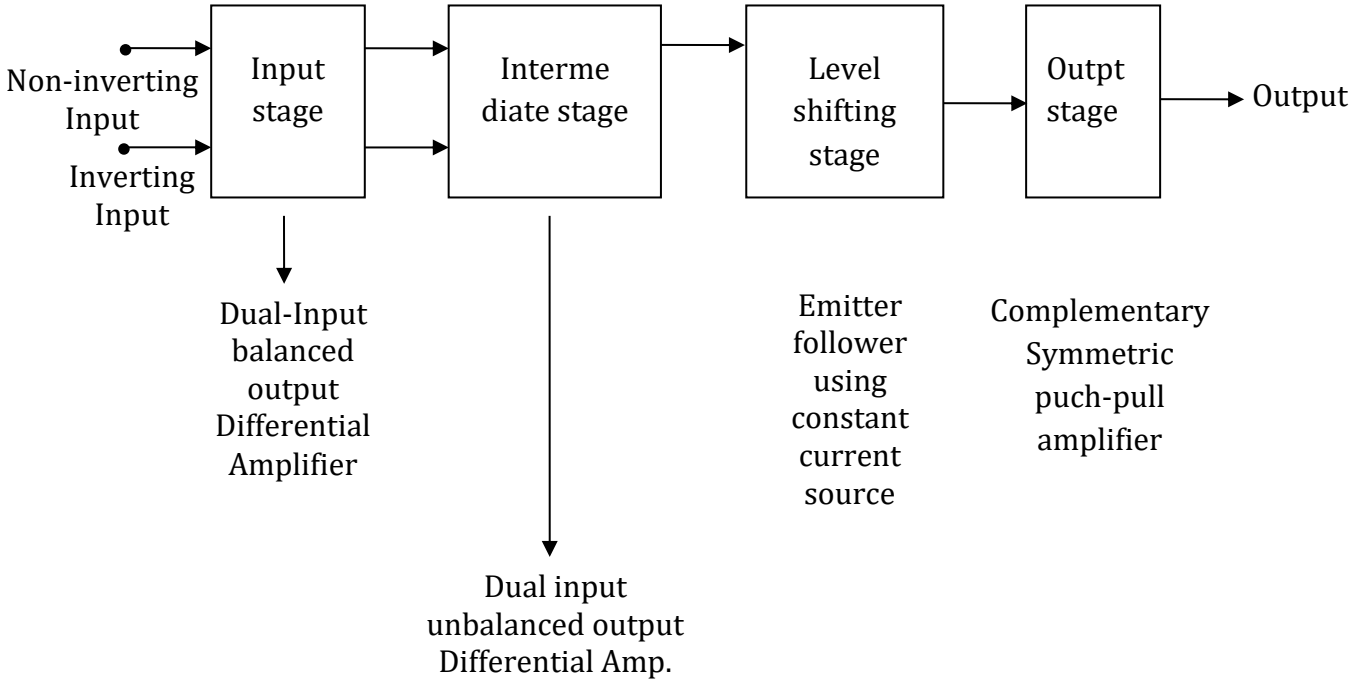
Why the name Operational Amplifier? This was used to perform some mathematical operations like integrate, subtract, division logarithmic etc...

4.3 More concepts on Operational Amplifiers

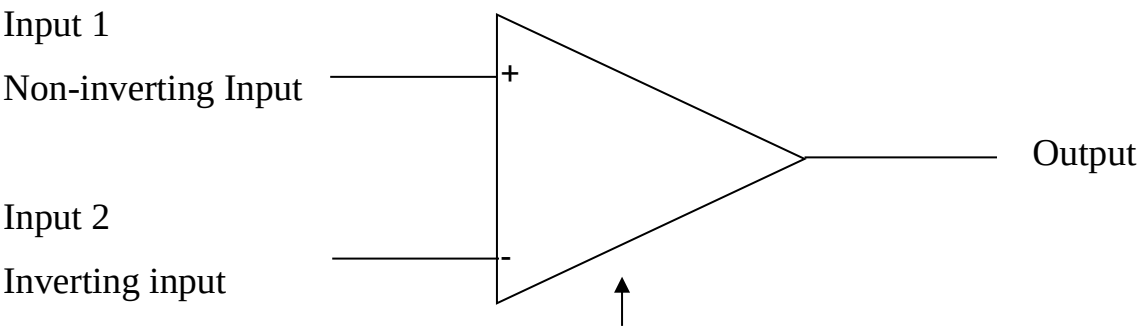
An operational amplifier is a direct coupled high gain amplifier usually consisting of one or more differential amplifiers & usually followed by a level translators and an output stage of push-pull or push-pull complementary symmetry pair.

- It is a versatile as a single integrated circuit package.
- It is a versatile device used to amplify DC as well as AC input signals.
- It was originally designed for performing mathematical operations such as addition, subtraction, multiplication, differentiation & integration.
- Applications:
    1. AC & DC signal amplification
    2. Actives filters
    3. Oscillators
    4. Comparators
    5. Regulators

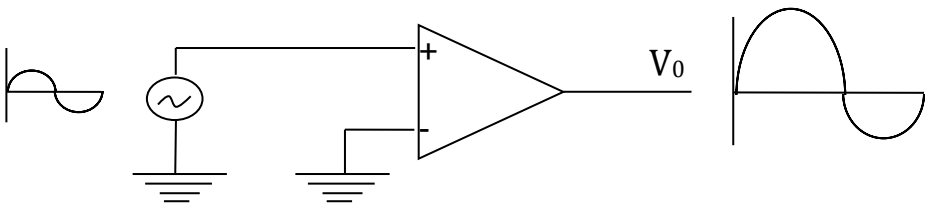
4.3.1Block Diagram of Op-Amp: Block diagram of Op-Amp consists of four stages shown below



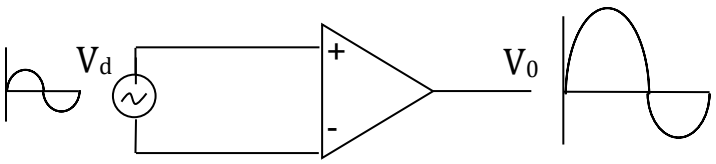
4.3.2 Op-Amp and its various working connections



Basic Op-Amp

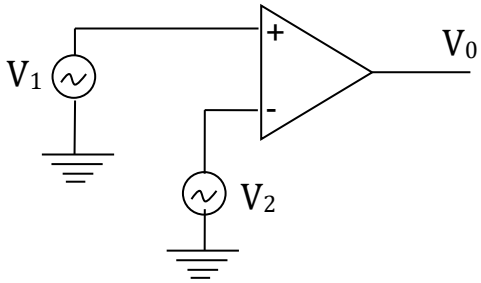


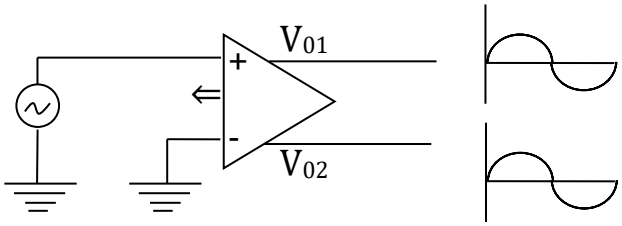
Single - ended operations



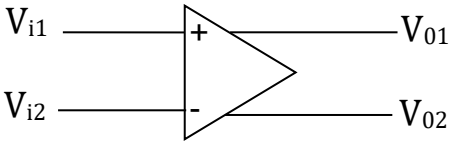
Double-ended (difference) operation

Or

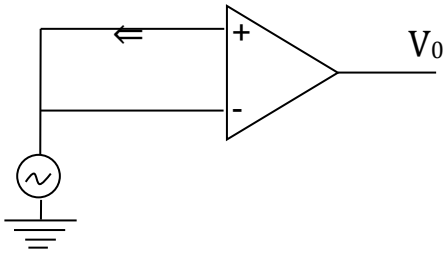




Double-ended output with single-ended input

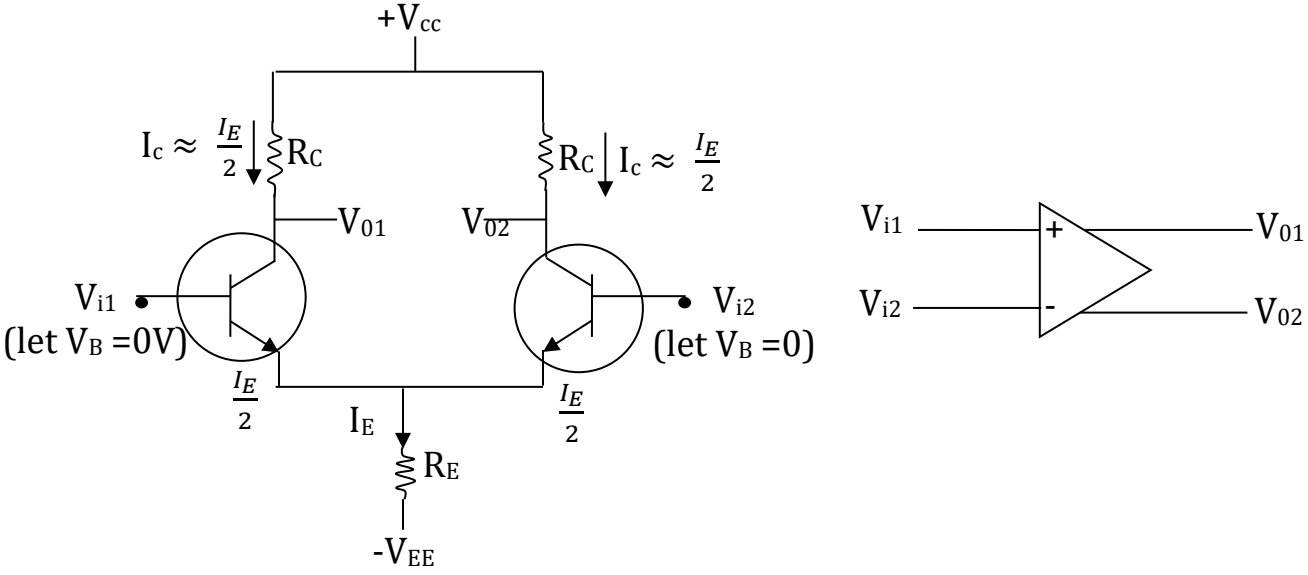


Double-ended input & Output



Common mode operation

Differential Amplifier Circuit



* The main feature is very large gain when opposite signals are applied to the inputs as compared to very small gain resulting from common inputs.

DC Bias

With each base voltage at 0V. The common-emitter DC bias voltage is

$$V_E = 0 - V_{EE} = -0.7V$$

$$I_E = \frac{V_E-(-V_{EE})}{R_E} \approx \frac{V_{EE}-0.7V}{R_E}$$

Assuming that both transiting are well method

$$I_{c1} = I_{c2} = \frac{I_E}{2}$$

& $V_{C1} = V_{C2} = V_{CC} - I_C R_C$

$$\boxed{V_{C_1} = V_{C_2} = V_{CC} - \frac{I_E}{2} R_C}$$

4.4 Characteristics of Ideal Op-Amp: (1) Input resistance $R_i = \infty$ so that there is no loss of input voltage $V_{in} = V_+ - V_-$ and is directly send at the output by the OP-Amp as

$V_{output} = A_v(V_1 - V_2)$

(2) Output resistance $R_o = 0$

So that output V_0 is directly send to load resistance and there is no drop across R_0.

(3) Voltage gain Av = $\frac{v_o}{v_i}$ =∞ (maximum amplification).

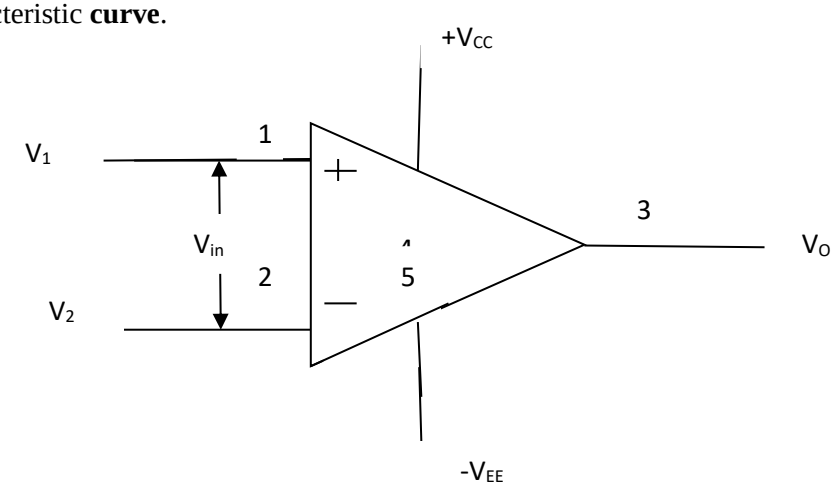
(4) V_{out} = 0 when $V_{in} = V_1-V_2=0$ i.e., $V_1=V_2$

(5) Bandwidth = ∞ (OP-Amp must operate at all frequencies)

(6) Characteristics don't drift with temperature.

4.4.1 Transfer Characteristics of Op-Amp:-

The curve plotted between output voltage and differential input voltage is called transfer characteristic **curve**.



$V_O = A_v V_{in} = A_v(V_1-V_2)$

Where A_v = Open loop voltage Gain= $A_v = \frac{v_o}{v_{in}}$

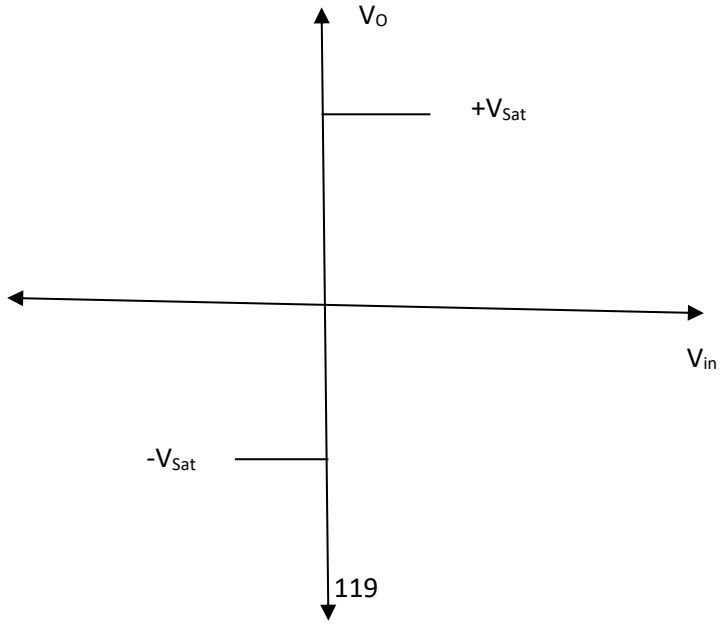
Case I: Ideal Op-Amp:-

For ideal Op-Amp $A_v = \infty$

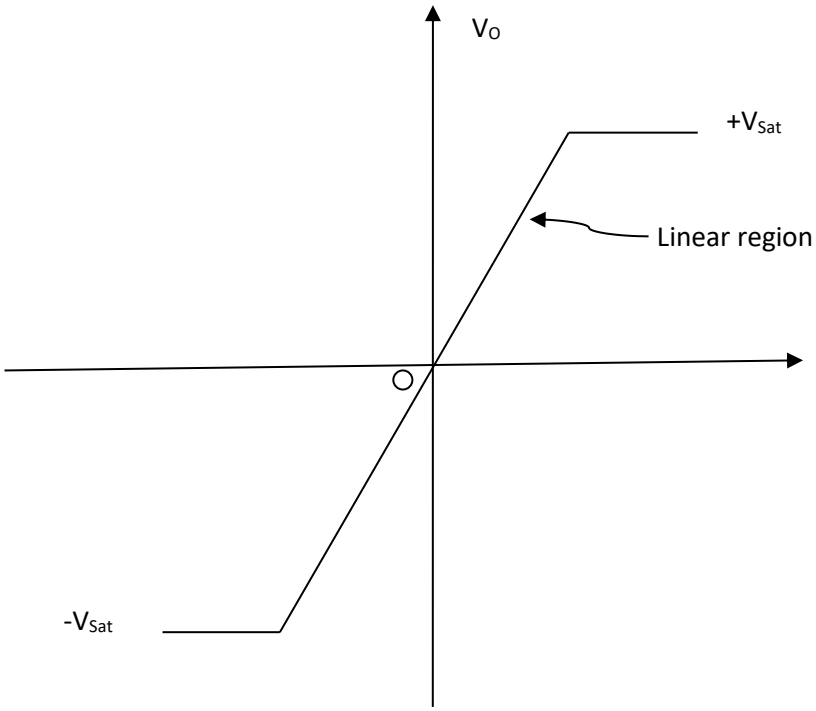
(i) When $V_{in} > 0$, i.e., $V_1 > V_2$; then Vo=+∞= $+V_{CC}$= the maximum voltage supplied at terminal 4 =$+V_{Sat.}$

(ii) When $V_{in} < 0$, i.e., $V_1 < V_2$; then Vo= -∞= $-V_{EE}$= the minimum voltage supplied at terminal 5 =$-V_{Sat.}$

(iii) When $V_{in}=0$, i.e., $V_1=V_2$; then $V_O = 0$



(Transfer Characteristics curve for Ideal op-Amp)



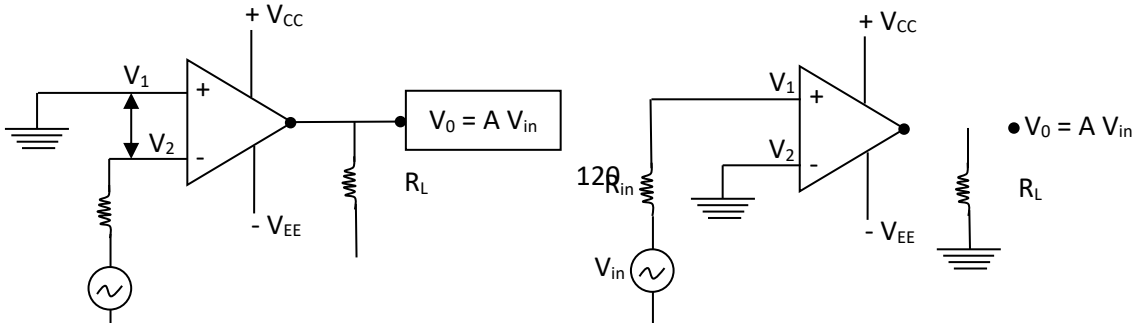
(Transfer Characteristics curve for practical op-Amp)

Self- check 1: Why is the name Operational Amplifier?

4.5 <u>Open – loop differential Amplifier</u> Op-Amp without feedback circuitry is called open loop differential amplifier.

There are three open-loop Op-Amp configurations:-

1. Differential Amplifier
2. Inverting Amplifier
3. Non-inverting Amplifier



Inverting Amplifier **Non-inverting Amplifier**

4.6 Closed Loop Gain:

The gain of an op-amp without feedback is called the open-loop gain whereas the gain of an op-amp with a feedback circuit is called the **closed-loop gain**. There are basically two types of circuits for closed loop gain, one is inverting Op-Amp and other is non-inverting Op-Amp.

1- Inverting Amplifier: From figure the point A is at virtual ground, hence

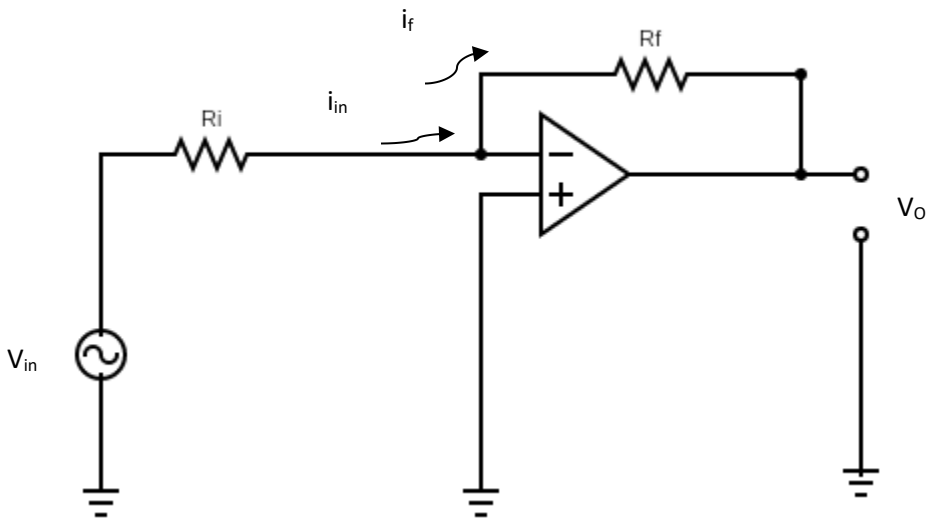


Figure 4.10 Inverting Op-Amp

Appliying KVL, we can write

$\mathbf{I}_{in} = \frac{V_{in}-V_A}{R_i} = \frac{V_{in}-0}{R_i} = \frac{V_{in}}{R_i}$ and

$\mathbf{I}_f = \frac{V_A - V_{Out}}{R_f} = \frac{0 - V_{Out}}{R_f} = \frac{-V_{Out}}{R_f}$

Since $\mathbf{I}_{in} = \mathbf{I}_f$ (For an ideal OP amp)

$\frac{-V_{Out}}{R_f} = \frac{V_{in}}{R_i}$

Hence Voltage gain $A_{CL} = \frac{V_{Out}}{V_{in}} = -\frac{R_f}{R_i}$

2- **Non inverting amplifier:** Figure 4.11 represents the non-inverting Op-Amp circuit, applying KCL we have,

Current through R_i = Current through R_f

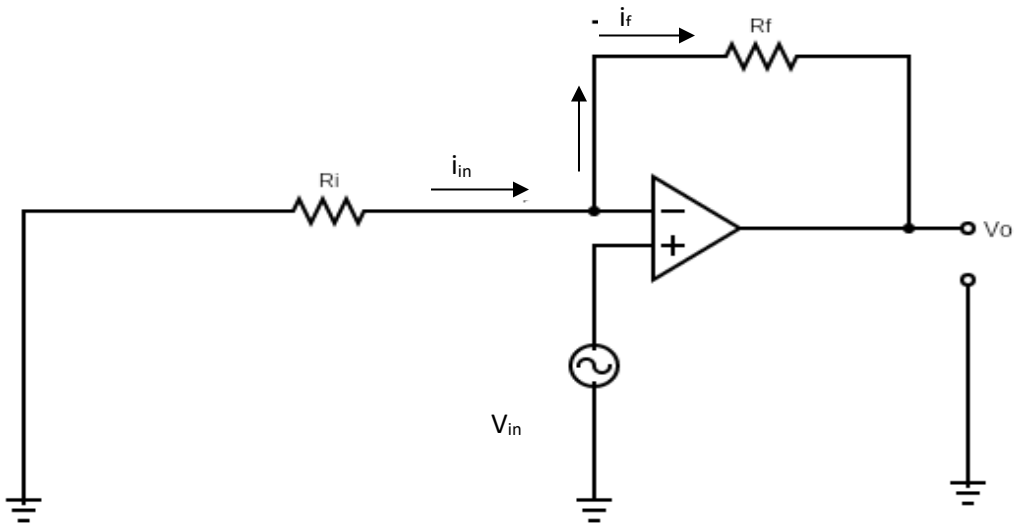


Figure 4.11 Non-inverting Op-Amp

$\mathbf{I}_{in} = \frac{V_{in}-0}{R_i} = \frac{V_{Out}-V_{in}}{R_f}$

$\mathbf{V_{in}}\ R_f = V_{Out}\ R_i - V_{in} R_i$

$\mathbf{V_{in}}\ (R_f + R_i) = V_{Out}\ R_i$

$\frac{V_{Out}}{V_{in}} = \frac{R_f + R_i}{R_i}$

Hence Voltage gain $A_{CL} = \frac{V_{Out}}{V_{in}} = 1 + \frac{R_f}{R_i}$

3- OUTPUT OFFSET VOLTAGE (V_{OO})

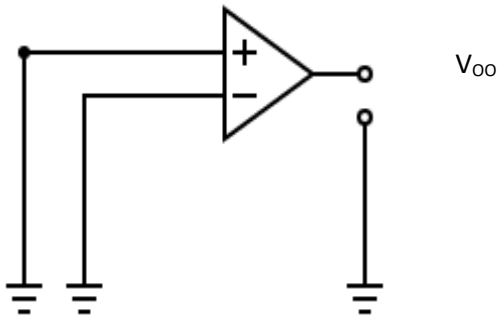


Figure 4.12 Output Offset Voltage

The voltage present at output without any input applied is called output offset voltage.

- Even though all the components are integrated on the same chip,it is not possible to have two transistors in the input stage with exactly the same characteristics.

- So difference in collector currents causes some small differential output which gets amplified in further stage.
- By applying differential voltage of opposite polarity at one of the input terminal.
- When both inputs are grounded, ideally the output must be zero. But practically op-amp produces the small output voltage. To nullify this voltage some voltage is required to be applied to either of the two inputs. This is called Input Offset Voltage.

3- INPUT OFFSET VOLTAGE (VIO)

The input 0ffset voltage is defined as the amount of voltage that must be applied between the two input terminals of the op-amp to obtain zero volts at the output.
Ideally, $V_O = A(V1-V2)=0$
Practically, V_O=some small value
Input offset voltage is applied at input.

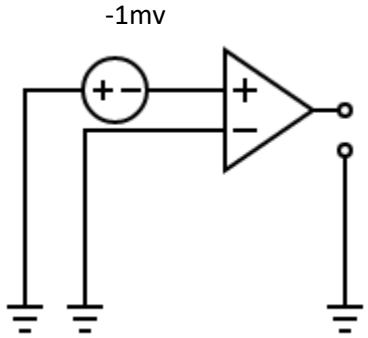


Figure 4.13 input Offset Voltage

4- INPUT OFFSET CURRENT(Iio)

The algebraic difference between the currents flowing into the inverting and non-inverting terminals is referred to as input offset current.

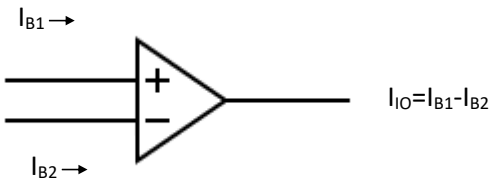


Figure 4.14 Input offset Current

$I_{io}=I_{B1}-I_{B2}$
Base currents of the differential amplifier stage.

Even though both of transistors are identical it is not possible to have IB1 and IB2 exactly equal to each other because of the internal imbalance between the two inputs.

5- INPUT BIAS CURRENT (IB)

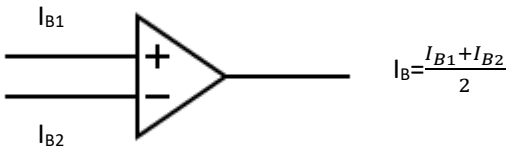


Figure 4.15 Input Bias Current

It is the average of the currents that flow into the inverting and non inverting input terminals of the op-amp.

$I_B=\frac{I_{B1}+I_{B2}}{2}$

6- COMMON MODE REJECTION RATIO

When the same input voltage is applied to both input terminals of an op-amp, the op-amp is said to be operating in a common mode configuration.

V_{cm}= common mode input

V_{ocm}= common mode output

Common mode voltage gain= $A_{cm}=\frac{V_{ocm}}{V_{cm}}$

Ideally op-amp amplifiers only differential input voltage but due to imperfections within practical op-amp some voltage will appear at output which is Vocm.

Common mode rejection ratio

$$A_{cm}=\frac{V_{Ocm}}{V_{cm}}$$

$$\text{CMRR} = \frac{\text{A}_\text{d}}{\text{A}_\text{cm}} = 20\log\frac{\text{A}_\text{d}}{\text{A}_\text{cm}}$$

CMRR is the ratio of the differential gain A_d to the common mode gain A_{cm}.

Generally expressed in db

For Op-Amp 741 IC , CMRR is 90 db.

7- Supply Voltage Rejection Ratio:

The change in an Op-Amps input offset voltage (V_{IO}) caused by variations in supply voltages is called the supply voltage rejection ratio(SVRR).

$$SVRR = \frac{\Delta V_{IO}}{\Delta V}$$

Where $\Delta V_{IO}$is change in input offset voltage.

ΔV is change in power supply.

8- **Thermal Drift**- Ideally parameters $V_{IO,}$ I_B, I_{IO}, are constants for Op-Amp but practically they vary with ;

(1) Change in temperature.
(2) Change in supply voltage V_{CC} and V_{EE}.
(3) Time of running device.

9- **Slew Rate:** Slew rate is defined as the maximum rate of change of output voltage per unit time and is expressed in volts per microseconds.

$$Slew\ Rate = (\frac{\Delta V_O}{\Delta t})_{max}$$

Slew rate indicates how rapidly the output of an Op-Amp can change in response to changes in input frequency

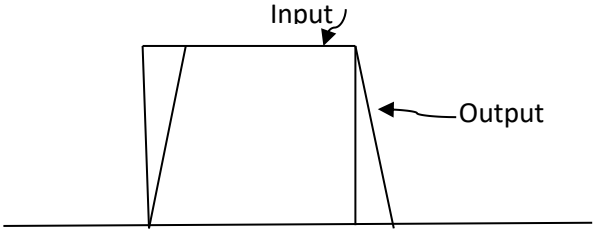


Figure 16 Distortion in signal due to Slew Rate

10- Differential Input Resistance:- The equivalent resistance that can be measured at either inverting or non-inverting input terminals with other terminal connected to ground.

11- Input Capacitance:- The equivalent capacitance that can be measured at either inverting or non-inverting terminal with other terminal connected to ground.

12- Common-Mode Rejection Ratio:- (CMRR)

$$CMRR = \frac{A_d}{A_{cm}} \qquad CMRR(dB) = 20log_{10}\frac{A_d}{A_{cm}}$$

13- Output Voltage swing:- The output voltage never exceeds the limit of given supply voltages, $+V_{CC}$ & $-V_{EE}$.

14- Output Resistance:- The equivalent resistance that can be measured between the output terminals of Op-Amp and ground. E.g. 75Ω for the 741.

4.7 IC 741 General purpose Operational Amplifier

The 741 Op Amp IC is a monolithic integrated circuit, comprising of a general purpose Operational Amplifier. It was first manufactured by Fairchild semiconductors in the year 1963. The number 741 indicates that this operational amplifier IC has 7 functional pins, 4 pins capable of taking input and 1 output pin.

IC 741 Op Amp can provide high voltage gain and can be operated over a wide range of voltages, which makes it the best choice for use in integrators, summing amplifiers and general feedback applications. It also features short circuit protection and internal frequency compensation circuits built in it. This Op-amp IC comes in the following form factors:

- 8 Pin DIP Package
- TO5-8 Metal can package
- 8 Pin SOIC

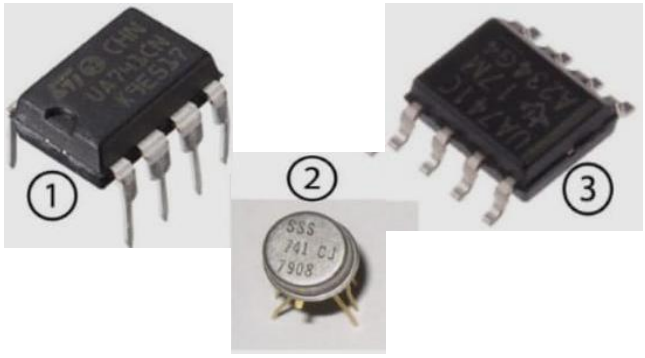


Figure 4.17 IC741

NOTE: The manufacturer of the first IC in the above picture in 8-pin DIP Package is STMicroelectronics and that of the third IC in 8-pin SOIC format is Texas Instruments. We couldn't find the information on the manufacturer of the second TO5-8 Metal can package IC.

4.8 Pinout of IC 741 Op Amp and their Functions

The below figure illustrates the pin configurations and internal block diagram of IC 741 in 8 pin DIP and TO5-8 metal can package.

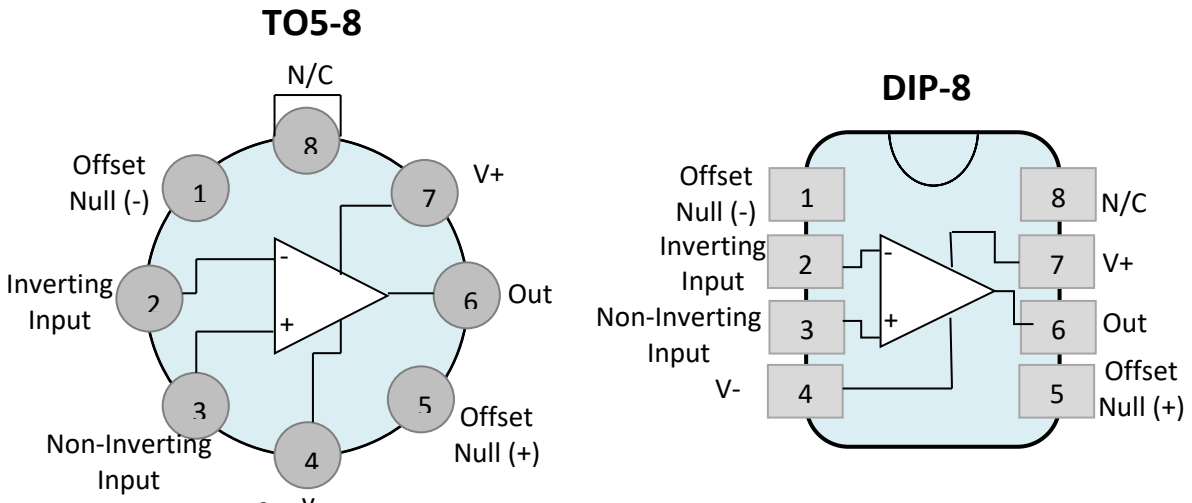


Figure 4.17 Pin-Outs of 741 IC

Now let's take a look at the functions of different pins of 741 IC:

- **Pin4 & Pin7 (Power Supply):** Pin7 is the positive voltage supply terminal and Pin4 is the negative voltage supply terminal. The 741 IC draws in power for its operation from these pins. The voltage between these two pins can be anywhere between 5V and two pins can be anywhere between 5V and 18V.
- **Pin6 (Output):** This is the output pin of IC 741. The voltage at this pin depends on the signals at the input pins and the feedback mechanism used. If the output is said to be high, it means that voltage at the output is equal to positive supply voltage. Similarly, if the output is said to be low, it means that voltage at the output is equal to negative supply voltage.
- **Pin2 & Pin3 (Input):** These are input pins for the IC. Pin2 is the inverting input and Pin3 is the non-inverting input. If the voltage at Pin2 is greater than the voltage at Pin3, i.e., the voltage at inverting input is higher, the output signal stays low.

  Similarly, if the voltage at Pin3 is greater than the voltage at Pin2, i.e., the voltage at non-inverting input is high, the output goes high.
- **Pin1 & Pin5 (Offset Null):** Because of high gain provided by 741 Op-Amp, even slight differences in voltages at the inverting and differences in voltages at the inverting and non-inverting inputs, caused due to irregularities in manufacturing process or external

disturbances, can influence the output. To nullify this effect, an offset voltage can be applied at pin1 and pin5, and is usually done using a potentiometer.

- **Pin8 (N/C):** This pin is not connected to any circuit inside 741 IC. It's just a dummy lead used to fill the void space in standard 8 pin packages.

Specifications

The following are the basic specifications of IC 741:

- **Power Supply:** Requires a Minimum voltage of 5V and can withstand up to 18V.
- **Input Impedance:** About 2 Ω
- **Output Impedance:** About *75* Ω
- **Voltage Gain:** 200,000 for low frequencies (200 V/mV)
- **Maximum Output Current:** 20 mA
- **Recommended Output Load:** Greater than *2 K*Ω
- **Input Offset:** Ranges between 2 mV and 6 mV
- **Slew Rate:** 0.5V/μS (It is the rate at which an Op-Amp can detect voltage changes)

NOTE: The above mentioned specifications are generic and may vary from manufacturer to manufacturer. To get accurate information, please refer to the datasheet.

- Question: What makes Op-Amp so special?
- Ans: The high input impedance and very small output impedance makes IC 741 a near ideal voltage amplifier.

4.9 Zero Crossing Detector using 741 IC

The zero crossing detector circuit is an important application of the op-amp comparator circuit. It can also be called as the sine to square wave converter. Anyone of the inverting or non-inverting comparators can be used as a zero-crossing detector. The only change to be brought in is the reference voltage with which the input voltage is to be compared, must be made zero (V_{ref} = 0V). An input sine wave is given as V_{in}. These are shown in the circuit diagram and input and output waveforms of an inverting comparator with a 0V reference voltage.

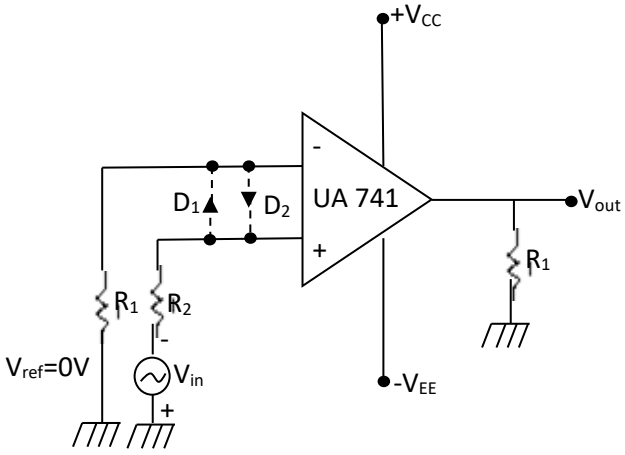


Figure 4.18 Zero Crossing Detector Using UA 741 op-amp IC

As shown in the waveform, for a reference voltage 0V, when the input sine wave passes through zero and goes in positive direction, the output voltage V out is driven into negative saturation. Similarly, when the input voltage passes through zero and goes in the negative direction, the output voltage is driven to positive saturation. The diodes D1 and D2 are also called diodes. They are used to protect the op-amp from damage due to increase in input voltage. They clamp the differential input voltages to either +0.7V or -0.7V.

In certain applications, the input voltage may be a low frequency waveform. This means that the waveform only changes slowly. This causes a delay in time for the input voltage to cross the zero-level. This cause further delay for the output voltage to switch between the upper and lower saturation levels. At the same time, the input noises in the op-amp may cause the output voltage to switch between the saturation levels. Thus zero noise voltages in input voltage. These difficulties can be removed by using a regenerative feedback circuit

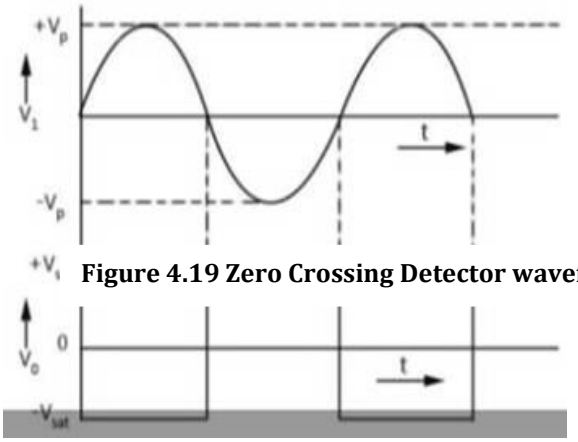


Figure 4.19 Zero Crossing Detector waveform

Zero-Crossing Detector Using 741 IC Waveforms

with a positive feedback that causes the output voltage to change faster thereby eliminating the possibility of any false zero crossing due to noise voltages at the op-amp input.

Applications of Zero Crossing Detector

Zero crossing detectors widely find applications in electronics circuits mainly for switching purpose and in phase locked loop. Also, these are used in frequency counters and in phase meters. It can also be used as phase meters, as it can be used to measure the phase angle between two voltages applied at its terminals.

4.10 Op-amp Comparator OR Positive and negative voltage level detector

The comparator is an electronic decision making circuit that makes use of an operational amplifiers very high gain in its open-loop state, that is, there is no feedback resistor.

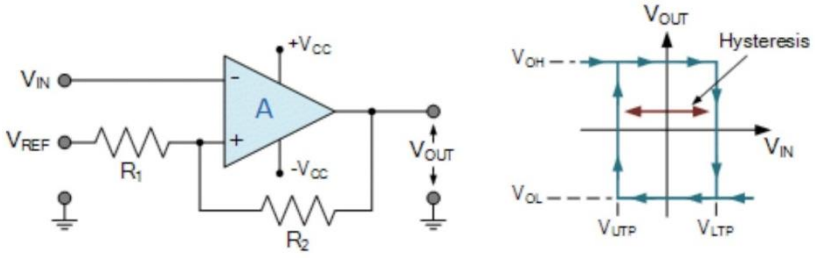


Figure 4.20 Op-Amp Comparator

The Op-amp comparator compares one analogue voltage level, or some preset reference voltage, V_{REF} and produces an output signal based on this voltage comparison. In other words, the op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is the largest of the two.

Op-amp Comparator Circuit

With reference to the op-amp comparator circuit above, lets first assume that V_{IN} is less than the DC voltage level at V_{REF}, ($V_{IN} < V_{REF}$). As the non-inverting (positive) input of the comparator is less than the inverting (negative) input, the output

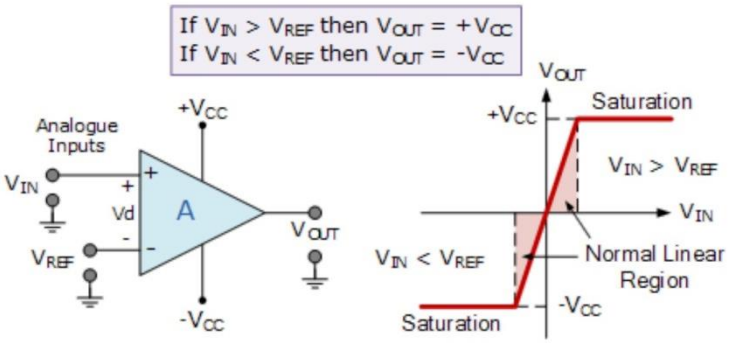


Figure 4.21 Op-Amp Comparator circuit

will be LOW and at the negative supply voltage, $-V_{cc}$ resulting in a negative saturation of the output.

If we now increase the input voltage, V_{IN} so that its value is greater than the reference voltage V_{REF} on the inverting input, the output voltage rapidly switches HIGH towards the positive supply voltage, $+V_{cc}$ resulting in a positive saturation of the output. If we reduce again the input voltage V_{IN}, so that it is slightly less than the reference voltage, the op-amp's output switches back to its negative saturation voltage acting as a threshold detector.

Then we can see that the op-amp voltage comparator is a device whose output is dependant on the value of the input voltage, V_{IN} with respect to some DC voltage level as the output is HIGH when the voltage on the non-inverting input is greater than the voltage on the inverting input, and LOW when the non-inverting input is less than the inverting input voltage. This condition is true regardless of whether the input signal is connected to the inverting or the non-inverting input of the comparator.

We can also see that the value of the output voltage is completely dependent on the op-amps power supply voltage. In theory due to the op-amps high open-loop gain the magnitude of its output voltage could be infinite in both directions, (±&#8734). However practically, and for obvious reasons it is limited by the op-amps supply rails giving $V_{OUT} = +V_{cc}$ or $V_{OUT} = -V_{cc}$.

We said before that the basic op-amp comparator produces a positive or negative voltage output by comparing its input voltage against some preset DC reference voltage. Generally, a resistive voltage divider is used to set the input reference voltage of a comparator, but a battery source, zener diode or potentiometer for a variable reference voltage can all be used as shown.

Comparator Reference Voltages

In theory the comparators reference voltage can be set to be anywhere between 0v and the supply voltage but there are practical limitations on the actual voltage range depending on the op-amp comparator being device used.

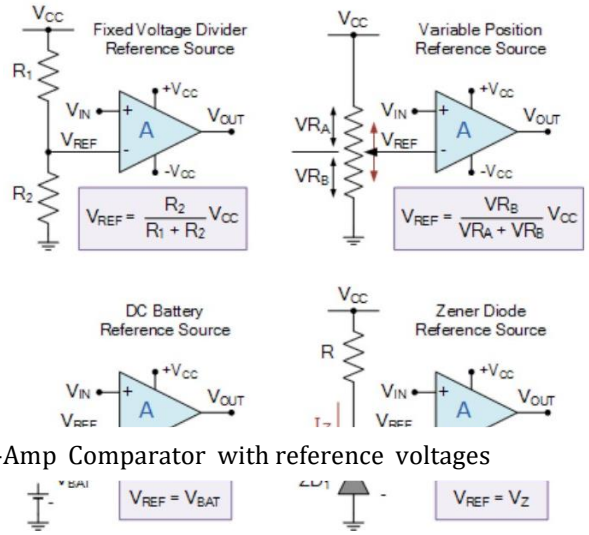


Figure 4.22 Op-Amp Comparator with reference voltages

Positive and Negative Voltages Comparator

A basic op-amp comparator circuit can be used to detect either a positive or a negative going input voltage depending upon which input of the operational amplifier we connect the fixed reference voltage source and the input voltage too. In the examples above we have used the inverting input to set the reference voltage with the input voltage connected to the non-inverting input.

But equally we could connect the inputs of the comparator the other way around inverting the output signal to that shown above. Then an op-amp comparator can be configured to operate in what is called an inverting or a non-inverting configuration.

Positive Voltages Comparator

The basic configuration for the positive voltage comparator, also known as a non-inverting comparator circuit detects when the input signal, V_{IN} is ABOVE or more positive than the reference voltage, V_{REF} producing an output at V_{OUT} which is HIGH as shown.

Non-inverting Comparator Circuit

In this non-inverting configuration, the reference voltage is connected to the inverting input of the operational amplifier with the input signal connected to the non-inverting input. To keep things simple, we have assumed that the two resistors forming the potential divider network are equal and: $R_1 = R_2 = R$. This will produce a fixed reference voltage which is one half

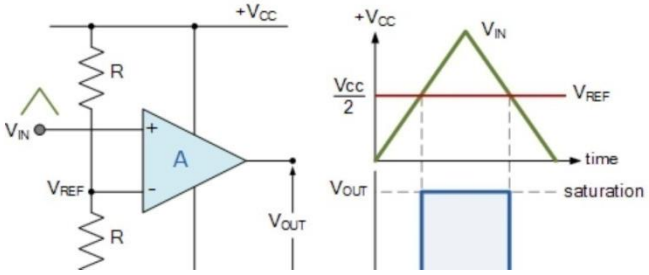


Figure 4.23 Non inverting Comparator Circuit

that of the supply voltage, that is $V_{cc}/2$, while the input voltage is variable from zero to the supply voltage.

When V_{IN} is greater than V_{REF}, the op-amp comparators output will saturate towards the positive supply rail, V_{cc}. When V_{IN} is less than V_{REF} the op-amp comparators output will change state and saturate at the negative supply rail, 0_v as shown.

Negative Voltage Comparator

The basic configuration for the negative voltage comparator, also known as an inverting comparator circuit detects when the input signal, V_{IN} is BELOW or more negative than the reference voltage, V_{REF} producing an output at V_{OUT} which is HIGH as shown.

Inverting Comparator Circuit

In the inverting configuration, which is the opposite of the positive configuration above, the reference voltage is connected to the non-inverting input of the operational amplifier while the input signal is connected to the inverting input. Then when V_{IN} is less

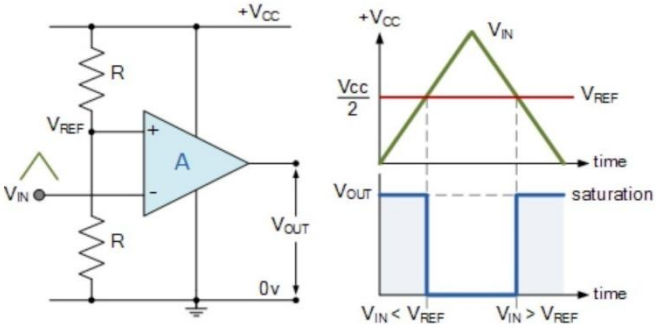


Figure 4.24 Inverting Comparator Circuit

than V_{REF} the op-amp comparators output will saturate towards the positive supply rail, V_{cc}.

Likewise the reverse is true, when V_{IN} is greater than V_{REF}, the op-amp comparators output will change state and saturate towards the negative supply rail, 0V.

Then depending upon which op-amp inputs we use for the signal and the reference voltage, we can produce an inverting or non-inverting output. We can take this idea of detecting either a negative or positive going signal one step further by combining the two op-amp comparator circuits above to produce a window comparator circuit.

Comparator Voltage Level Detector

As above, the voltage divider network provides a set of reference voltages for the individual op-amp comparator circuits. To produce the four reference voltages will require five resistors. The junction at the bottom pair of resistors will produce a reference voltage that is one-fifth the supply voltage, $1/5V_{cc}$ using equal value resistors. The second pair $2/5V_{cc}$, a third pair $3/5V_{cc}$ and so on, with these reference voltages increasing by a fixed amount of one-fifth (1/5) towards $5/5V_{cc}$ which is actually V_{cc}.

As the common input voltage increases, the output of

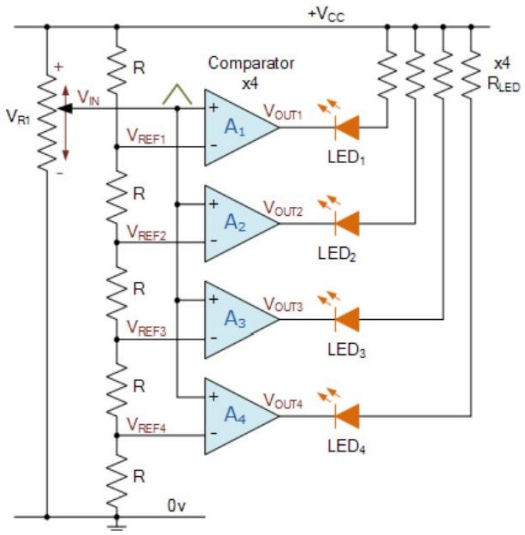


Figure 4.25 Non inverting Comparator Circuit

each op-amp comparator circuit switches in turn thereby turning OFF the connected LED starting with the lower comparator, A_4 and upwards towards A_1 as the input voltage increases. So by setting the values of the resistors in the voltage divider network, the comparators can be configured to detect any voltage level. One good example of the use of voltage level detection and indication would be for a battery condition monitor by reversing the LED's and connecting them to 0V (ground) instead of V_{CC}.

Also by increasing the number of op-amp comparators in the set, more trigger points can be created. So for example, if we had eight op-amp comparators in the chain and fed the output of each comparator to an 8-to-3 line Digital Encoder, we could make a very simple analogue-to-digital converter, (ADC) that would convert the analogue input signal into a 3-bit binary code (0-to-7).

Op-amp Comparator with Positive Feedback

We have seen here that operational amplifiers can be configured to operate as comparators in their open-loop mode, and this is fine if the input signal varies rapidly or is not too noisy. However if the input signal, V_{IN} is slow to change or electrical noise is present, then the op-amp comparator may oscillate switching its output back and forth between the two saturation states, $+V_{cc}$ and V_{cc} as the input signal hovers around the reference voltage, V_{REF} level. One way to overcome this problem and to avoid the op-amp from oscillating is to provide positive feedback around the comparator.

As its name implies, *positive feedback* is a technique for feeding back a part or fraction of the output signal that is in phase to the non-inverting input of the op-amp via a potential divider set up by two resistors with the amount of feedback being proportional to their ratio.

The use of positive feedback around an op-amp comparator means that once the output is triggered into saturation at either level, there must be a significant change to the input signal V_{IN} before the output switches back to the original saturation point. This difference between the two switching points is called **hysteresis** producing what is commonly called a Schmitt trigger circuit. Consider the inverting comparator circuit below.

Inverting Op-amp Comparator with Hysteresis

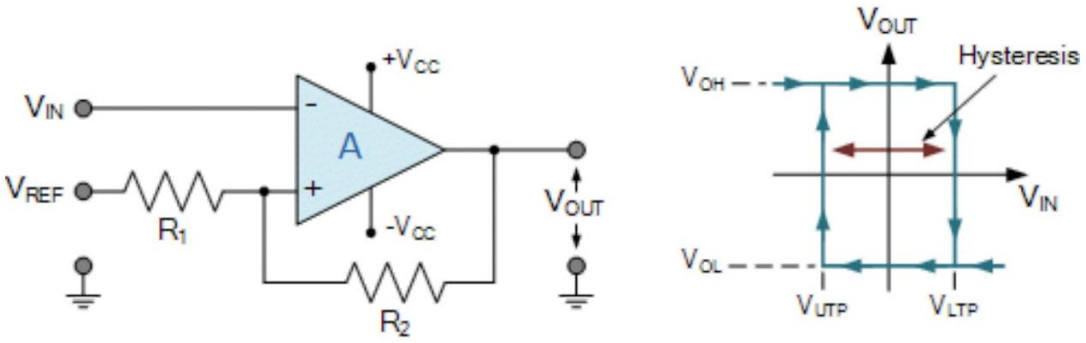


Figure 4.26 Inverting Comparator Circuit with Hysteresis

For the inverting comparator circuit above, V_{IN} is applied to the inverting input of the op-amp. Resistors R_1 and R_2 form a voltage divider network across the comparator providing the positive feedback with part of the output voltage appearing at the non-inverting input. The amount of feedback is determined by the resistive ratio of the two resistors used and which is given as:

Non-inverting Op-amp Comparator with Hysteresis

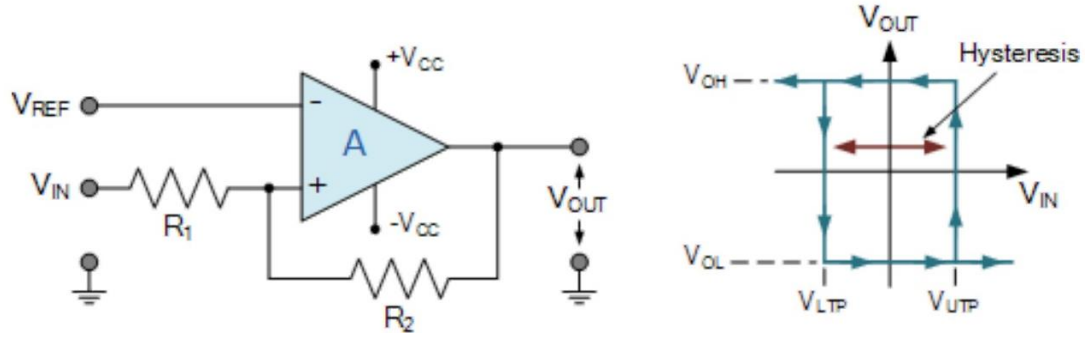
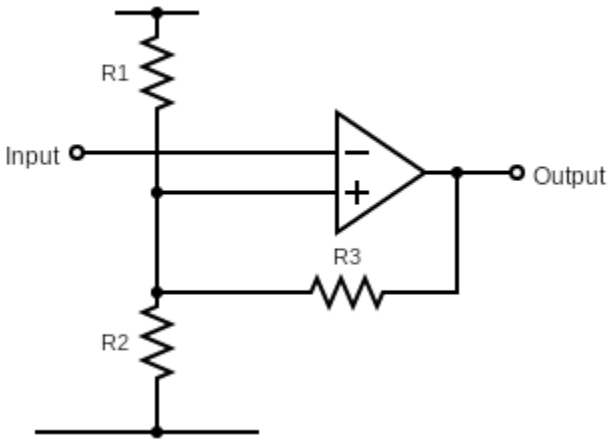


Figure 4.27Non-inverting Comparator Circuit with Hysteresis

Note that the arrows on the hysteresis graph indicate the direction of switching at the upper and lower trip points.



4.11 Worked Examples

Example 1: Draw the circuit diagram for positive feedback which is used for square wave generator

Answer: Schmitt Trigger is a device made by Op-Amp with positive feedback and used to generate square wave. The Schmitt Trigger is a widely used circuit used with a comparator to provide noise immunity and reduce the possibility of multiple switchings cause by noise on the input.

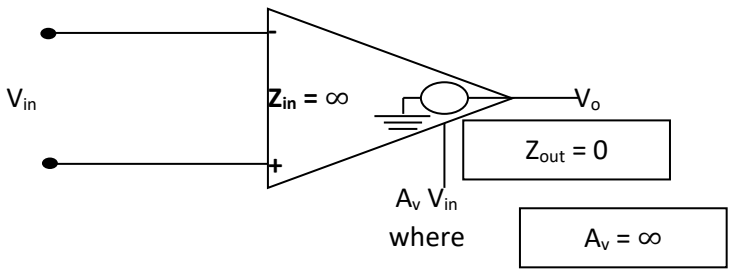
A Schmitt Trigger is form of comparator circuit that has hysteresis or different input switching levels to change the output between the two states.

Figure (Schmitt Trigger

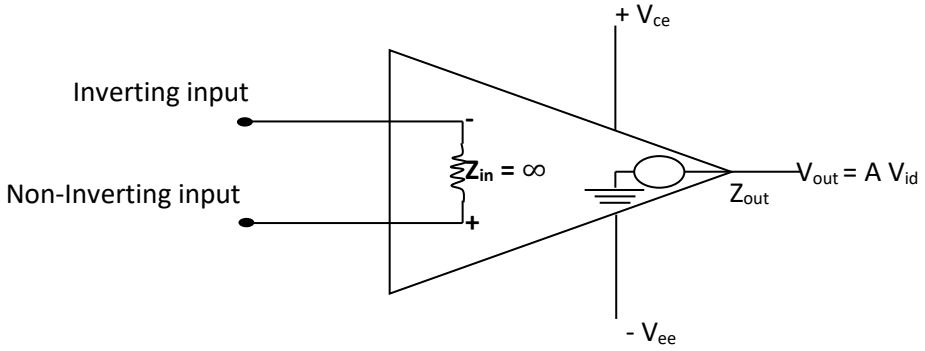
4.12 SUMMARY

Ideal OP-AMP

1. Infinite voltage gain A.
2. Infinite input resistance R_i so that almost any signal source can drive it and there is no loading of the preceding stage.
3. Zero output resistance R_0 so that it can drive an infinite no. of other devices.
4. Zero output voltage when input voltage is zero.
5. Infinite bandwidth (any signal (0 to ∞Hz) can be amplified without attenuation.
6. Infinite common-mode rejection ratio so that the output common-mode noise voltage is zero.
7. Infinite slew rate so that the output voltage changes occur simultaneously with input voltage changes.



Ideal Op-Amp



Practical Op-Amp

Important Conclusions and Concepts

1. Differential operation involves the use of opposite polarity inputs.
2. Common-mode operation involves the use of the same polarity inputs.
3. Common-mode rejection compares the gain for differential inputs to that for common inputs.
4. An op-amp is an operational amplifier.
5. The basic features of an op-amp are:
   Very high input impedance (typically megohms)
   Very high voltage gain (typically a few hundred thousand and greater)
   Low output impedance (typically less than 100 Ω)
6. Virtual ground is the concept based on the practical fact that the differential input voltage between plus (+) and minus(-) inputs is nearly (virtually) zero volts-when calculated as the output voltage (at most, that of the voltage supply) divided by the very high voltage gain of the op-amp.
7. Basic op-amp connections include:
   Inverting amplifier
   Noninverting amplifier
   Unity-gain amplifier
   Summing amplifier
   Integrator amplifier
8. Op-amp specs include:
   Offset voltages and currents
   Frequency parameters

Gain-bandwidth

Slew rate

Equations

$$CMRR = 20\,Log_{10}\frac{A_d}{A_c}$$

Inverting amplifier:

$$\frac{V_o}{V_i} = \frac{R_f}{R_1}$$

Noninverting amplifier:

$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

Unity follower:

$$V_o = V_1$$

Summing amplifier:

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

Integrator amplifier:

$$v_o(t) = -\frac{1}{RC}\int v_t(T)dt$$

$$\text{Slew rate (SR)} = \frac{\Delta V_o}{\Delta t} \qquad V/\mu s$$

In this chapter we have discussed about the fundamentals of Op-Amp and various concept over which this device works. We discussed the concept of virtual ground, Slew rate, offset nulls, input offset and output offset voltages, transfer characteristics of Ideal and practical Op-Amp**.** Readers are suggested to go through reference section for further study**.**

4.13 Modal Questions

1- Why do we need Op-Amp?
10- What is the virtual ground?
11- What is the difference between Comparator and Schmitt Trigger?
12- Draw the circuit diagram for Op-Amp as astable and Monostable Multivibrators
13- Define the Slew Rate?
14- What are differences in Input offset and output offset voltages and how we can overcome these offsets.

4.14 References and further readings

Linear integrated Circuit by D Roy choudhary

Introduction of Operational Amplifier and circuit theory by Boylstad

UNIT 5 Inverting and Noninverting Amplifiers

Structure

5.1 INTRODUCTION

An operational amplifier or op-amp is a very high gain voltage amplifying device. It has very high input impedance and very low output impedance. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain.

Figure 5.1 shows a basic op-amp with two inputs and one output.One of the inputs, which is marked with a negative or minus sign (–) is called inverting input.The other input is called the non-inverting input and marked with a positive or plus sign (+). A third terminal represents the operational amplifiers output port.

The OP-AMP is designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. These feedback components determine the resulting function of the amplifier. It can be used to implement various mathematical and logical functions. Also, Operational amplifier is used to achieve high voltage amplification, and to design oscillators, filters circuits, and various types of instrumentation circuits.

5.2 OBJECTIVES

After studying this unit, you will know about-

- Applications of op-amp as amplifiers such as inverting, non-inverting and differential amplifier
- Use of operational amplifier for mathematical functions: adder, subtractor, multiplier, and divider
- Comparator and wave shapers using operational amplifier
- Nonlinear applications of operational amplifier such as logarithmic amplifier, differentiator and integrator
- Analog computer

5.3 IDEAL Operational Amplifier:

Important characteristics of ideal OP-Amp is given in table 5.1 which are necessary to simple analysis of building blocks.

Table 5.1 : Parameters of ideal Op-AMP

Input Impedance	Infinite
Output Impedance	Zero
Open loop voltage gain	Infinite
Bandwidth	Infinite
Offset voltage	zero

5.4 INVERTING AMPLIFIER:

The circuit of analog inverting amplifier is shown in fig.5.2. The output V_O is connected to inverting input terminal (V_2) through a resistance R_F. Input signal (Vin) is connected to Inverting terminal through Resistance R.

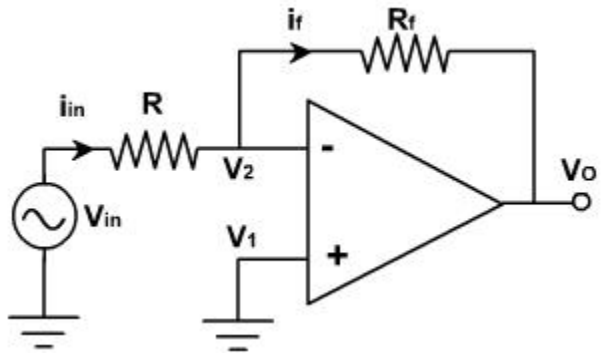


Fig.5.2: Analog inverting amplifier

Assuming OPAMP to be an ideal one, the differential input voltage is zero. i.e. $V_d = 0 = V_1 - V_2$, Therefore, $V_1=V_2=0$; Because V_1 is connected to ground, so V_2will be zero, this is called as virtual ground.Since input impedance is very high, therefore, input current is zero. OPAMP do not sink any current.

So, $i_{in} = i_f$

$(V_{in}-V_2) / R = (V_2 - V_O) / R_f$,

Since $V_2=0$

therefore, $V_O = - (R_f / R) V_{in}$ (5.1)

The negative sign in the equation indicates an inversion of the output signal with respect to the input as it is 180^o out of phase. This is due to the feedback being negative in value.

The equation for the output voltage V_O also shows that the circuit is linear in nature for a fixed amplifier gain as $V_O = V_{in}$ x Gain. Here gain is $-(R_f/R)$. This property can be very useful for converting a smaller sensor signal to a much larger voltage.

If $R = R_f$ then $V_O = -V_{in}$, the circuit behaves like an analog inverter.

5.5 NONINVERTING AMPLIFIER:

In this configuration, the input voltage signal, (V_{in}) is applied directly to the non-inverting (+) input terminal which means that the output gain of the amplifier is in same phase with input signal.

Feedback control of the non-inverting operational amplifier is achieved by voltage divider network. In voltage divider circuit resistance Rf is connected between Vo and INV (–) input terminal and resistance R is connected between INV and Ground terminal as shown in Fig. 5.3.

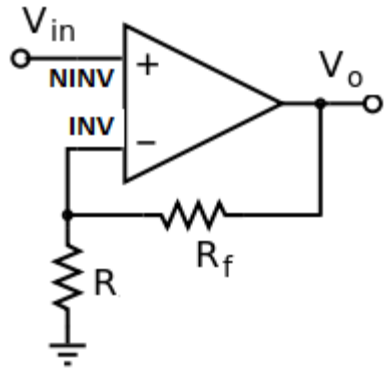


Fig.5.3: Analog Noninverting amplifier

Assuming OPAMP to be an ideal one, the differential input voltage is zero. i.e. $V_d = 0 = V_1 - V_2$, therefore, $V_1 = V_2$,

Since input impedance is very high, therefore, input current is zero. OPAMP do not sink any current.

So, $i_{inv} = i_{ninv} = 0$

now, Applying KCL at INV terminal $\frac{(Vo-V2)}{R_f} = \frac{(V0-0)}{R}$

$V_2 = V_1 = V_{in}$, replacing V_2 by V_{in}

$$Vo = \left(1 + \frac{R_f}{R}\right) Vin \qquad (5.2)$$

from the equation, it can be observed that the overall closed-loop gain of a non-inverting amplifier will always be either 1 or greater than one (unity), it is positive in nature and is determined by the ratio of the values of R_f and R.

If the value of the feedback resistor Rf is zero, and R is very large the gain of the amplifier will be exactly equal to one (unity). This special type of the non-inverting amplifier circuit called a Voltage Follower or also called a "unity gain buffer".

The advantage of the unity gain voltage follower is that it can be used when impedance matching or circuit isolation is more important than amplification as it maintains the signal voltage.

5.6 DIFFERENTIAL AMPLIFIER AND SUBTRACTOR:

A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs. It is an analog circuit with two inputs (V_a and V_b) and one outputV_O, in which the output is ideally proportional to the difference between the two voltages:

$$V_O = A\,(V_a - V_b)$$

where, A is the gain of the amplifier.

Single amplifiers are usually implemented by either adding the appropriate feedback resistors to a standard op-amp, or with a dedicated integrated circuit containing internal feedback resistors.

The basic differential amplifier is shown in fig. 5.4.

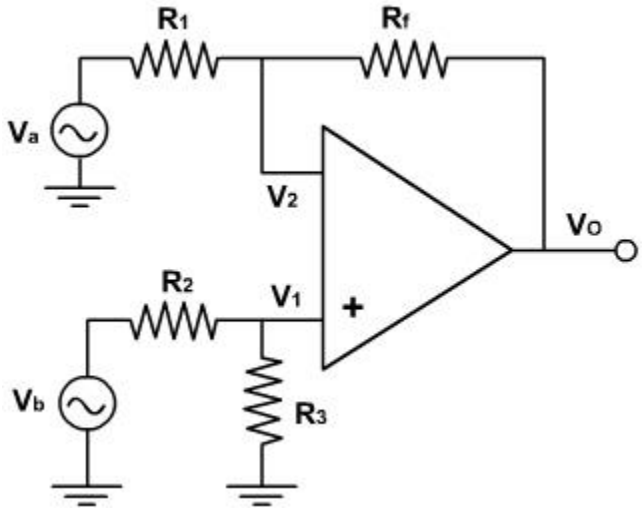


Fig. 5.4: Basic Differential Amplifier

Since there are two inputs and the circuit is linear, superposition theorem can be used to find the output voltage. When V_b= 0, then the circuit becomes inverting amplifier, hence the output due to V_a only is$V_{o(a)} = -(R_f / R_1)\, V_a$

Similarly when, V_a = 0, the configuration is a non-inverting amplifier having a voltage divided network at the noninverting input. Here $V_1$is the voltage at noninverting terminal due to input voltage $V_b$which is

$V_1 = (\frac{R3}{R2+R3})V_b$ **(5.3)**

The output due to noninverting voltage V_1

$V_{0(b)} = (1 + \frac{Rf}{R1})V_1$**(5.4)**

Now, replacing$V_1$with V_b, The output due to noninverting voltage is

$V_{0(b)} = (1 + \frac{Rf}{R1})(\frac{R3}{R2+R3})V_b$**(5.5)**

If ,R1 = R2 andRf = R3 $_{\text{then}}$ replacing$V_1$with V_b, The output due to noninverting voltage is

$V_{0(b)} = (\frac{Rf}{R1})V_b$ **(5.6)**

Therefore, the total output voltage V_0 is given by $V_0 = V_{0(a)} + V_{0(b)}$

$V_0 = (\frac{Rf}{R1})(-V_a + V_b)$ **(5.7)**

From the above equation, the output is the difference of two input with a gain of Rf/ R1.

If $R_f = R_1$, then gain of the *differential amplifiers* becomes 1 and the output is the difference of two input signals. Therefore, this type of operational amplifier circuit is known as **Subtractor.**

$V_0 = (-V_a + V_b)$ **(5.8)**

5.7 ADDER OR SUMMING AMPLIFIER:

Adder is a circuit in which two or more analog signals are to be added or combined into a single signal. It is also known as Summing Amplifier. One of best examples for such application is the Music Recording and Broadcasting applications. In case of a typical music recoding setup, it has several inputs from a number of microphones (instruments) and the output is stereo. In this setup adder combines several inputs into one common signal (output) without noise or interference. Adders are designed using two types ofconfiguration: Inverting and non-inverting.

5.7.1 Inverting Adders Amplifier

The most commonly used voltage AdderAmplifier is an extended version of the Inverting Amplifier configuration. Multipleinputs are applied to the inverting input terminal of the Op Amp, while the non-inverting input terminal is connected to ground. Due to this configuration, the output of Voltage Adder circuit is out of phase by 180^o with respect to the input.

A general design of the 3 inputvoltagesAdderAmplifier is shown in the figure 5.5. Three inputs voltages (V_1, V_2 and V_3) are appliedthrough their own input drive resistors through R_1, R_2 and R_3, respectively. Resistor (R_f) is in the feedback path between inverting and output terminal and non-inverting terminal is grounded.

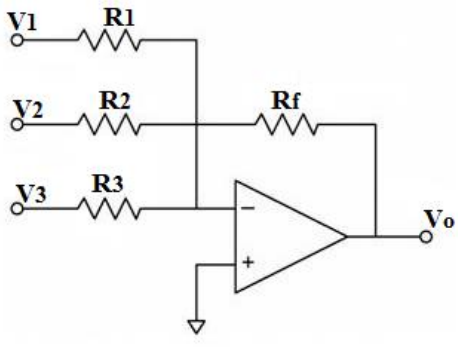


Fig. 5.5: 3-input Inverting Voltage Adder Amplifier

Before analyzing the above circuit, let us discuss about an important point in this setup: The concept of Virtual Ground. As the Non-Inverting Input of the above circuit is connected to ground, the Inverting Input terminal of the Op Amp is at virtual ground. As a result, the inverting input node becomes an ideal node for summing the input currents.

As the circuit is linear, superposition theorem can be used to find the output voltage. So, the output voltage

$$Vo= V_{o(V1)}+ V_{o(V2)}+ V_{o(V3)} , \qquad \textbf{(5.9)}$$

Where $V_{o(V1)}$is the output voltage when input voltage is V1 and all other input voltage sources are grounded.

When V_1 is applied and $V_2=V_3= 0$, then the circuit becomes inverting amplifier, hence the output due to V_1 only is$V_{o(V1)}= -(R_f / R_1) V_1$ **(5.10)**

Similarly,When V_2 is applied and $V_1=V_3= 0$, then the circuit becomes inverting amplifier, hence the output due to V_2 only is$V_{o(V2)}= -(R_f / R_2) V_2$ **(5.11)**

Similarly, When V_3 is applied and $V_2=V_3= 0$, then the circuit becomes inverting amplifier, hence the output due to V_3 only is$V_{o(V3)}= -(R_f / R_3) V_3$ **(5.12)**

So putting the value of$V_{o(V1)}$, $V_{o(V2)}$, and $V_{o(V3)}$in the equation $Vo = V_{o(V1)}+ V_{o(V2)}+ V_{o(V3)}$

we get,

$$Vo = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \qquad \textbf{(5.13)}$$

This equation is for a Scaling Summing Amplifier, as the input resistances here are not equal. But if all the input resistances are chosen to be of equal magnitude (R_1=R_2= R_3), then the Summing Amplifier is said to be having an equal-weighted configuration, where the gain for each input channel is same and output equation is as follows:

$$\text{Vo} = -\frac{R_f}{R_1}(V_1 + V_2 + V_3) \qquad \textbf{(5.14)}$$

Sometimes, it is necessary to just add the input voltages without amplifying them. In such situations, the value of input resistance R_1, R_2, R_3 etc. must be chosen equal to that of the feedback resistor R_f. As a result, the gain of the amplifier will be unity. Hence, the output voltage will be an addition of the input voltages.

$$\text{Vo} = -(V_1 + V_2 + V_3) \qquad \textbf{(5.15)}$$

5.7.2 Non-Inverting Adders

A Non-Inverting Adder Amplifier can also be constructed using the Non-Inverting Amplifier configuration of the Op Amp. Here, the input voltages are applied to the non-inverting input terminal of the Op Amp and a part of the output is fed back to the inverting input terminal.

The circuit of a Non-Inverting Summing Amplifier is shown in the figure5.6. In the circuit only three inputs are applied.

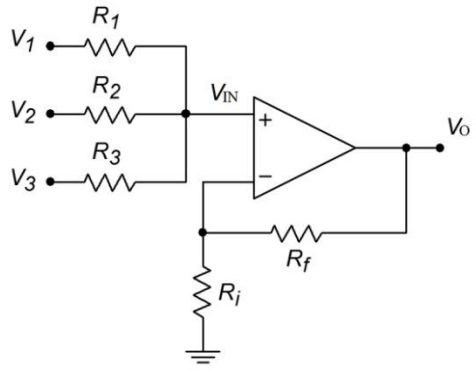


Fig. 5.6: 3-input Nonnverting Voltage Adder Amplifier

In this circuit as none of the input terminals are connected to the ground. So, the concept of virtual ground cannot be applied and the calculations are not as straight forward as the Inverting Summing Amplifier.

If, V_{IN} is the combination of all the input signals applied at the non-inverting terminal of the Op Amp.Then the output voltage is

$$\text{Vo} = \left(1 + \frac{R_f}{R_i}\right) V_{IN} \qquad \textbf{(5.16)}$$

Where, R_f and R_i are feedback resistor and inverting node resistor, respectively.
To calculate V_{IN}, apply Kirchoff Current Law at non-inverting terminal

So,

$$\frac{(V_1 - V_{IN})}{R_1} + \frac{(V_2 - V_{IN})}{R_2} + \frac{(V_3 - V_{IN})}{R_3} = 0 \qquad \textbf{(5.17)}$$

$$V_{IN} = \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) / \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) \qquad \textbf{(5.18)}$$

Putting the value of vin in eqn 5.17

$$\text{Vo} = \left(1 + \frac{R_f}{R_i}\right)\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) / \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) \qquad \textbf{(5.19)}$$

If $R_1 = R_2 = R_3 = R$,

$$\text{Vo} = \left(1 + \frac{R_f}{R_i}\right)\left(\frac{V_1 + V_2 + V_3}{3}\right) \qquad \textbf{(5.20)}$$

Now, keep $R_f = 2R_i$, then

$$\text{Vo} = (V_1 + V_2 + V_3) \qquad \textbf{(5.21)}$$

Eqn 5.21/ fig 5.6

5.8 COMPARATORS:

An analog **comparator** compares two inputs voltage level one is usually a constant reference voltage V_R , other is a time varying analog signal v_i and produces an output signal based on this voltage comparison. In other words, the op-amp voltage comparator compares the magnitudes of twovoltage inputs and determines which is the largest of the two.

The basic circuit of a comparator is shown in fig. 5.7**. Input signal** (V_i) **is applied at inverting terminal and reference voltage** (V_R) **is connected to** non-inverting terminal.**The** op-amp is in open loop configuration and has a very high open loop voltage gain. Due to high gain, when the non-inverting voltage (V_R) is larger than the inverting voltage (V_i) the comparator produces a high output voltage ($+V_{sat}$). When the non-inverting input (V_R) is less than the inverting input the output is low ($-V_{sat}$).

$V_O = -V_{sat}$ if $V_i > V_R$

$= +V_{sat}$ if $Vi < V_R$

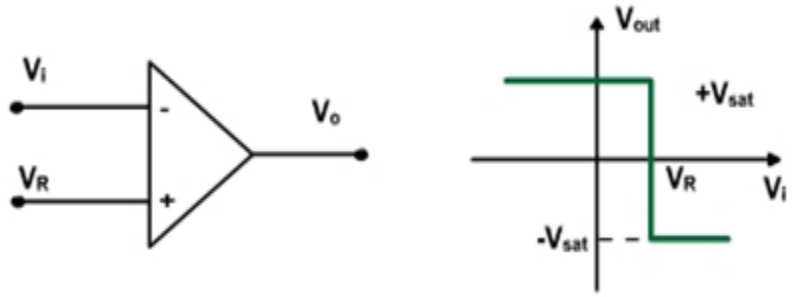


Fig. 5.7: The basic circuit of a comparator

If a sinusoidal input voltage is applied to the basic comparator, then the output will be as shown in fig.5.8

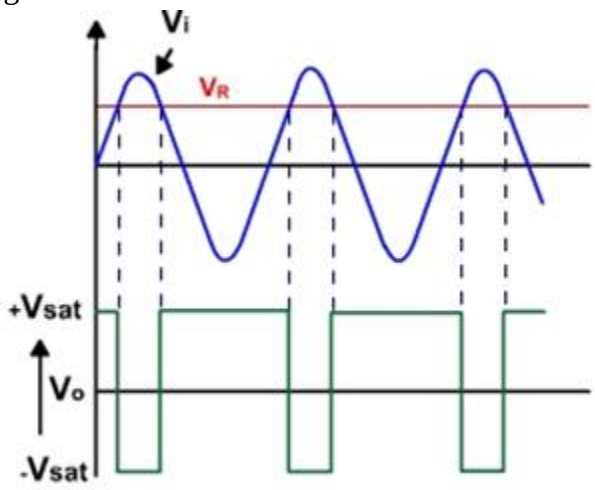


Fig. 5.8:output of a comparator for a sinusoidal input.

5.8.1 Zero crossing detectors

A zero-crossing detector is one type of voltage comparator, used to detect a sine waveform, triangular waveform etc. transition from positive and negative that coincide when the input crosses the zero voltage condition. The applications of the Zero Crossing Detector are phase meter and time marker generator.

A zero-crossing detector as shown in **fig.5.9**. Here $V_R = 0$, now if input voltage (in mV) is slightly higher than zero, then it is enough to saturate the OPAMP. If the supply voltages are ±15V, then the output compliance is from approximate – 13V to +13V. The more the open loop gain of OPAMP, the smaller the voltage required to saturate the output. If $v_d$required is very small then the characteristic is a vertical line as shown in **fig. 5.9**.

Every time the input crosses to zero, output changes either + V_{sat} to -V_{sat} or -V_{sat} to +V_{sat} which can be easily identified.

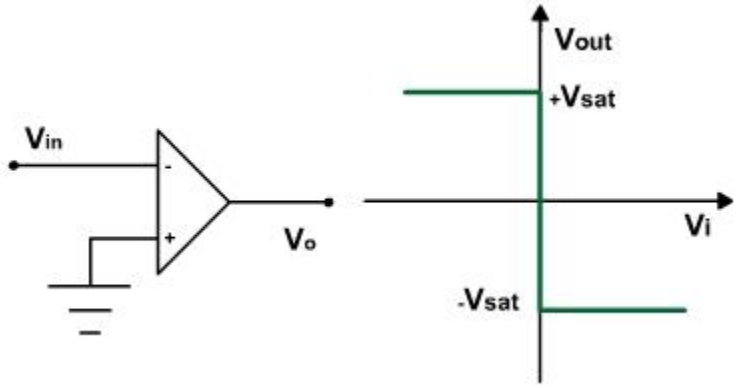


Fig. 5.9: zero crossing detector

5.8.2 Schmitt Trigger:

A Schmitt trigger circuit is also called a regenerative comparator circuit. The circuit is designed with a positive feedback and hence will have a regenerative action which will make the output switch levels. The use of a regenerative circuit is to remove the difficulties in a zero-crossing detector circuit due to low frequency signals and input noise voltages.

If the input to a comparator contains noise, the output may be erractive when V_{in} is near a trip point. For instance, with a zero crossing, the output is low when V_{in} is positive and high when V_{in} is negative. If the input contains a noise voltage with a peak of 1mV or more, then the comparator will detect the zero crossing produced by the noise. **Fig. 5.10**, shows the output of zero crossing detection if the input contains noise.

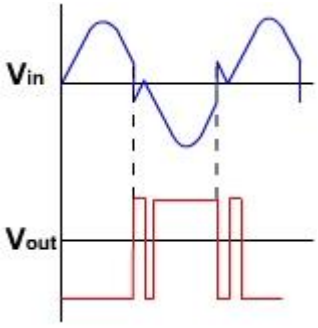


Fig. 5.10

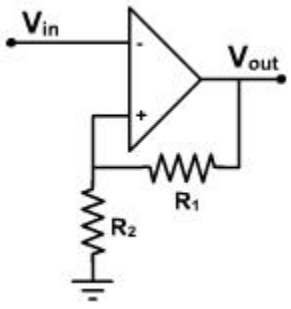


Fig. 5.11

This can be avoided by using a Schmitt trigger, circuit which is basically a comparator with positive feedback. **Fig. 5.11**, shows an inverting Schmitt trigger circuit using OPAMP.Because of the voltage divider circuit, there is a positive feedback voltage. When OPAMP is positively saturated, a positive voltage is feedback to the non-inverting input, this positive voltage holds the output in high stage. ($V_{in}<V_f$). When the output voltage is negatively saturated, a negative voltage feedback to the inverting input, holding the output in low state.

When the output is $+V_{sat}$ then reference voltage V_{ref} is given by

$V_{\text{ref}} = (\frac{\text{R1}}{\text{R1+R2}})V_{sat} = +\beta\ V_{sat}$ **(5.22)**

If V_{in} is less than V_{ref} output will remain $+V_{sat}$.

When input v_{in} exceeds $V_{ref} = +V_{sat}$ the output switches from $+V_{sat}$ to $-V_{sat}$. Then the reference voltage is given by

$V_{\text{ref}} = (\frac{-\text{R2}}{\text{R1+R2}})V_{sat} = -\beta\ V_{sat}$ **(5.23)**

The output will remain $-V_{sat}$ as long as $v_{in} > V_{ref}$.

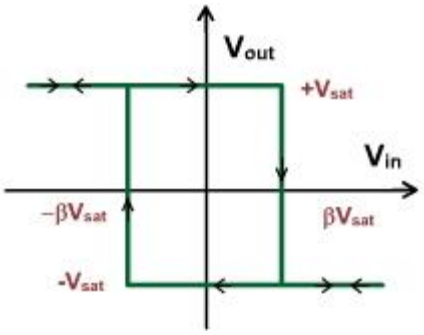


Fig. 5.12

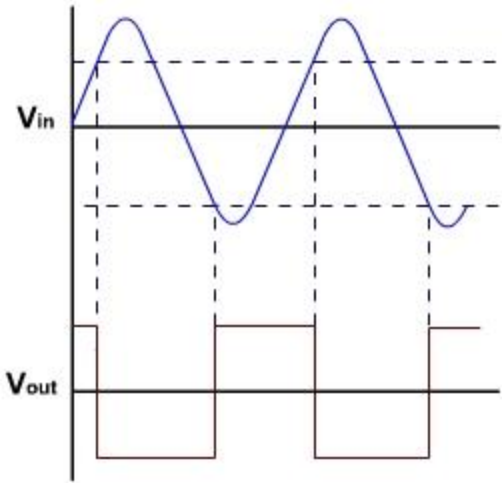


Fig. 5.13

If $V_{in} < V_{ref}$ i.e. V_{in} becomes more negative than $-V_{sat}$ then again output switches to $+V_{sat}$ and so on. The transfer characteristic of Schmitt trigger circuit is shown in fig. 5.12. The output is also shown in fig. 5.13 for a sinusoidal wave.

5.13/5.23/5.8

5.9 LOGARITHMIC/ ANTILOG AMPLIFIERS

5.9.1 Logarithmic Amplifier

A logarithmic amplifier, or a **log amplifier**, is an electronic circuit that produces an output that is proportional to the logarithm of the applied input.This circuit can be designed either with diode or BJT as feedback component and resistor as a series component.

The circuit diagram of a basic log amplifier using diode is shown in figure 5.14. The diode D is used in the feedback path.

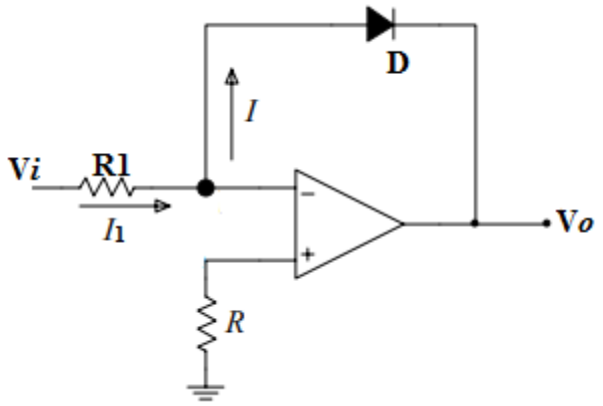


Fig. 5.14: Logarithmic Amplifier

By virtual ground $V_A = V_B = 0$.

As the op-amp draws zero input current, from the input side, we write

$$I = \frac{Vin - V_A}{R} = \frac{Vin}{R}$$

The current I also flows through the feedback path. Hence we write, Voltage across the diode is VA −VO = −VO. Hence using the diode current equation we write,

$$-V_O = \eta\, V_T\, ln\left(\frac{I}{I_O}\right)$$

Substituting for I, we get,

$$V_O = -\,\eta\, V_T\, ln\left(\frac{V_{in}}{RI_O}\right)$$

As I_OR is constant dc voltage, it is referred as V_{ref}.

$$V_O = -\,\eta\, V_T\, ln\left(\frac{V_{in}}{V_{ref}}\right)$$

It is seen that the output voltage is a function of logarithm of the input voltage. The basic log amplifier can also be constructed by replacing diode by a transistor. The output is proportional to the logarithm of the input given by

$$V_O = -\,V_T\, ln\left(\frac{V_{in}}{V_{ref}}\right)$$

However these circuits face demerits. They are

1. The reverse saturation current of the diode changes with change in temperature.
2. The Emitter saturation current also varies from one transistor to other and also with temperature. Hence setting Vref becomes difficult.
3. VT is also a function of temperature.

Hence, some sort of temperature compensation is required. Due to the presence of active elements like transistor, diodes in the feedback the circuit tends to oscillate. The circuit is compensated by

an emitter resistance and a capacitor across the negative feedback. This lowers the gain as the frequency increases and avoids oscillations. The resistance range as 1 KΩ and 100pF respectively.

5.9.2 Antilog Amplifier

An anti-logarithmic amplifier, or an anti-log amplifier, is an electronic circuit that produces an output that is proportional to the anti-logarithm of the applied input. The basic antilog amplifier is shown in the figure. The positions of diode and resistor are interchanged w.r.t log amplifier.

The circuit diagram of an op-amp based anti-logarithmic amplifier is shown in the following figure 5.15

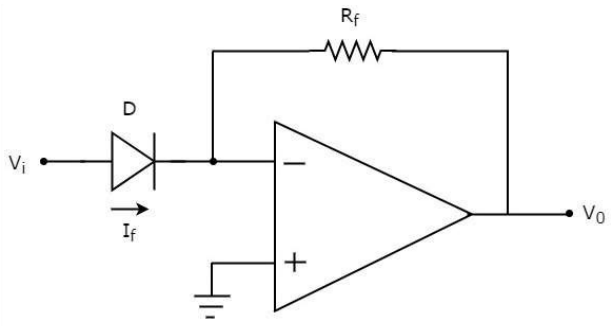


Fig. 5.15: Antilogarithmic Amplifier

In the circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. According to the virtual ground, the voltage at the inverting input terminal of op-amp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at its inverting input terminal will be zero volts.

The nodal equation at the inverting input terminal's node is –

$$-I_f + \frac{(0 - V_o)}{R_f} = 0$$

$\Rightarrow V_0 = -R_f I_f$

the current flowing through a diode in forward bias, is as given below –

$$I_f = I_s\, e\left(\frac{V_f}{\eta\, V_T}\right)$$

So,

$$V_o = -R_f I_s\, e\left(\frac{V_i}{\eta\, V_T}\right)$$

In the above equation the parameters η, V_T, andI_s are constantSo, the output voltage V_0 is proportional to the anti-log amplifier of the input voltage Vi, for a fixed value of feedback resistance R_f. Observe that the output voltage V0 is having a negative sign, which indicates that there exists a 180^0 phase difference between the input and the output.

It is seen that the output voltage is exponential function of the input. The basic antilog amplifier can also be constructed by replacing diode by a transistor. The output is proportional to the antilogarithm of the input given by the above equation. This equation holds good for both the cases. This equation is temperature dependent and hence as temperature changes the equation varies. So, the antilog amplifier also suffers from the same problem as that of log amplifier. Hence some sort of temperature compensation is required. The antilog amplifier is subjected to noise, bias currents, offset voltages, drifts and frequency stability problems. Transistorized circuits give accuracy, reduced bulk resistance and high operating ranges.

5.10 MULTIPLIER AND DIVIDER

5.10.1 Multiplier

A *multiplier* is a device with two inputs and a single output. The output potential is the product of the two inputs along with a scaling factor, *K*.

Vout=K VxVy

Typically, *K* is 0.1 in order to minimize the possibility of output overload. The schematic symbol for the multiplier is shown in Figure 5.16. It is called a four quadrant device, as both inputs and the output may be positive or negative.

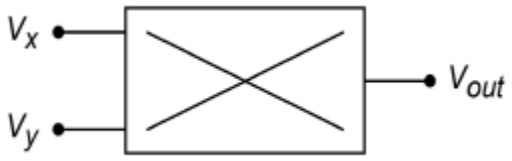


Fig. 5.16: Basic multiplier

Multipliers have many uses including squaring, dividing, balanced modulation/demodulation, frequency modulation, amplitude modulation, and automatic gain control. The most basic operation, multiplication, involves using one input as the signal input and the other input as the gain control potential. In multiplier circuit, the gain control potential is allowed to swing both positive and negative. A negative polarity will produce an inverted output. This basic connection is shown in Figure 5.17.

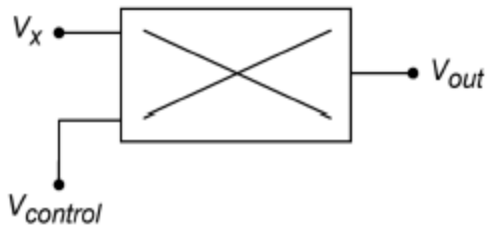


Fig. 5.17: Multiplication circuit

This same circuit can be used as a balanced modulator. This is very useful for creating dual sideband signals for communications work. Multipliers ICs may have external connections for scale factor and offset adjust potentiometers. Also, they may be modeled as current sources, so an external op amp connected as a current-to-voltage converter may be required.

If the two inputs are tied together and fed from a single input, the result will be a squaring circuit. Squaring circuits can be very useful for RMS calculations and for frequency doubling.

5.10.2 Divider

A divider circuit is shown in Figure 5.18.

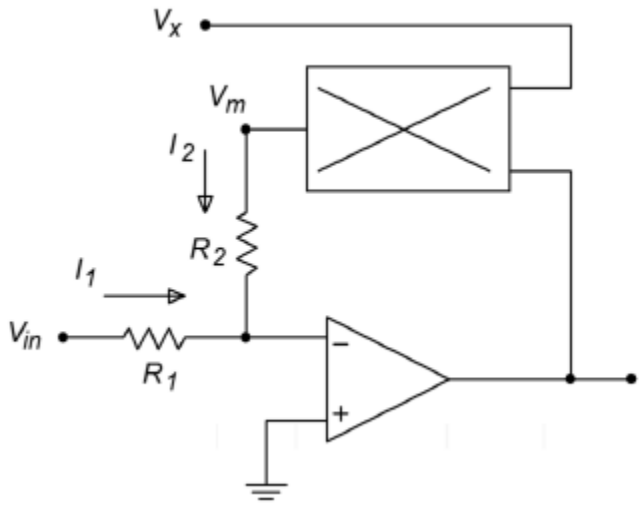


Figure 5.18: A divider circuit

Here's how it works: First, note that the output of the multiplier, *Vm*, is a function of *Vx*and the output of the op amp, *Vout*.

$V_m = K \cdot V_x \cdot V_{out}$

*Vm*produces a current through R_2. Note that the bottom end of $R_2$is at a virtual ground, so that all of $V_m$drops across R_2.

$I_2 = V_m / R_2$

As we have already seen,

$I_1 = V_{in} / R_1$

Now, because the current into the op amp is assumed to be zero, $I_1$and I_2must be equal and opposite. It is apparent that the arbitrary direction of $I_2$is negative. Therefore, if $R_1$is set equal to R_2,

Vm*=−*Vinand using Equation xxx,

$$-Vin = K \cdot Vx \cdot Vout$$

$$Vout = -Vin/(K \cdot Vx)$$

*Vx*then sets the magnitude of the division.

5.11 DIFFERENTIATOR AND INTEGRATOR:

5.11.1 Differentiator

A differentiator is an electronic circuit that produces an output equal to the first derivative of its input ora circuit in which the output voltage waveform is the differentiation of input voltage is called differentiator.

An op-amp based differentiator produces an output, which is equal to the differential of input voltage that is applied to its inverting terminal. The circuit diagram of an op-amp based differentiator is shown in the following figure 5.19.

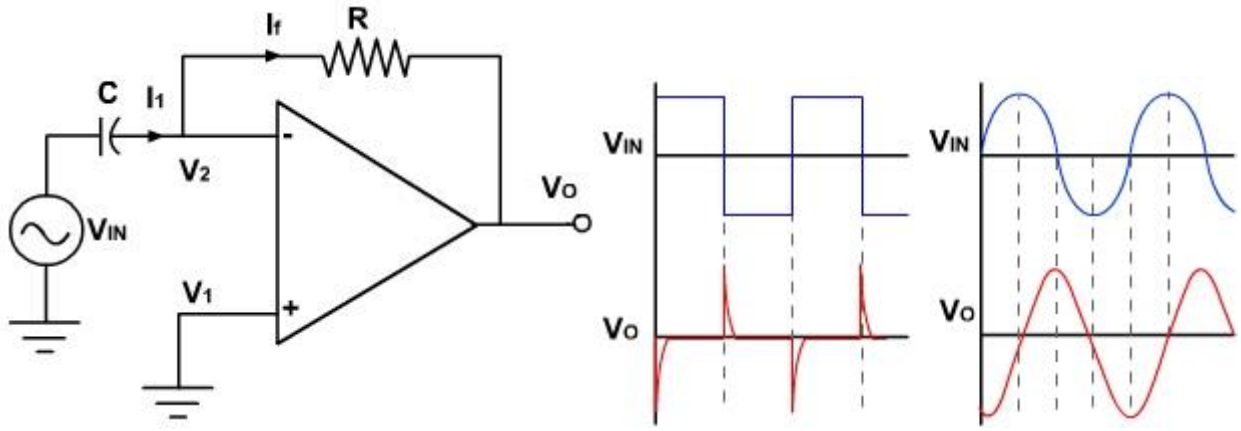


Fig. 5.19: A differentiator circuit and its output

The expression for the output voltage can be obtained from the Kirchoff's current equation written at node v2. $V_1 = V_2 = 0$ and $I_{in} = 0$

So, $I_1=I_f$

Therefore, $C\frac{d}{dt}(V_{in}-0)=\left(\frac{0-V_o}{R}\right)$

And, $V_o=-RC\left(\frac{dV_{in}}{dt}\right)$

Thus the output v_o is equal to the RC times the negative instantaneous rate of change of the input voltage v_{in} with time. A cosine wave input produces sine output. Fig.5.19 also shows the output waveform for square wave input voltages in which we get pulses at the output.

The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to R_f C. The differentiator circuit has problems of frequency dependent gain and higher noise level. As the frequency changes, the gain also changes. Also, at higher frequencies the circuit is highly susceptible at high frequency noise and noise gets amplified and circuit becomes unstable. Both the high frequency noise and frequency dependent gain can be corrected by shunting $R_f$with a small capacitor.

The other major problem of the basic circuit is that the input impedance is inverselyproportional to the input frequency. This is because $X_C$is the sole input impedance factor. This may present a problem at higher frequencies because the impedance will approach zero. To circumvent this problem, a resistor may be placed in series with the input capacitor in order to establish a minimum impedance value.

A practical differentiator circuit is shown Figure 5.20which can resolve the low input impedance, frequency dependent gain and higher noise problems.

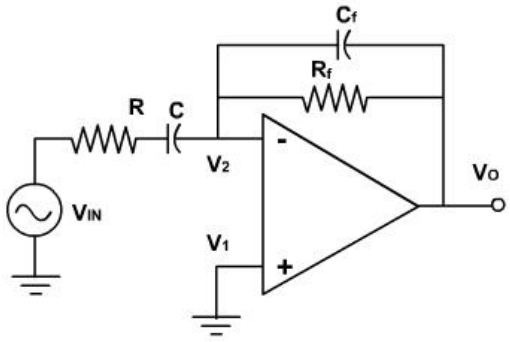


Fig. 5.20: A Practical differentiator circuit

5.11.2 Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is called integrator. Fig. 5.21shows an integrator circuit using OPAMP.

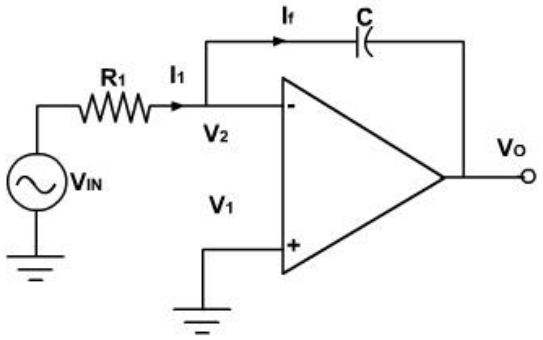


Fig. 5.21: AnIntegrator circuit

Here, the feedback element is a capacitor. The current drawn by OPAMP is zero and also the V_2 is virtually grounded.

Therefore, $i_1 = i_f$ and $V_2 = V_1 = 0$

$$\frac{(V_{in} - 0)}{R} = C\frac{d(0 - V_0)}{dt}$$

Integrating both sides with respect to time from 0 to t, we get

$$\int_0^t \frac{V_{in}}{R}\,dt = \int_0^t C\frac{d(-V_0)}{dt}\,dt$$

$$\int_0^t \frac{V_{in}}{R}\,dt = \int_0^t C\frac{d(-V_0)}{dt}\,dt = \int_{V_{at\ t=0}}^{V_o} d(-V_o)$$

If $V_{o\ at\ t=0}$ =0V, then

$$V_o = -\frac{1}{R_0}\int_0^t V_{in}\,dt$$

The output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant RC.

If the input is a sine wave the output will be cosine wave. If the input is a square wave, the output will be a triangular wave. For accurate integration, the time period of the input signal T must be longer than or equal to RC.

Fig. 5.22shows the output of integrator for square and sinusoidal inputs.

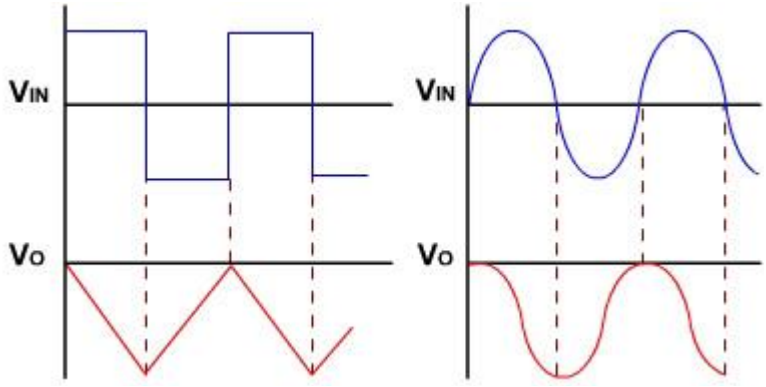


Fig. 5.22: input and output waveform of an Integrator circuit

5.12 ANALOG COMPUTERS

These Analog computers were developed to simulate the non-electrical systems such as mechanical, civil, etc. It was inexpensive to build an electrical equivalent of a complex mechanical system, to simulate its behavior. Engineers arrange a few operational amplifiers (op amps) and some passive linear components to form a circuit that follows the same equations as the mechanical system being simulated. All measurements can be taken directly with an oscilloscope.

In the electronic circuit, the simulated stiffness of the spring can be changed easily by adjusting the parameters of an integrator in comparison to change stiffness of the spring in mechanical prototype.So, The electrical analogy of the physical system were used to simulate physical system on analog computer because it is much less expensive, much easier to modify, and generally saferthan a mechanical prototype. Further, the electronic circuit can also be made to run faster or slower than the physical system being simulated and they offer a comparatively intimate control and understanding of the problem.

Electronic analog computers typically have front panels with numerous jacks (single-contact sockets) that permit patch cords (flexible wires with plugs at both ends) to create the interconnections that define the problem setup. In addition, there are precision high-resolution potentiometers (variable resistors) for setting up (and, when needed, varying) scale factors. In addition, there is usually a zero-center analog pointer-type meter for modest-accuracy voltage measurement. Stable, accurate voltage sources provide known magnitudes.

Typical electronic analog computers contain hundredsof operational amplifiers ("op amps"), named because they perform mathematical operations. Many mathematical functions such as addition, subtraction, log, antilog, integration, differentiation etc. were implemented using Op amps. They Op-amps are always used with precision feedback components that, in operation, all but cancel out the currents arriving from input components. The majority of op amps in a representative setup are summing amplifiers, which add and subtract analog voltages, providing the result at their output jacks. As well, op amps with capacitor feedback are usually included in a

setup; they integrate the sum of their inputs with respect to time.Other computing elements include analog multipliers, nonlinear function generators, and analog comparators.

Electrical elements such as inductors and capacitors used in electrical analog computers had to be carefully manufactured to reduce non-ideal effects. The use of electrical properties in analog computers means that calculations are normally performed in real time (or faster), at a speed determined mostly by the frequency response of the operational amplifiers and other computing elements.

Nonlinear functions and calculations can be constructed to a limited precision (three or four digits) by designing function generators—special circuits of various combinations of resistors and diodes to provide the nonlinearity. Typically, as the input voltage increases, progressively more diodes conduct.

When compensated for temperature, the forward voltage drop of a transistor's base-emitter junction can provide a usably accurate logarithmic or exponential function. Op amps scale the output voltage so that it is usable with the rest of the computer. Any physical process that models some computation can be interpreted as an analog computer.

Many small computers dedicated to specific computations are still part of industrial regulation equipment, but from the 1950s to the 1970s, general-purpose analog computers were the only systems fast enough for real time simulation of dynamic systems,especially in the aircraft, military and aerospace field.

5.13 WAVE SHAPER

A **clamper** is an electronic circuit that produces an output, which is similar to the input but with a shift in the DC level. In other words, the output of a clamper is an exact replica of the input. Hence, the peak to peak amplitude of the output of a clamper will be always equal to that of the input. Clampers are intelligent in that they can adjust the amount of DC if the peak value of the input signal changes.

Clampers are used to introduce or restore the DC level of input signal at the output. There are **two types** of op-amp based clampers based on the DC shift of the input.

- Positive Clamper
- Negative Clamper

5.13.1 Positive Clamper

Figure 5.23 shows an active positive clamper. On the first negative going peak of the input, the inverting input of the op amp to go slightly negative, thus creating a positive op amp outputand diode D will operate in forward bias. Thus a charging current flow to the capacitor until the capacitor will charge to the negative peak value of the input.

Whenthe input signal is positive, the op amp will produce a negative output, thus turning off the diode and effectively removing the op amp from the circuit. Because the discharge time for *C* is much longer than the input period, its potential stays at roughly *Vp*-. It now acts like a voltage source. These two sources add, so we can see that the output must be:

Vout=Vin+|Vp|

The op amp will remain in saturation until the next negative peak, at which point the capacitor will be recharged. During the charging period, the feedback loop is closed,and thus, the diode's forward drop is compensated for by the op amp. In order to make a negative clamper, just reverse the polarity of the diode.

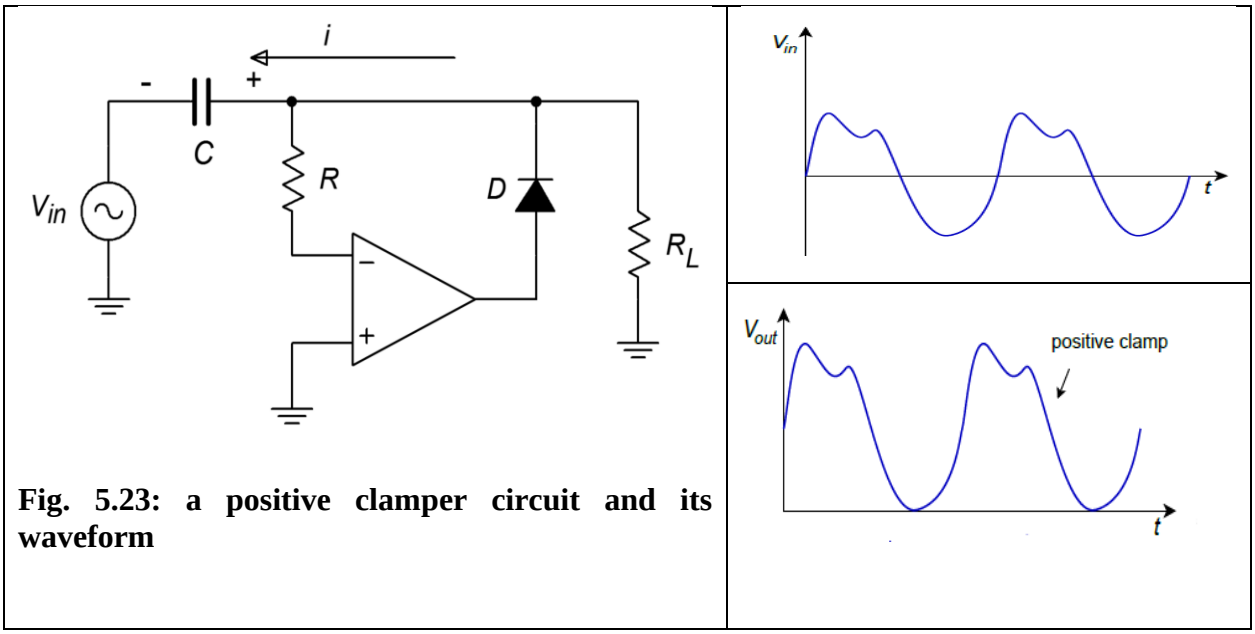


Fig. 5.23: a positive clamper circuit and its waveform

5.13.2 Negative Clamper

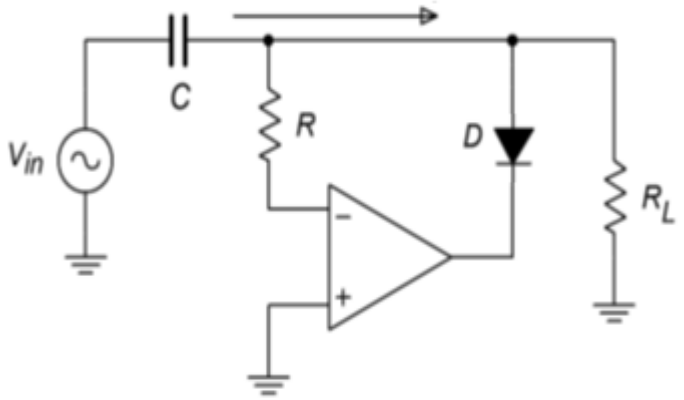
Figure 5.24 shows an active negative clamper with input and output waveform. On the first positive going peak of the input, the inverting input of the op amp to go slightly positive, thus creating a negative op amp outputand diode D will operate in forward bias. Thus a charging current flow to the capacitor until the capacitor will charge to the positive peak value of the input.

Whenthe input signal is negative, the op amp will produce a positive output, thus turning off the diode and effectively removing the op amp from the circuit. Because the discharge time for *C* is

much longer than the input period, its potential stays at roughly *Vp*. It now acts like a voltage source. These two sources add, so we can see that the output must be:

Vout=Vin-|Vp|

The op amp will remain in saturation until the next positive peak, at which point the capacitor will be recharged. During the charging period, the feedback loop is closed,and thus, the diode's forward drop is compensated for by the op amp.



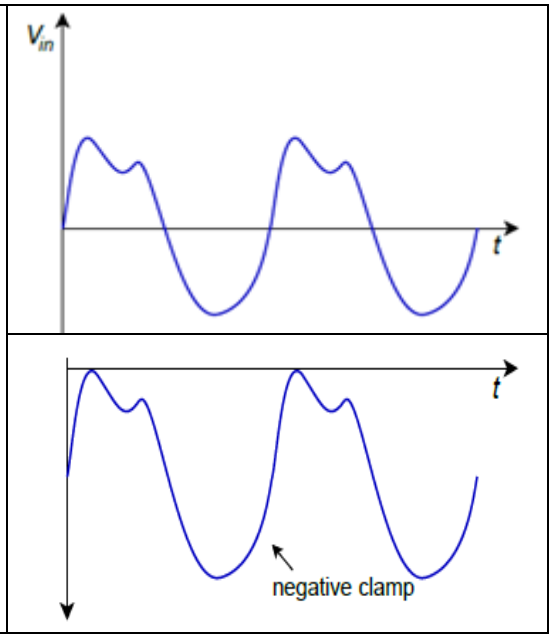


Fig. 5.24: a negative clamper circuit and its waveform

5.14 EXAMPLES

Example 1: What are the input impedance and gain of the circuit in Figure 5.25?Assume op-amp is ideal.

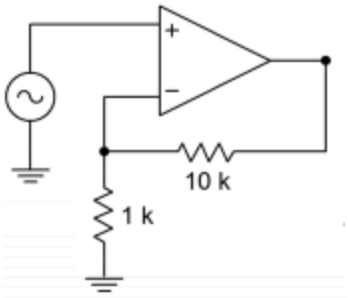


Figure 5.25

Solution: as the op-amp is ideal and input is connected to non-inverting terminal. Input impedance Zin is infinite

Now, for the gain: the configuration is non-inverting, negative feedback amplifier.
So, gain

$$\text{Av} = \left(1 + \frac{R_f}{R_1}\right)$$

put R_f=10k and R_1=1k
so, Av=11.

Example 2: Determine the output voltage for input voltage of 100mV connected to an inverting terminal of closed loop inverting amplifier with R_f=20k and R_1=5k.

Solution: The output voltage of an inverting amplifier is given by

$$\text{Vo} = -\left(\frac{R_f}{R_1} V_{in}\right)$$

Putting the values, we get

$$\text{Vo} = -\left(\frac{20k}{5k} * 100mV\right) = -400mV$$

Example 3: What is the output of the summing amplifier in Figure 5.26, with the given DC input voltages?

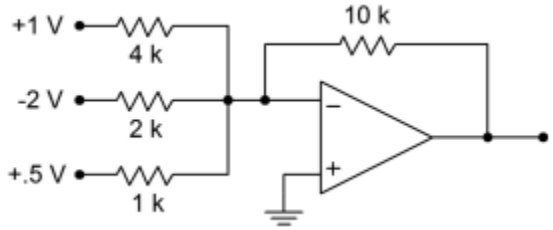


Figure 5.26

Solution: The circuit is inverting summing amplifier. Here three input voltage sources are applied.

First voltage source is V1= +1V with resistance R1=4K.

Second voltage source is V2= -2V with resistance R2=2K.

Third voltage source is V3= +0.5V with resistance R3=1K and, feedback resistance R_f=10 K.

Output for the inverting summing amplifier is

$$\text{Vo} = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$$

Putting the values,

$$\text{Vo} = -\left(\frac{10k}{4k}\ 1V + \frac{10k}{2k}(-2V) + \frac{10k}{1k}\ 0.5V\right)$$

We get, Vo = 2.5V

The output voltage is 2.5V.

Example 4: Sketch the output waveform for the circuit of Figure 5.27, if the input signal is a 5 V peak sine wave. (Given maximum output voltage swing is ±13V)

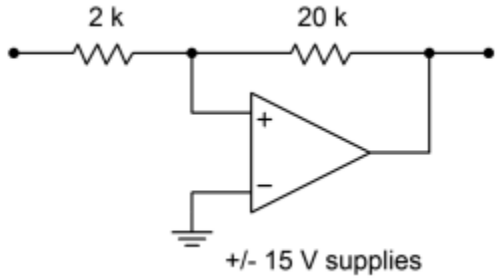


Figure 5.27

Solution: First, determine the upper and lower threshold voltages.

$V_{UTH} = \left(\frac{R_2}{R_1}\right) V_{sat}$ and $V_{LTH} = -\left(\frac{R_2}{R_1}\right) V_{sat}$

Putting the values , we get V_{UTH} =1.3 V and V_{LTH} = -1.3 V

So, The output will go to +13 V when the input exceeds +1.3 V and will go to −13 V when the input drops to −1.3 V. The input/output waveform sketches are shown in Figure 5.28.

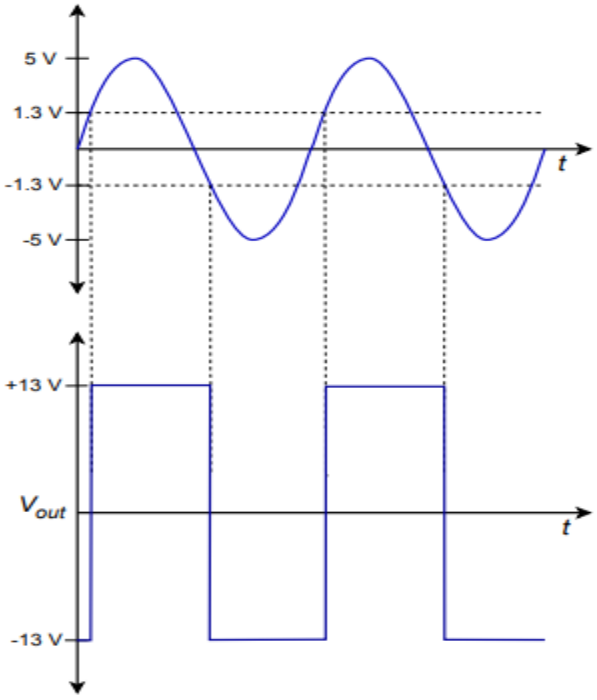


Figure 5.28

Example 5: Determine the output voltage for the circuit of **Figure 5.29,**if Vin = 1 V, Ri = 50 kΩ, and Is = 30 nA. Assume T = 300 kelvin. Also, determine the output for inputs of 0.5 V and 2 V.

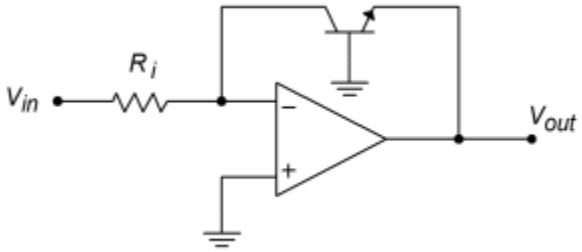


Figure 5.29

Solution: For Vin = 1V

$$V_{out} = 25.9 \times 10^{-3} ln\left(\frac{V_{in}}{R_i I_s}\right)$$

$V_{out} = 25.9 \times 10^{-3} ln\left(\frac{1}{50k \times 30nA}\right)$ = -0.1686V

For Vin = 0.5 V

$V_{out} = 25.9 \times 10^{-3} ln\left(\frac{0.5}{50k \times 30nA}\right)$ = -0.1504V

For Vin = 2.0 V

$V_{out} = 25.9 \times 10^{-3} ln\left(\frac{2}{50k \times 30nA}\right)$ = -0.1864V

Notice that for each doubling of the input signal, the output signal went up a constant 18 mV. Such is the nature of a log amplifier.

Example 6: Determine the equation for *Vout*, and the lower frequency limit of integration for the circuit of Figure 5.30

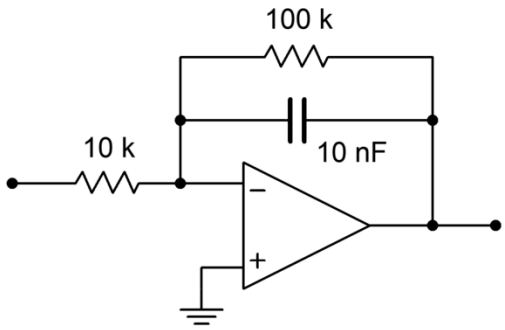


Figure 5.30

Solution: The general form of the output equation is given by

$$V_{out} = -\frac{1}{R_i C}\int V_{in}(t)dt$$

$V_{out} = -\frac{1}{10k \times 10nF}\int V_{in}(t)dt = -10^4 \int V_{in}(t)dt$

The lower limit of integration is set by f_{low}

$f_{low} = (1/2\pi)R_f C = (1/ 2\pi)100\ k\times 10\ nF$

f_{low}=159Hz

This represents our 50% accuracy point. For 99% accuracy, the input frequency should be at least one decade above *flow*, or 1.59 kHz. Accurate integration will continue to higher and higher frequencies.

5.15PROBLEMS

Review questions

(a)What is virtual ground?

(b)What are the advantages of active rectifiers versus passive rectifiers?

(c)What are the disadvantages of active rectifiers versus passive rectifiers?

(d)What is a peak detector?

(e)What is a limiter?

(f)What is the function of a clamper?

(g)What are the differences between active and passive clampers?

(h) What is a Schmitt trigger?

(i) What is the advantage of a Schmitt-type comparator versus an ordinary open-loop op amp comparator?

(j) How are log and anti-log amplifiers formed?

(k) What is the effect of passing a signal through a log or anti-log amplifier?

(l) What is a four-quadrant multiplier?

(m) What is the basic function of an integrator?

(n) What is the basic function of a differentiator?

(o) What is the function of the capacitor in the basic integrator and differentiator?

(p) Why are capacitors used in favor of inductors?

(q) What practical modifications need to be done to the basic integrator, and why?

(r) What practical modifications need to be done to the basic differentiator, and why?

(s) What are the negative side effects of the practical versus basic integrator and differentiator?

(t) What is an analog computer, and what is it used for?

(u) What are some of the advantages and disadvantages of the analog computer versus the digital computer?

(v) How might integrators and differentiators be used as wave-shaping circuits?

Analysis Problems

P1. Determine the voltage gain of (i) Ist stage (ii) IInd Stage and (iii) overall gain of the system in fig. 5.31.

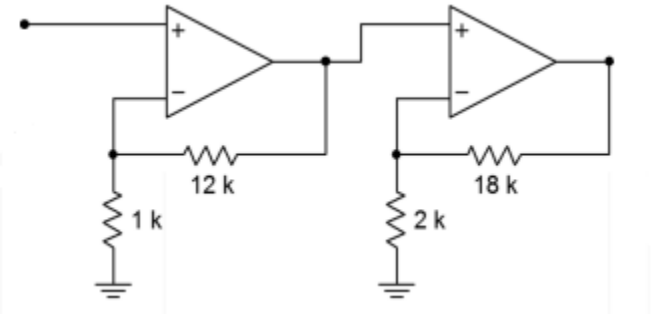


Figure 5.31

P2. If the differential input signal is 300 mV in Figure P5.32, what is Vout?

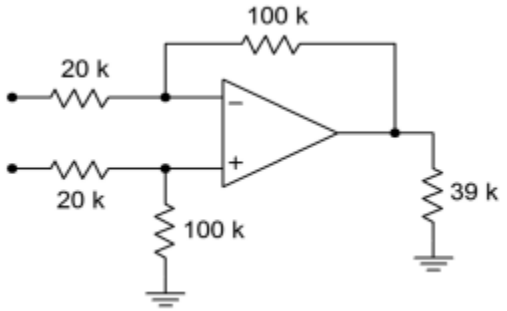


Figure P5.32

P3. Sketch the output waveform for the circuit ofFigure P5.33, if (i) the input is a 4 V peak square wave at 1 kHz. (ii) *Vin (t) = 5 sin 2π318t*. (iii) *Vin (t) = 20 cos 2π1000t*.

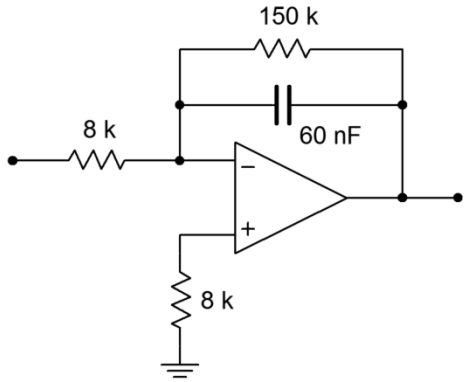


Figure P5.33

P4. For the Figure P5.34 (i) determine the low frequency gain for the circuit and (ii) determine *Vout*If *C* = 33 nF and *Vin* is a 200 mV peak sine wave at 50 kHz.

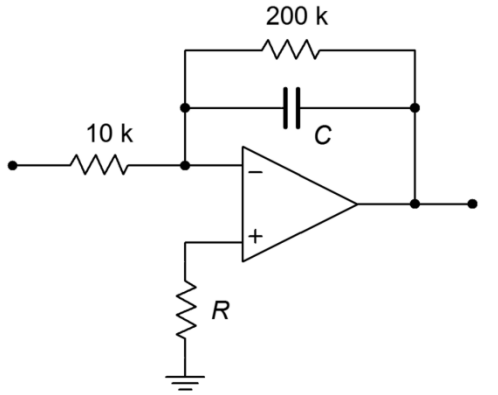


Figure P5.34

P5. If *R1* = 10 kΩ and *R2* = 33 kΩ in Figure P5.35, determine the upper and lower thresholds if the power supplies are ±15 V.

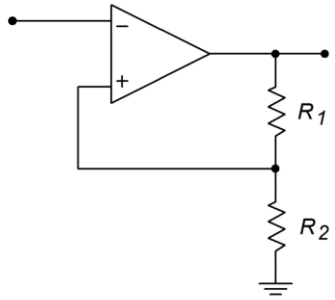


Figure P5.35

P6. Determine the upper and lower thresholds for Figure P5.36, if *R1* = 4.7 kΩ and *R2* = 2.2 kΩ, with ±12 V
power supplies.

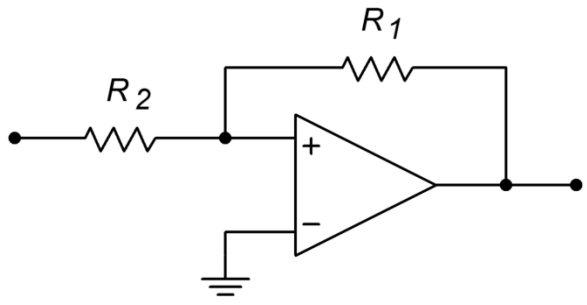


Figure P5.36
P7. Given the circuit in Figure P5.37, sketch its transfer curve.

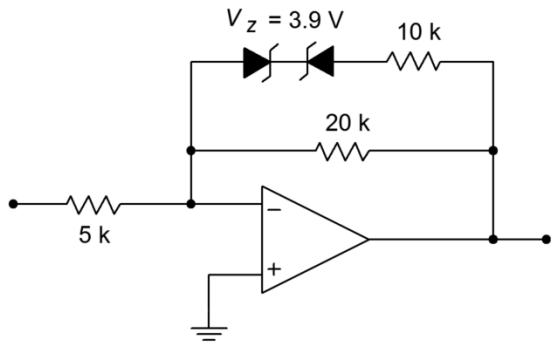


Figure P5.37

P8. Determine *Vout*in Figure P5.38 if *Vin*+ = +20 mV DC and *Vin*- = −10 mV DC.

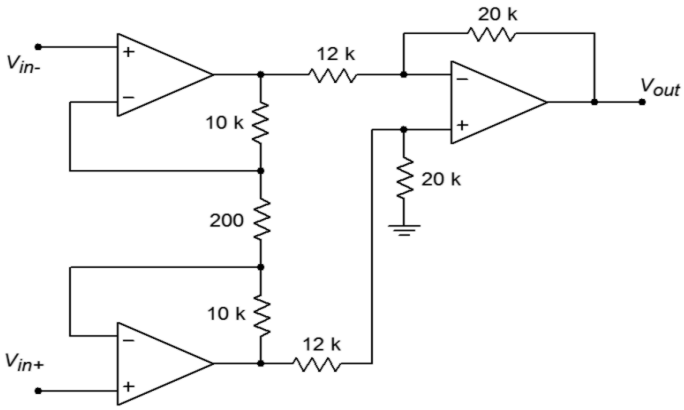


Figure P5.38

P9. A three-stage amplifier uses identical noninverting voltage stages with gains of 10 each. If the op amps used have an*f*unity*f* of 4 MHz, what is the system gain and upper break?

P10. What is the system input impedance in Figure P5.39? What is the system gain?

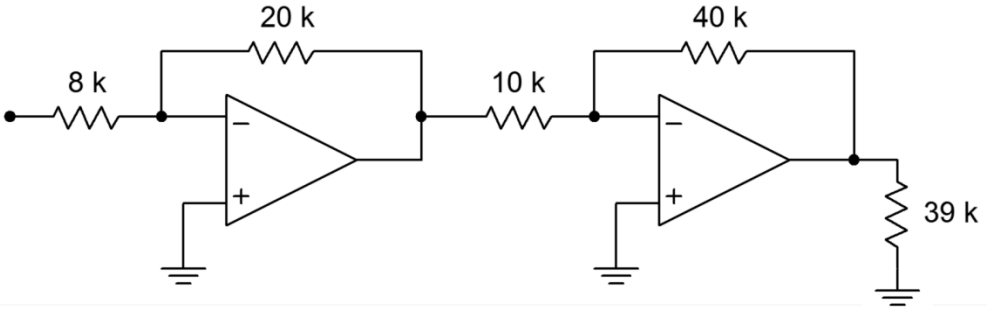


Figure P5.39

UNIT-6: APPLICATION OF OPERATIONAL AMPLIFIER

Contents

6.1. Objectives

After finishing this chapter students will be able to know

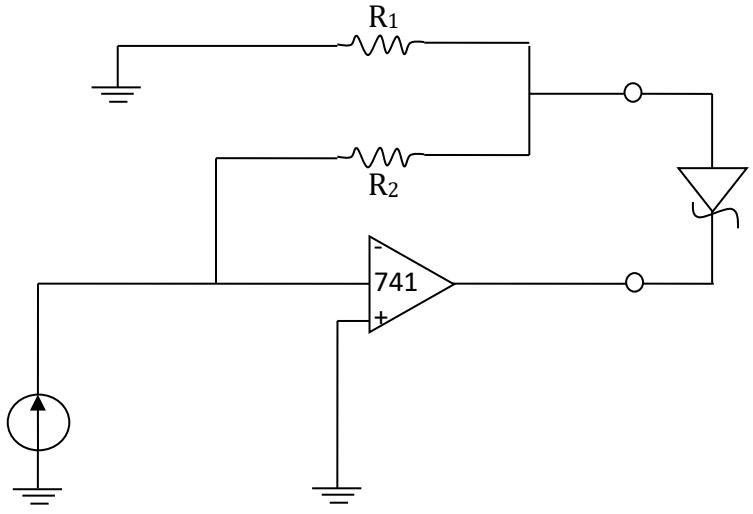
- High resistance DC voltmeter using Op-Amp.
- Universal high resistance voltmeter.
- LED tester 741Op-Amp.
- Current amplifier using Op-Amp.
- Phase shifter using Op-Amp.

6.2 INTRODUCTION

An operational amplifier, or Op-Amp, is a very high gain differential amplifier with high input impedance and low output impedance. In this chapter we will go through some advance applications of Op-Amp such as Current amplifier, Phase shifter, high input impedance, Universal high impedance Voltmeter and LED Tester.

6.3 Current amplifier using Operational Amplifiers

A current amplifier circuit is a circuit which amplifies the input current by a fixed factor and feeds it to the succeeding circuit. A current amplifier is somewhat similar to a voltage buffer but the difference is that an ideal voltage buffer will try to deliver whatever current
required by the load while keeping the input and output voltages same, where a current amplifier supplies the succeeding stage with a current that is a fixed multiple of the input current.



Figure(6.1) current amplifier

6.4 Phase Shift Circuits

The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called constant-delay filters or all-pass filters. That constant delay refers to the fact the tile difference between input remains constant when frequency is changed over a range of operating frequencies.

This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles.

Phase-lag circuit:

Phase log circuit is constructed using an op-amp, connected in both inverting and non inverting modes. To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at(-)terminal of op-amp and a non inverting amplifier with a low-pass filter.

It is also assumed that inverting gain is -1 and non-inverting gain after the low-pass circuit is

$1 + \frac{R_f}{R} = 1 + 1 = 2$ Since $R_f = R_1$.

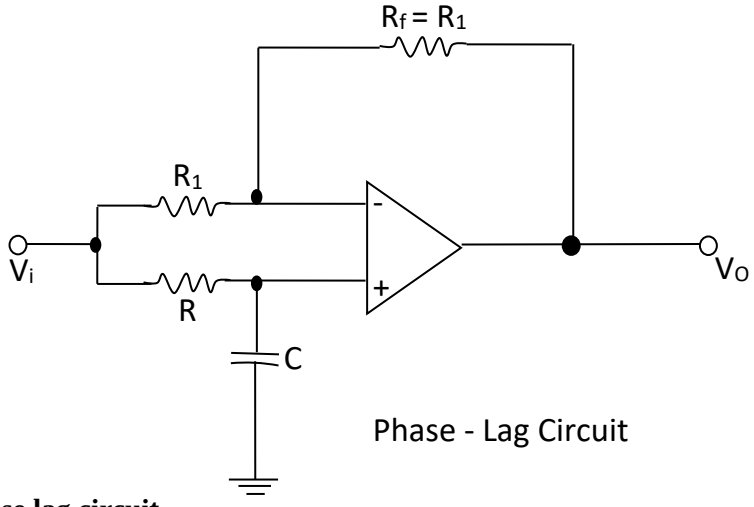


Fig. 6.2 Phase lag circuit

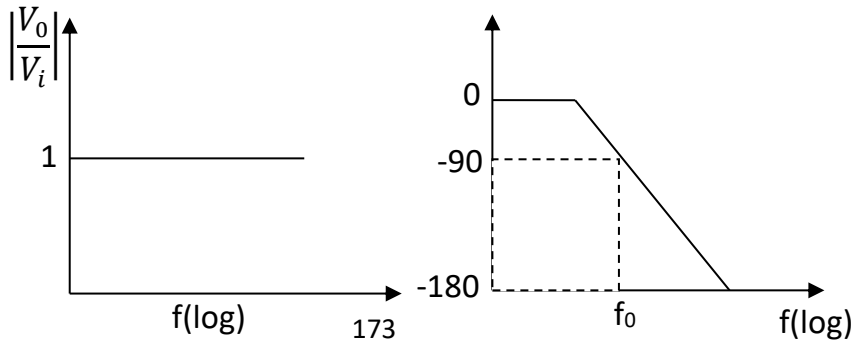


Fig. 6.3 Bode plot of phase lag circuit

For the circuit fig. 6.2, it can be written as $V_0(jw) = -V_i(jw)\left(-1 + \frac{2}{1+jwRC}\right)$ and the relationship between output and input can be expressed by $\frac{V_0(jw)}{V_i(jw)} = \frac{(1-jwRC)}{(1+jwRC)}$.

The relationship is complex as defined above equation and it shows that it has both magnitude and phase. Since the numerator and denominator are complex conjugates, their magnitudes are identical and the overall phase angle equals the angle of numerator less the angle of the denominator.

Phase-lead circuit:

$$\theta = -2\tan^{-1} RC\omega$$

$$\frac{V_0(jw)}{V_i(jw)} = \frac{(1-jwRC)}{(1+jwRC)}$$

$$\theta = 180^o - 2\tan^{-1} RC\omega$$

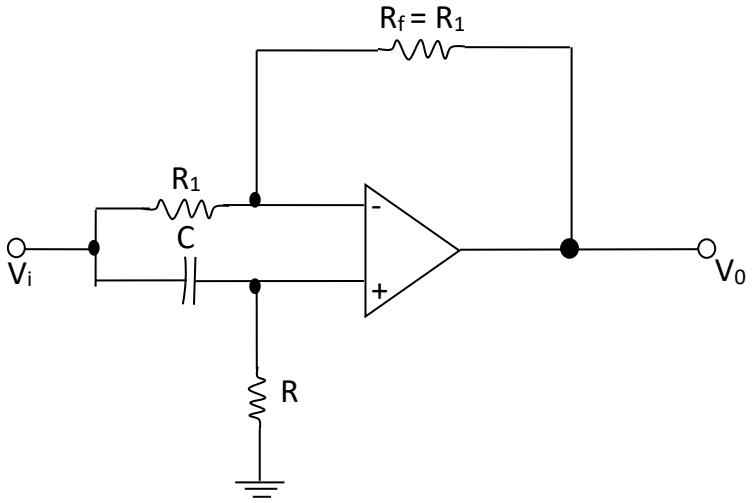


Fig. 6.4 Bode plot of Phase lead circuit

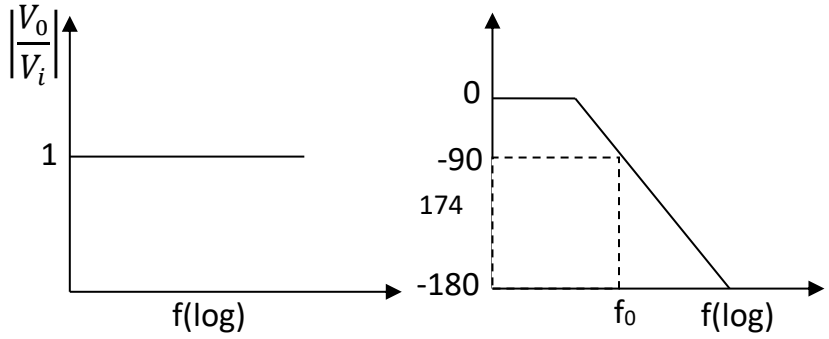


Fig. 6.5 Bode plot of Phase lead circuit

6.6 High Impedance DC Voltmeter using MOS Op-Amp

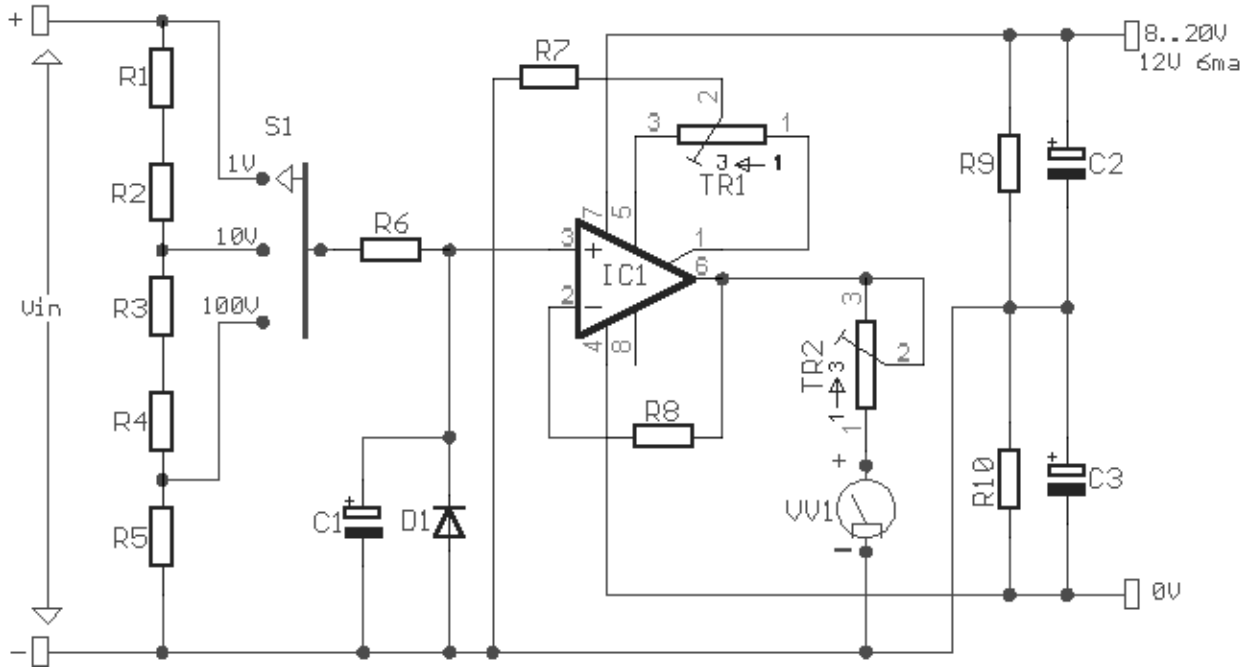


Figure 6.7: HIGH IMPEDANCE DC-VOLTMETER

The circuit was designed for the purpose of creating a voltmeter with high impedance that would measure Direct Current voltages across any types of circuits.

- CA3130 - a BiMOS operational amplifier that combines the advantage of both bipolar transistor and CMOS, which can be used in photodiode sensor amplifiers, peak detectors, single-supply full wave precision rectifiers, voltage regulators and followers, high input impedance comparators and wideband amplifiers, long duration timers, fast sample-hold amplifiers, and ground referenced single supply amplifiers.

- Voltmeter- a device or an instrument used for measuring the electrical potential difference between two points of either alternating current or direct current electric circuit.
- Impedance - a measure of the total opposition to the flow of time-varying and alternating current in a circuit, which consists of resistance and reactance.
- Metal Oxide Semiconductor Field Effect Transistor (MOSFET) - a device utilized for switching and amplification of signals.

The use of CA3130 is suitable for dealing with DC voltmeters with high impedance because of its MOSFET input. The range by which the circuit measures is dictated by the use of selector switch S_1. The presence of the resistor in the voltage divider part of the circuit limits the input impedance to 10M ohms. This is still considered as an acceptable value. The mechanical instrument should have a rating of 100 µA, before the initial switch ON of the device. The pointer should be placed below the scale of zero and this requires the mentioned adjustment procedure.

Upon switching ON the unit, the input is kept shorted while obtaining an exact zero indication which is done by adjusting the trimmer TR_1. For the full scale deflection in three ranges 1V, 10V and 100V, the calibration of voltages is performed by the trimmer TR_2. The voltage supply may be between 8V to 20V since the consumption of current in a 12Vsupply is less than 6mA. The quality of 100 µA instrument is very essential since the voltmeter is highly dependent on it along with the precise calibration done on the unit.

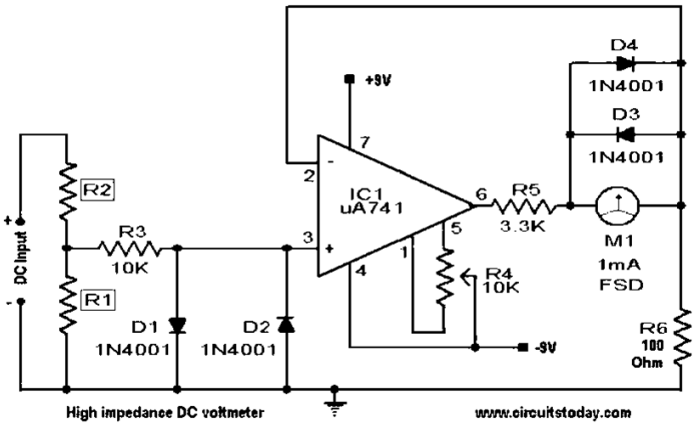
R1=8.2Mohms	R7=1Kohms	C2-3=10uF 25V
R2-3=820Kohms	R9-10=10Kohms	D1=1N4148
R4=82Kohms	TR1=10Kohms trimmer	IC1=CA3130
R5=100Kohms	TR2=25Kohms trimmer	VV1=100uA instrument
R6-8=47Kohms	C1=1.5uF 25V	

DC voltmeter can be used as equipment for professional grade automotive test where it covers the testing of electrical components and circuits that normally found in industrial and marine engines, trucks, automobiles, and other low voltage DC applications. During the measurement, they are being connected in parallel across the component being measured with the black probe typically connected to the negative terminal while the red probe to the positive side of the component.

Sources: DC Voltmeter with high impedance
Cell Phone Detector
PIC and EEPROM Programmer
300 Watt MOSFET Real HI-FI Power Amplifier
RSA Supported Credit Card Payment System

6.6 (a)High impedance DC voltmeter(Alternate Circuit)

A high impedance DC voltmeter using a uA741 IC is shown here. The operational amplifier is used as a non-inverting DC amplifier in which the negative feedback is through a DC meter requiring 1mA for full scale deflection. Since R6 is 100 Ohms, the meter will show full scale reading when the DC input voltage to pin3 is equal to the voltage drop across R6, viz 0.1 volts. Choice of R1 and R2 for getting different voltage ranges are shown in the table. The diodes D1 and D2 protect the IC from accidental excessive input voltages and diodes D3 and D4 protect the meter from overloads.



Spice simulation:

Following steps have to make:

- Assemble the circuit on good quality PCB or common board.
- Mount the IC on a holder.
- The circuit can be powered from a +9V/-9V dual power supply.
- The meter M1 can be a 1mA FSD DC ammeter.
- The values of R1 & R2 for different voltage ranges can be obtained from the table given below.

  Values of R1 ,R2 and the corresponding ranges.

R1	R2	Full scale voltage
100K	900K	1V
100K	10M	10V
10K	10M	100V

6.7 Universal High Resistance DC Voltmeter

The full-scale deflection of the universal high-input-resistance voltmeter circuit shown in the figure depends on the function switch position as follows:

(a) 5V DC on position 1

(b) 5V AC rms in position 2

(c) 5V peak AC in position 3

(d) 5V AC peak-to-peak in position 4

The circuit is basically a voltage-to-current converter.

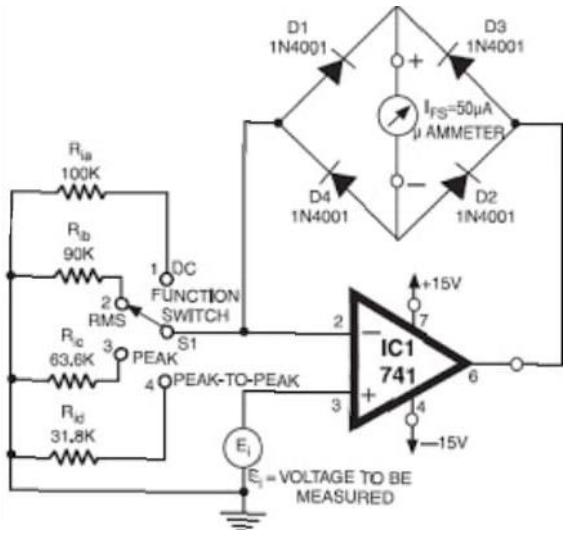


Figure 6.6: Universal High Resistance DC Voltmeter

6.5 Operational Amplifier 741 Tester

The op-amp IC 741 is a DC-coupled, high gain differential amplifier with external negative feedback. IC 741 is characterized by almost infinite open loop gain (100,000), almost infinite input impedance (2MΩ) and almost zero output impedance (75Ω). IC 741 is most popular, cheap and

easy to use op-amp. Various type of circuit is designed using Op-amp 741 out of which some are voltage follower, current to voltage converter and vice versa, summing amplifier etc.

Various type of circuit based on op-amp 741 have already described in previous chapter op-amp section. Now here is a simple circuit operational amplifier 741 tester which test op-amp 741 either is good or fault.

Circuit Description of Operational Amplifier 741 Tester

The circuit of operational amplifier 741 tester comprises two diode and very few passive components and a 741 IC to be test. All the components are connected as shown in circuit diagram. A LED_1 is used to indicate either IC is good or fault. Blinking LED_1 indicate IC is good.

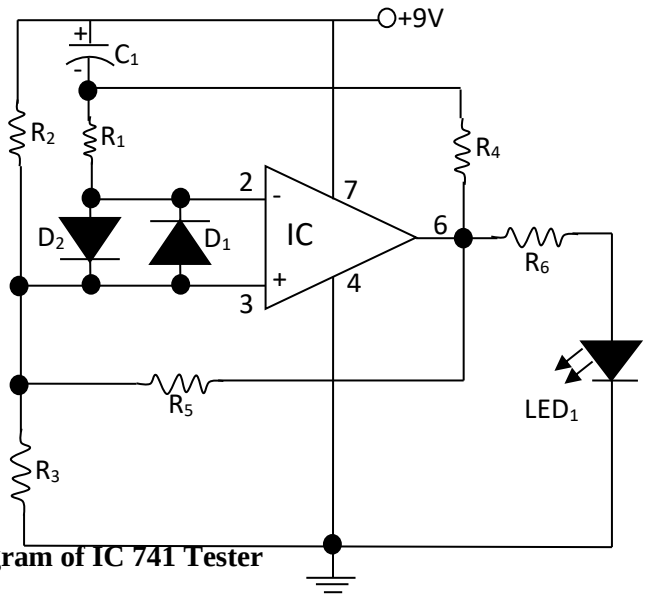


Figure 6.6: Circuit Diagram of IC 741 Tester

Working of the circuit/Operational Amplifier 741 Tester

Working of the circuit is simple and straight forward. The IC to be tested is configured in voltage comparator mode. Voltage at pin 3 (non inverting pin) is fixed where voltage at pin 2 (inverting pin) varying due to charging and discharging of capacitor C1. Where battery is connected to the circuit the voltage at pin 3 is high in compare to voltage at pin 2 due to charging of capacitor, as a result output of IC become high and LED start to glow.

At this instant capacitor start to charge through the resistor R4. When charge (voltage) of capacitor exceed voltage at inverting pin (pin 2), the output of IC become LOW, as a result LED stop to glow. When voltage at capacitor become higher then inverting input pin it start to discharge and again output of IC become high. This high and low output of IC generate square wave and Cause LED to blink.

NOTE: If the LED doesn't blink in fixed interval of time i.e. either stay ON or OFF, the IC which is testing is faulty.

4.8 Worked Example:

1) **What forms of feedback are used for the inverting and non-inverting voltage amplifiers?**
   The inverting forms used a modified parallel scheme whereas the non-inverting form uses series-parallel negative feedback.
3) **What form of feedback is used for the inverting current amplifier?**
   Parallel- series feedback is used in the inverting current amplifier.
5) **What is a virtual ground?**
   A virtual ground is a point that is very close to 0 volts. It is normally found at the inverting input of parallel-input feedback forms and behaves as an ideal current summing node.
7) **How can output current by increased?**
   Output current can be increased by adding a discrete B follower stage after the op amp and wrapping it inside of the feedback loop. The op amp delivers current to the follower, which is then responsible delivering final load current.
9) **What operational parameters change when a circuit is set up for single supply blasing?**
   All Parameters stay unchanged with the exception of the system input impedance (set by the input divider network), low frequency response (set by coupling and feedback capacitiors), and the current drawn (additional draw through the bias network).
11) **What is meant by the term "Floating load"?**
   A floating load is one that is not tied to ground at one end.
1) **Define Gain-Bandwidth product. What is its use?**
   Gain-Bandwidth product is also known as f…. and is defined as the frequency at which the open-loop response falls to unity (0dB). It is useful because the product of closed-loop noise gain and f1 must equal f…… It can be seen, therefore, that gain can be traded for bandwidth and vice-verse.
3) **What happens if two or more stages share the same break frequency?**
   For lower breaks, the combination will produce an f2 higher than the individual break frequencies. For upper breaks, combination will produce an f2 lower than the individual break frequencies.
5) **How is power bandwidth determined?**
   Power bandwidth (f……) is proportional to slew rate and inversely proportional to peak sine amplitude. f….- Slew Rate/(2aV……).
7) **What are the advantages and disadvantages of non-compensated op amps?**

On the down side, non-compensated amplifiers require external compensation circuits (a capacitor at minimum). The advantage is that the frequency response and slew rate can be optimized for a given gain

9) What causes DC offset voltage?

Output offset voltage is caused by less-than-perfect matching of the internal components if the op amp, as well as in the surrounding feedback network.

11) What is CMRR?

CMRR stands for Common Mode Rejection Ratio. It is a measure of how well the op amp suppresses identical signals on the inputs relative to differential input signals.

13) What parameters describe an op amps noke performance?

In general, noise is proportional to temperature, boundwidth and resistance. The key parameters to look for on an op amp's data sheet are the input noise voltage density and input noise current density.

1) What are the advantages of using instrumentation amplifiers versus a simple op amp simple differential amplifier?

Instrumentation amplifiers generally offer very high gain, isolated high input impedances for both inputs, and superior common-mode rejection when compared to a single op amp based differential amplifier.

3) What are the advantages of using programmable op amps?

The device is able to go into a “power down” or “sleep” mode and thereby drastically reduce power consumption. Further, the performance can be fine-tuned against power consumption.

5) Give at least two applications for a high-power op amp.

Direct motor drive and audio power amplifiers.

7) What is an OTA?

OTA stand for Operational TransconductnnceAmplifier. The transconductannce(and hence the gain) of the device is set by an external control current. IABC’

9) Give an application that might use an OTA.

Any application requiring a controlled-gain amplifier would suffice, such as an audio compressor.

11) Describe how a Norton amplifier achieves input differencing.

Input differencing is achieved through the use of a current mirror. The input circuit generates the difference between the input currents by subtracting the current presented so one input (via the current mirror) from the other input current.

13) Explain why a current feedback amplifier does not suffer from the same gain band width limitations that ordinary op amps do.

The construction of current feedback amplifier differ considileabry from that of an ordinary op amp. The current feedback amplifier does not rely or negative feedback to maintain its inverting or non-inverting inputs at the same level; rather a unity gain buffer is used. Also the output also factor O

1) What are the advantages of active rectifiers versus passive rectifiers?

Active rectifiers have the primary advantage of accurately rectifying small signal levels. They also exhibit a high input impedance and a low output impedance.

3) What is a peak detector?

A peal detector produces an output that is proportional to the peak value of the input waveform. It can be used as an envelope detector in AM systems.

5) What is the function of a clamper?

A clamper adds or subtracts a DC potential to an input signal in order to shift it to a new level, for example, making the entire waveform positive by shifting it up.

7) What is a transfer function generator circuit, and what is its use?

A transfer function generator has an arbitrary input output function curve. In comparison, the function for an amplifier is a straight line (the slope of which indicates the gain). Function generation circuits can be used to create some desired transfer characteristic or to pre-distort or compensate for nonlinearities that exist elsewhere, creating an overall linear system response.

9) What is a Schmitt trigger?

A Schmitt trigger is a comparator with hysteresis. In effect there are different threshold levels depending on the current output state. The circuit winds up being relatively immune to generating false outputs due to input noise.

11) What are the advantages of dedicated comparators such as the I.M311 versus ordinary op amp comparators?

Dedicated comparators are usually designed to produce very fast switching times. Further, external connections are usually available for logic interfacing, strobe, and so forth.

13) What is the effect of passing a signal through a log or anti-log amplifier?

A log amplifier produces an output signal that is proportional to the log of the input. This has the effect of compressing the signal. In contrast, the anti-log amplifier produces a signal that is proportional to the anti-log of the input, producing an expansion of the input signal.

1) What is the basic function of an integration?

Integration find the "area under the curve" of the input waveform.

3) What is the function of the capacitor in the basic integrator and differentiator?

The capacitor has a differential characteristic between voltage and current, i-C *dv/dt*. When placed in the feedback loop, this gives rise to the differential (C as R_i) or the integral (C as R_i) of the input.

5) What practical modifications need to be done to the basic integrator, and why?

The basic integrator has very high DC gain and will eventually saturate due to offsets. For this reason, a lower gain limit is imposed. This has the side effect of producing a lower frequency limit of accurate integration.

7) What are the negative side effects of the practical versus basic integrator and differentiator?

Primarily the additional components reduce the range of frequencies that can be accurately processed. In the case of the integrator, a lower limit is created, and in the case of the differeniator, an upper limit is established.

9) What are some of the advantages and disadvantages of the analog computer versus the digital computer?

One advantage of the analog computer is its immediacy: a technician or engineer can "tweak the knobs" in realtime if desired. An advantage of using a digital computer is its accuracy and repeatability.

4.9 Summary: In this chapter we have discussed about some advance applications of Op-Amp. We have lernt about Current amplifier, Phase lead and phase lag circuits, DC voltmeterand Universal high resistance voltmeter and LED tester to test either a given Op-Amp is in working condition or not?. Things are so vast the readers are suggested that to follow reference books at the reference section for further study.

4.10 Modal Questions

1- Describe the working of a current amplifier
2- Compare the high impedennce DC voltmeter and Universal high impedance voltmeter
3- Differentiate between phase lead circuit and phase lag circuit.
4- Draw circuit diagram for LED op-amp tester and describe its working also.

4.11References and further readings

- **Linear integrated Circuit by D Roy Choudhary**
- **Introduction of Operational Amplifier and circuit theory by Boylstad**

UNIT 7: INTEGRATED CIRCUIT TECHNOLOGY

Outline of unit7

7.1 Objectives

After study of this unit, the student should be able to:

1. Describe the importance of integrated circuits (ICs).
2. Categorize the major components of an integrated circuit.
3. To understand the photolithography
4. To understand the metal-semiconductor interface
5. To understand the charge coupled devices
6. Identify advantages and disadvantages of integrated circuits.

7.2 Introduction

An integrated circuit (IC) is a collection of electronic circuits packaged into a single compact flat piece known as a "chip". Semiconducting materials (such as silicon)are used to make the chip. The following points about ICs are worth noting:

1. An IC is quite compact.
2. No IC components can be seen rising above the chip's surface.
3. Individual components in an IC are automatically integrated into a compact semiconductor chip, and they cannot be removed or replaced.

Chip with the same electronics parameters have various IC packaging. IC packaging specifies the shapes and dimensions of the chips, Various types of IC packaging are used for integrated circuits to protect them from the outside environment and to provide mechanical protection.ICpackages are of two types: (i) Hermite (Metal or ceramic with glass) (ii) Non-Hermite (Plastics)as shown in figure 7.1. Non Hermite are less expensive than Hermite, but they are still unsuitable for extremes in temperature and humidity. Package standardization has only recently begun, despite the fact that integrated circuits (ICs) have been on the market for several years.

Figure 7.1Various types of integrated circuits (ICs)

7.3Classification of IC's

Monolithic ICs, thick and thin-film ICs, and hybrid ICs are the different types of integrated circuits.

7.3.1 Monolithic IC

In Monolithic IC, the whole electronic circuit or a group of the electronic circuit is integrated into a single piece of a semiconductor chip usually silicon that contains active and passive elements, and because of its flat shape, this type of integrated circuit is sometimes referred to as a planar IC

(Figure 7.2). The commonly used Integrated circuits such as modern computer microprocessors, microcontrollers, memories like RAM, ROM, etc., all are monolithic. In monolithic IC, all components are fabricated on the same substrate. Because the similar wafer can be used to make a large number of undistinguishable ICs, this property permits for mass production of ICs.Monolithic ICs are the most prevalent in practice because they minimize the cost of production and, as a result, the overall cost of the circuit.

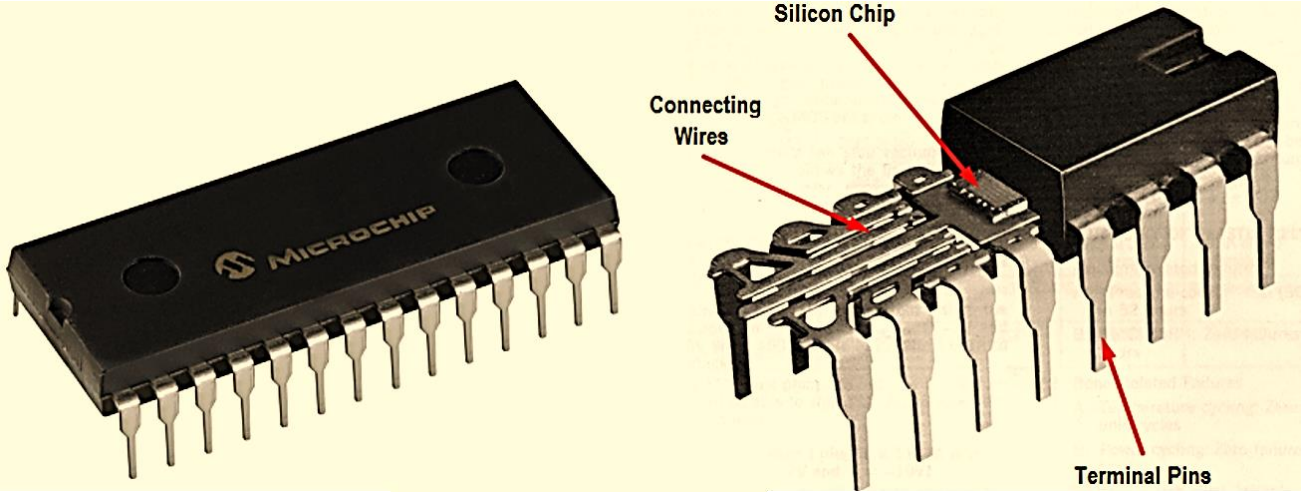


Figure7.2Monolithic IC in plastic package

7.3.2 Hybrid IC

In hybrid IC the entire electronic circuit is integrated into the ceramic wafer surface using different components and then enclosed in the complete unit, is shown in figure7.3.Therefore, it consists of many monolithic ICs which are interconnected using metallic connections mount on a common substrate.Hybrid IC is simply a miniaturized electronic circuit constructed by using individual devices, such as semiconductor devices and passive components bonded to a substrate or on a printed circuit board (PCB).

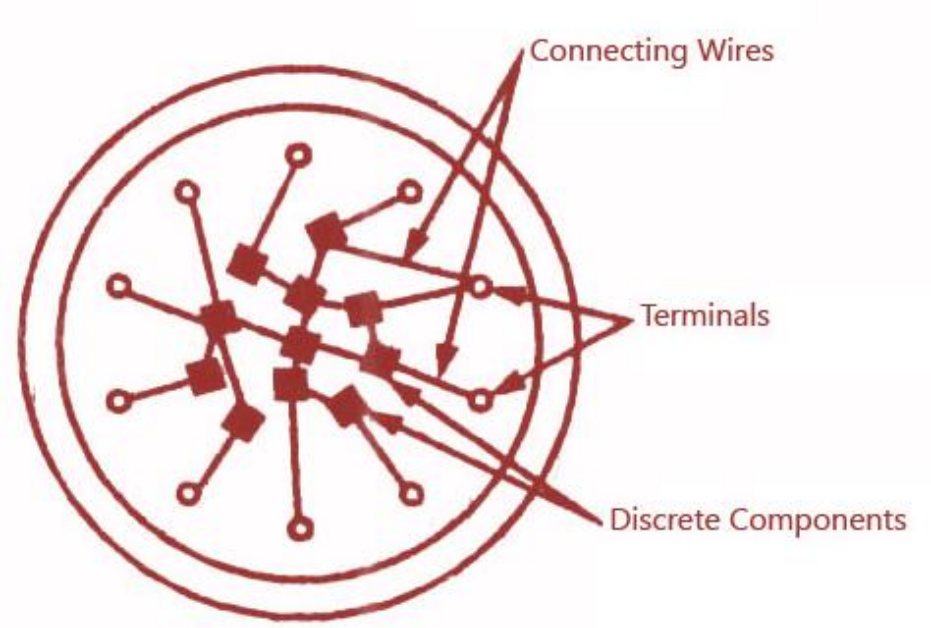


Figure7.3 The structure of a hybrid IC

By replacing wire bonding, this technology streamlines the connection between different semiconductor chips. It facilitates greater system yield and allows for enhanced communication bandwidth.

7.3.3 Thick and Thin Film

Only passive components such as resistors and capacitors are madeupof thin and thick-film ICs. In discrete circuits, active elements such as transistors are connected externally. The difference between thick and thin-film ICs is the thickness of the film deposited during fabrication, not the thickness of IC. In terms of shape and size, they are very similar. A thin film of conductor material is created on a ceramic or glass surface while its width is controlled in thin-film ICs.To make resistors, different resistant materials are chosen and added to the appropriate resistance.An insulating oxide is layered between two conducting sheets to manufacture capacitors.Even though thick and thin-film ICs are larger than monolithic ICs, they require higher tolerances. They also

have more flexibility and in-circuit style than monolithic ICs, as well as a more reliable high-frequency performance.A portion of thickfilm circuit is given in figure 7.4.Integrated circuits are functionally classified into two categories – *Analog* and *Digital*. Analog ICs operates under conditions in which currents and voltage vary continuously in a periodic way. Amplifiers including operational amplifiers, oscillators, various signals converters, etc., are an example of analog ICs. Digital ICs are mainly used in computers that operate in a pulsed mode and may, at any given instant, reside in one of two distinct states because present-day computers mostly use binary number systems where only two digits are used,0 and 1.

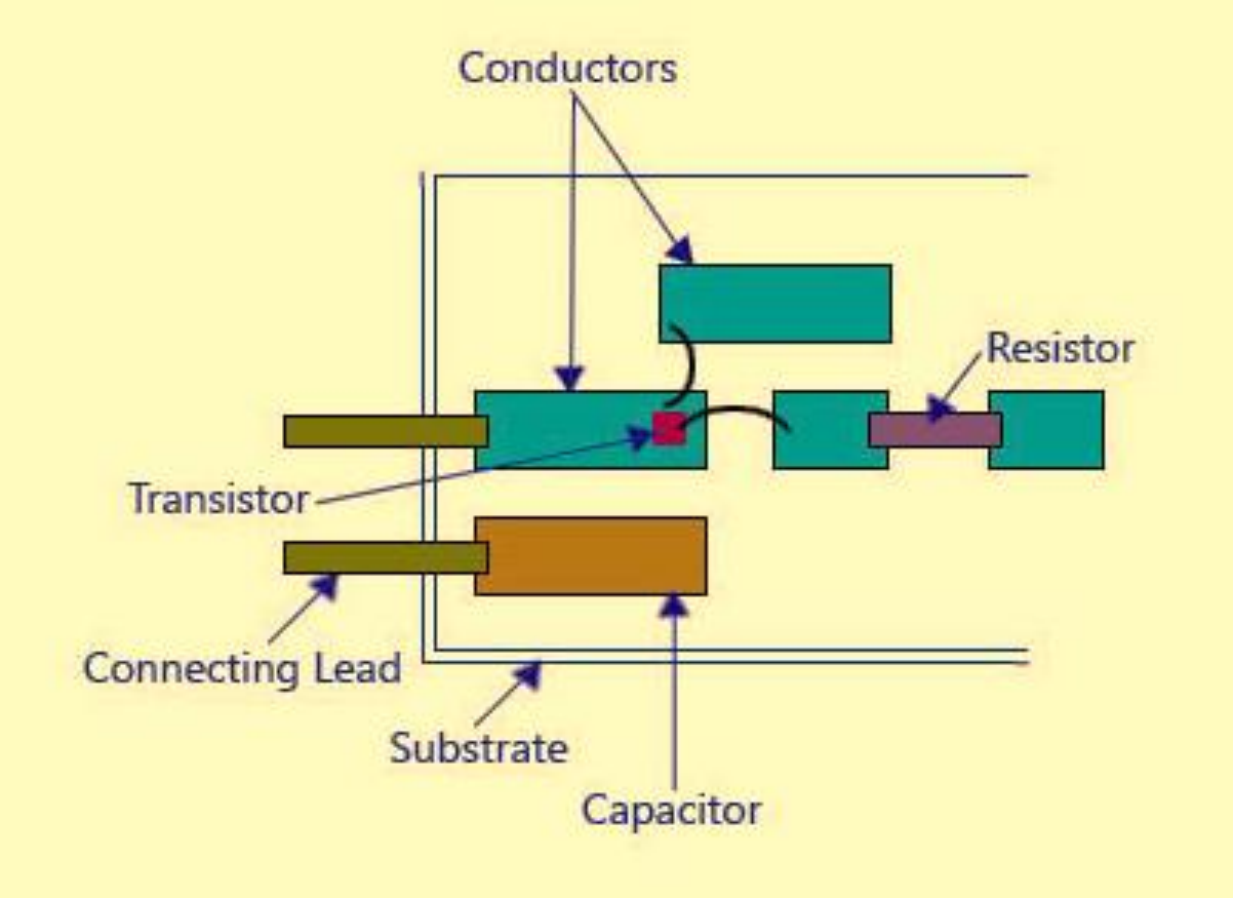


Figure 7.4 Thick film circuit

The complexity of ICs that may be produced on a single chip of silicon is defined by descriptive terms and are listed below with approximate dates of implementation:

(a) ***Small-scale integration*** (SSI) were no more than 10 components per chip

(b) ***Medium-scale integration*** (MSI) with 10 to 100 components per chip.

(c) ***Large-scale integration*** (LSI) with 100 to 1000 components per chip.

(d) ***Very-large-scale integration*** (VLSI) with more than 100 components per chip

(e) ***Very very-large-scale integration*** (V^2LSI)also caller ultra-large-scale integration (ULSI) with high packaging density

LSI, VLSI, and V^2LSI chips are often described by the number of bits that can be stored in a computer memory of similar complexity. Thus, LSI denotes circuits with a capability between 16KB (Kilobits), VLSI describesa circuit with capability between 16 KB and 1 MB (megabit) and V^2LSI refers to circuits containing more than 1MB.

7.4 Basic Monolithic Integrated Circuit Technology

Monolithic chip is the most important element of IC technology and it is the leading field of microelectronics as the basis for LSI, VLSI, and V^2LSI chips. Many processes are used in IC technology, some of which are common to both bipolar and MOS circuits, while others are not. As a result, these two are rarely combined in the same circuit. Thousands of separate steps are required for complete processing, many of which are critical. It must be carried out in a sterile environment with carefully controlled humidity, temperature, and, in some cases, light. To avoid contamination, ultrapure materials and chemicals must be used.Si must be refined to a high degree of purity before being processed into a monocrystalline wafer or disc for use in electronic

components. Wafers are doped with either a donor or an acceptor impurity to achieve the desired resistivity. Because monocrystalline Si is brittle, wafers are prone to breakage.All subsequent processes are carried out on one side of the wafer, which is known as planar technology and is lapped and polished to a mirror-like smoothness. Si wafers typically have a thickness of 200um and a diameter of 8-15cm, as shown in Figure 7.5.All bipolar ICs are made up of NPN transistors on p-type substrates because there are several appropriate n dopants with sufficiently high solubilities in Si (As, P, Sb), but only one for p-type doping.A PNP transistor compatible with the described technology can be made laterally, that is, with the emitter and collector side by side and current flow lateral rather than vertical, or by using the substrate as a common collector.

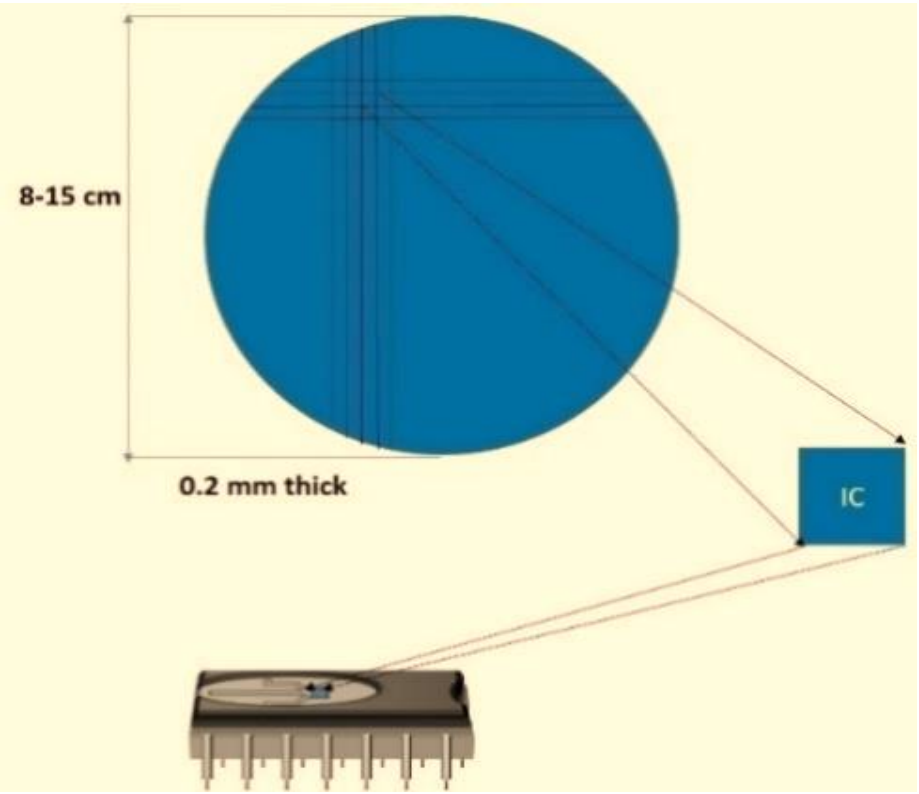


Figure 7.5A single piece of a semiconductor chip cut out from a silicon wafer

7.4.1 The process used in Monolithic Technology

The process involved in monolithic technology are shown in figure 7.6.

7.4.1.1 p-substrate

The primary step to make an IC is p-substrate in which cylindrical p-type silicon is grown. Then the crystal is cut by a diamond show in wafers as shown in the figure. Then the crystal is cut by a diamondshow in wafers as shown in the figure. This wafer is used to make integrated circuits.

7.4.1.2 Epitaxial N layer

The second phase is placing the wafer in a diffusion furnace.A thin layer of n-type semiconductors is formed by passing a mixture of silicon atoms and pentavalent atoms over the wafers. This thin layer is named as Epitaxial n layer.The entire integrated IC is built in this layer.

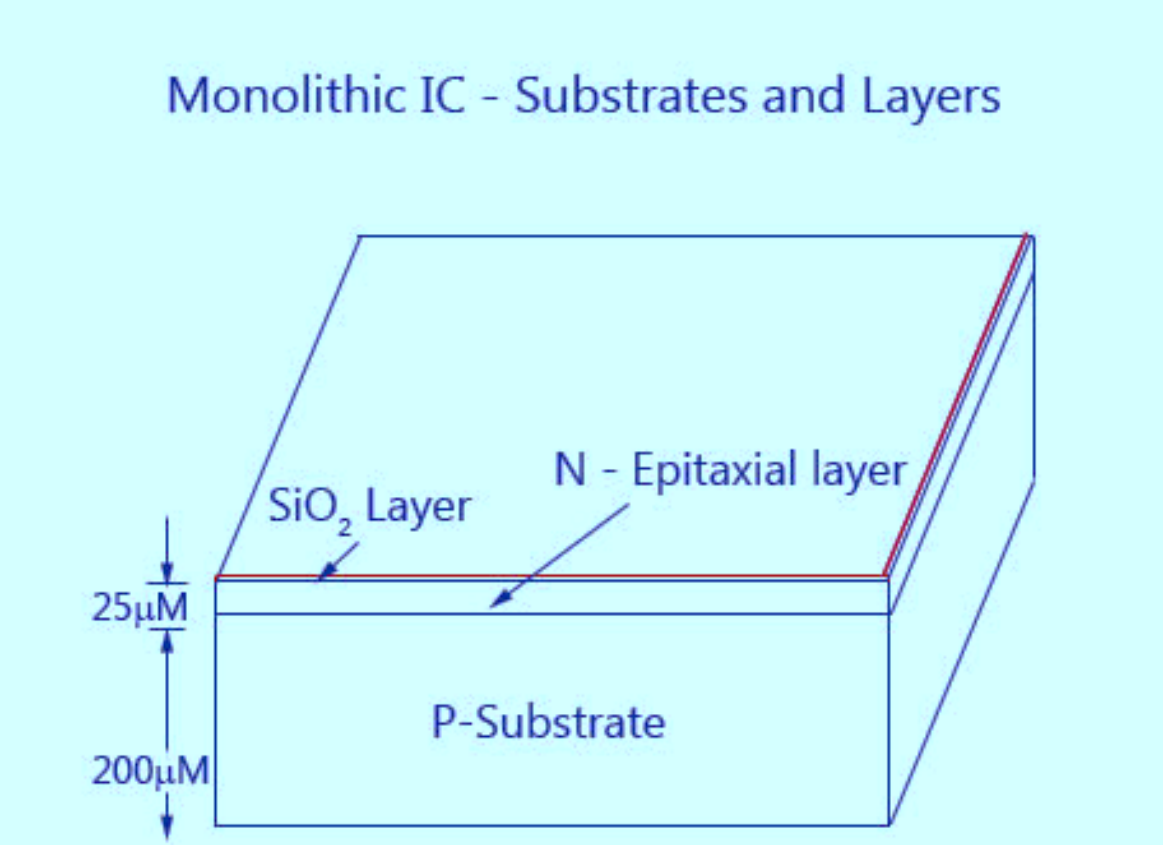


Figure 7.6 Process involved in monolithic technology

7.4.1.3 Insulating Layer

A thin SiO_2 layer is deposited across the entire chip surface to protect the epitaxial n layer from contamination. Pure oxygen is passed over the epitaxial layer.The oxygen atoms are combined with the silicon atoms to form a layer of silicon dioxide.

7.4.2 Producing Components

To manufacture distinct components, appropriate elements are introduced to the substrate at specific locations via the diffusion process. Diffusion is used to make resistors, capacitors, diodes, and transistors.

7.4.2.1 Etching

Before any contaminant is added to the substrate, the oxide layer is erased. The epitaxial layer is exposed during the etching process, allowing for the fabrication of required components. Etching is used to etch desired locations.

7.4.2.2 Chips

Wafers come in a variety of shapes and sizes. Each of these sections is its chip. On each wafer, the manufacturer produces hundreds of ICs. The wafer is then sliced into little chips using glass cutting. This is the primary reason for integrated ICs' low cost. After the chip has been cut, it is mounted and connections between the IC and external leads are created.

7.5Photolithography

Photolithography is the optical process of transferring geometrical shapes on a mask to the surface of a silicon wafer. Thethree basic steps involved in the photolithographic process are photoresist coating, UV exposer and development, and hard-baking. The process for the formation of a thin

film uniform layer of photoresist on the wafer is shown in figure7.7. In the starting phase of the photolithography process, the wafer is coated with photoresist the monolithic fabrication technique requires the selective removal of the insulator layer of SiO_2 to form an opening through which impurities can be diffused. There are two types of photoresists used- positive and negative photoresists. For positive resist is slightly hardened by soft baking and then selectively removed by a projection of UV light through a mask. The monolithic fabrication technique requires the selective removal of the insulator layer of SiO_2 to form an opening through which impurities can be diffused. There are two types of photoresist techniques that are used- positive and negative photoresist. For positive photoresists, the resist is exposed to UV light. Exposure to UV light changes the chemical structure of the resist and it becomes more stable in the developer solution. The developer solution removes the exposed resist part, forming an exact pattern that is to be transferred on the substrate.

The negative photoresist behavior is just the opposite of the positive photoresist technique. When it is exposed to UV light is becomes polymerized, which doesn't dissolve in the developer. this technique forms the inverse of the pattern which is to be transferred on the substrate whenever it is exposed to UV light.

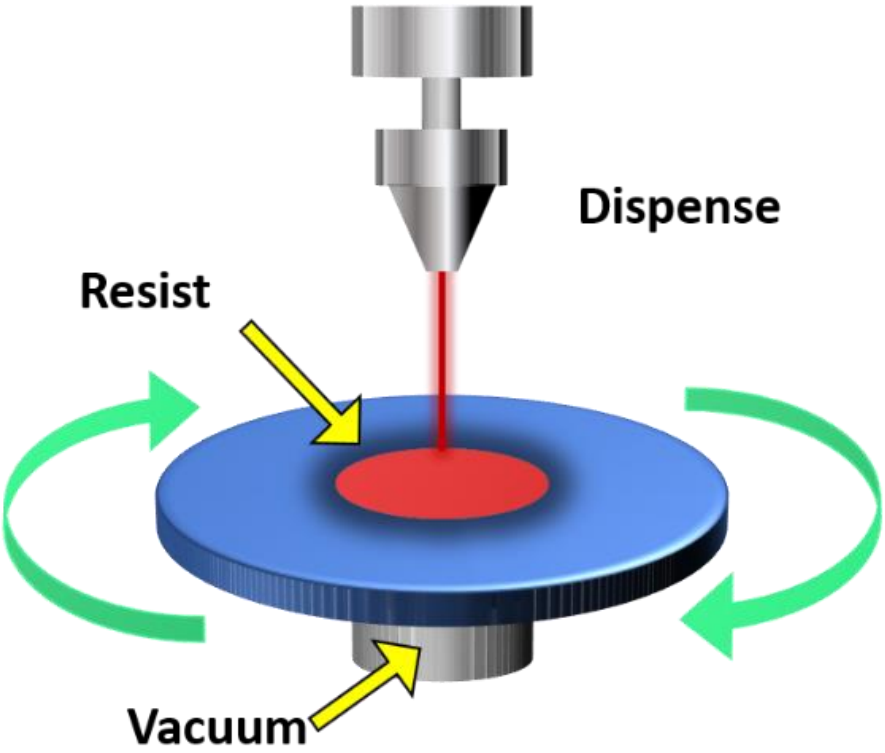


Figure 7.7Coating photo resist layer

7.5.1 Soft-Baking

Soft-baking is the process of removing nearly all of the solvents from the photoresist coating (Figure 7.8).In photo-imaging, soft-baking is extremely important. Only after soft baking does the photoresist coatings become photosensitive, or imageable. Light will not be able to reach the sensitizer while soft-baking. If there is still a lot of solvent in the coating, positive resists will onlybe partially exposed. The developer targets this under soft-baked positive resists in both exposed and unexposed areas tends to result in less etching resistance.

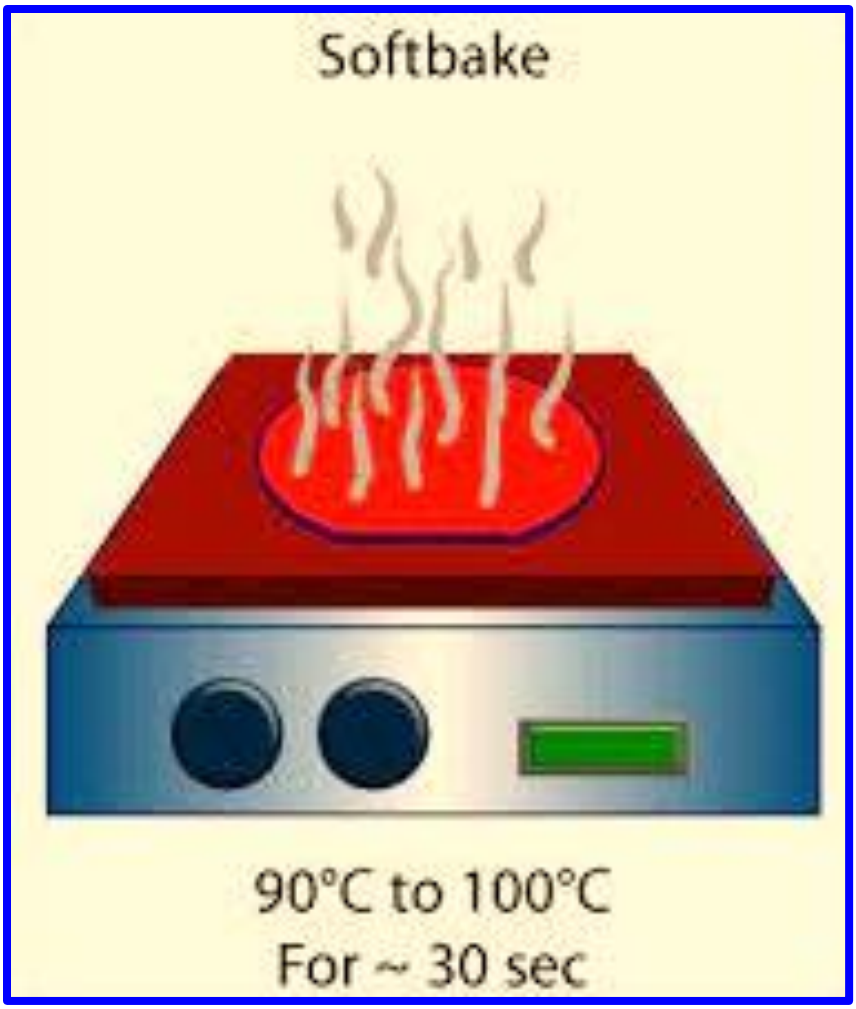


Figure 7.8 Soft baking step of photolithography

7.5.2 Exposure and Developer

Mask alignment is one of the most crucial steps in the photolithography process. A mask, also known as a "photomask," is a square glass plate with a patterned metal emulsion on one side. The pattern is transferred onto the wafer surface after the mask is aligned with wafer. Once the mask has been accurately aligned with the pattern on the wafer's surface, the photo-resist is exposed through the pattern on the mask with a high-intensity ultraviolet light (Figure 7.9a). The exposure

to light causes a chemical change that allows some of the photoresists to be removed by a specialsolution, called "developer" by analogy with a photographic developer (Figure 7.9b). Positive photoresist is the most common type.

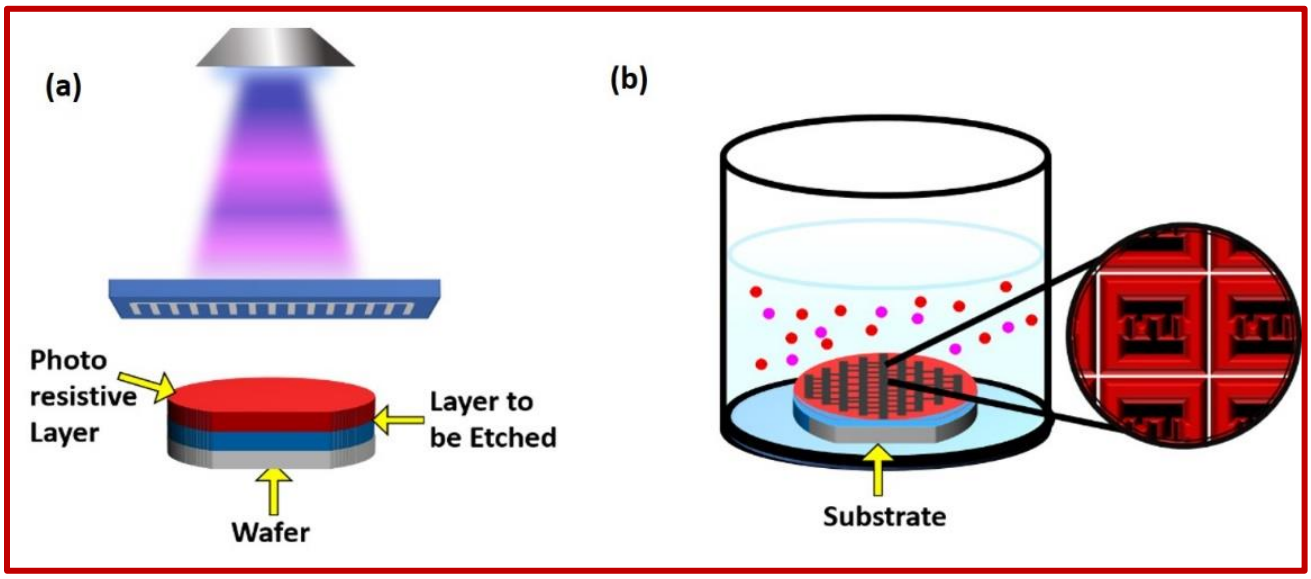


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Figure 7.9 (a) Coating exposure layer (b) Coating developer layer

When exposed positive photoresist becomes soluble in the developer.Similarly, with negative photoresist the unexposed regions are soluble in the developer. The final step after the developer is hard-baking.The solvent can be removed after the resist has been dissolved by heating to 80°C without leaving traces. This step is required in order to harden the photoresist and enhance its adhesion to the wafer surface.

7.6Active and Passive Components

7.6.1 Active components

Active components require an external source of energy to execute their unique function. They have some ability to control the flow of electricity.

Most active components are transistors, integrated circuits (chips), and diodes (Figure 7.10).

7.6.1.1Transistors: Transistors are typically used to intensify electrical impulses or as switching devices.

7.6.1.2Integrated circuits: Integrated circuits (ICs) are a type of circuit that consists of numerous complex circuits on a single circuit board and can be used to execute a variety of tasks.

7.6.1.3 Diodes A diode is a device that allows electricity to flow in just one direction.

7.6.2 Passive components

A passive device is one that adds no power gain (amplification) to a system or circuit. It does not have any control actions and does not require any input other than a signal to work. Passive components cannot oscillate or amplify a signal since their gain is always less than one. Passive components may multiply a signal by values less than one, adjust the phase of a signal, reject a signal if it does not contain the right frequencies, and regulate complex circuits, but they cannot multiply by more than one since they possess amplification. Resistors, capacitors, and inductors are examples of passive devices.

7.6.2.1 Resistors: Electronic components with a constant electrical resistance are known as resistors. The resistance of a resistor restricts the flow of electrons in a circuit.

7.6.2.2 Capacitors:A capacitor is an electrical energy storage device that operates in an electric field. It's a two-terminal passive electrical component.

7.6.2.3 Inductors: When electricity is applied to an inductor, it stores energy in the form of magnetic energy, which is employed in most power electronic circuits.

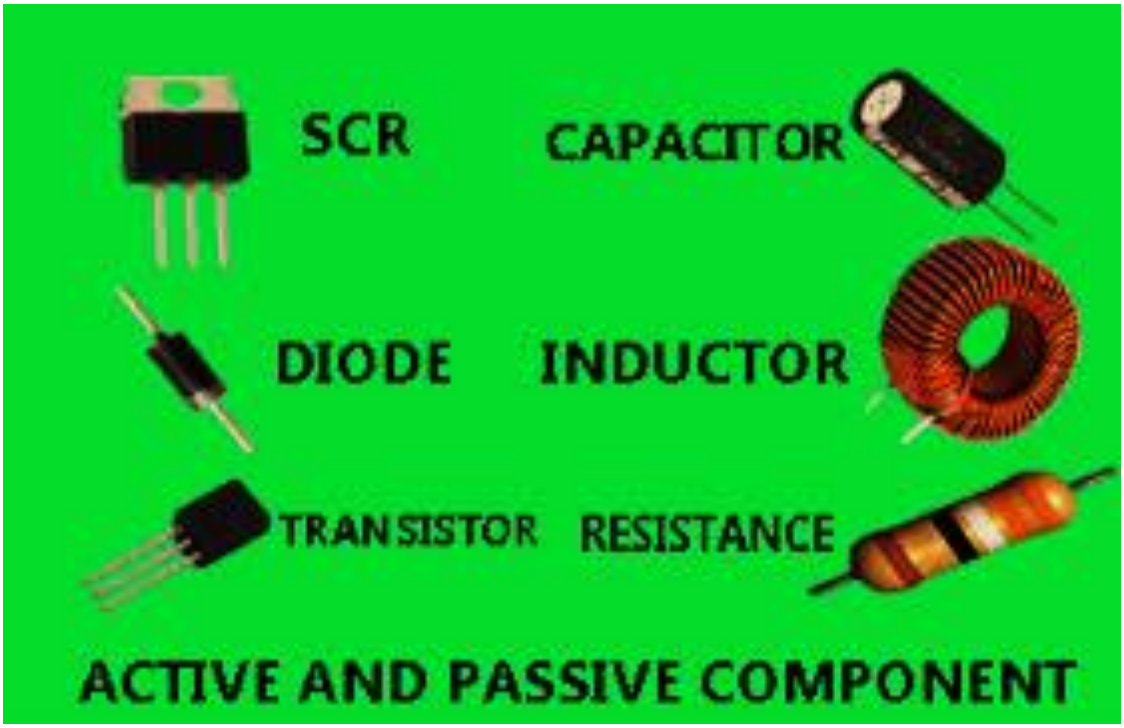

Figure 7.10 Some of the active and passive components

7.7Metal Semiconductor Contact

The metal-semiconductor contact is a crucial part of most semiconductor devices' performance. A metal-semiconductor junction occurs when metal and semiconductor materials are in close contact. The discrepancy in fermi energy between metal and semiconductor material, which is related to the difference in work functions, is the principle of forming different types of metal-semiconductor contacts. There are two types of metal-semiconductor contacts, both of which are often used in semiconductor devices:

1. Schottky Contact
2. Ohmic Contact

7.7.1 Schottky Contact

When the Fermi energies of the metal and the semiconductor are aligned together, a Schottky barrier contact is generated with a significant potential barrier height. It is usually employed as a diode because the Schottky barriers can cause rectifying properties. The Schottky contact can be generated by both n-type and p-type semiconductors.

Under the Equilibrium Condition of metal-semiconductor contact (When $\Phi_M > \Phi_{S)}$, electrons will migrate from semiconductor to metal owing to their higher energy. The net loss of electrons generates a positive charge in the semiconductor and a negative charge in the metal, resulting in a depletion region and forming a barrier at the surface of the semiconductor. Consequently, Figure 7.11depicts the equilibrium band structure for a metal and a semiconductor (n-type).

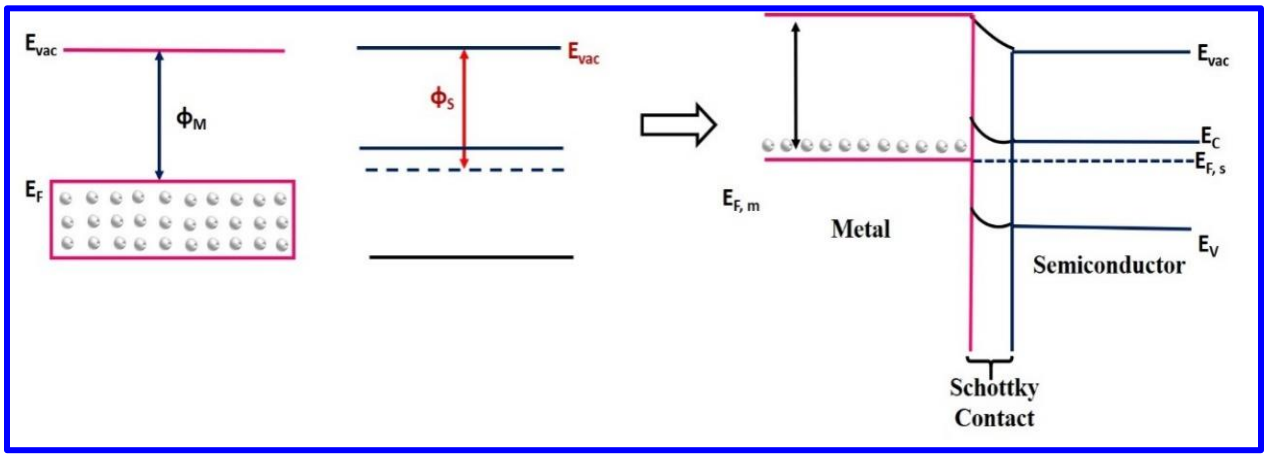

Figure 7.11 Band structure of metal and semiconductor, when work function of the metal is higher than semiconductor (Schottky contact)

7.7.2 Ohmic Contact

The contact is described as Ohmic contact in which current can flow in both directions through the metal-semiconductor contact. Between the metal-semiconductor interface, an ideal Ohmic contact has a low resistance and a non-rectifying junction with no potential. In the case of metal-semiconductor contact (When $\Phi_S > \Phi_M$), electrons will migrate from metal to semiconductor owing

to their low efficiency, causing the Fermi level in the semiconductor to elevate until the equilibrium state is reached. Figure 7.12 shows the band diagram at the equilibrium state.

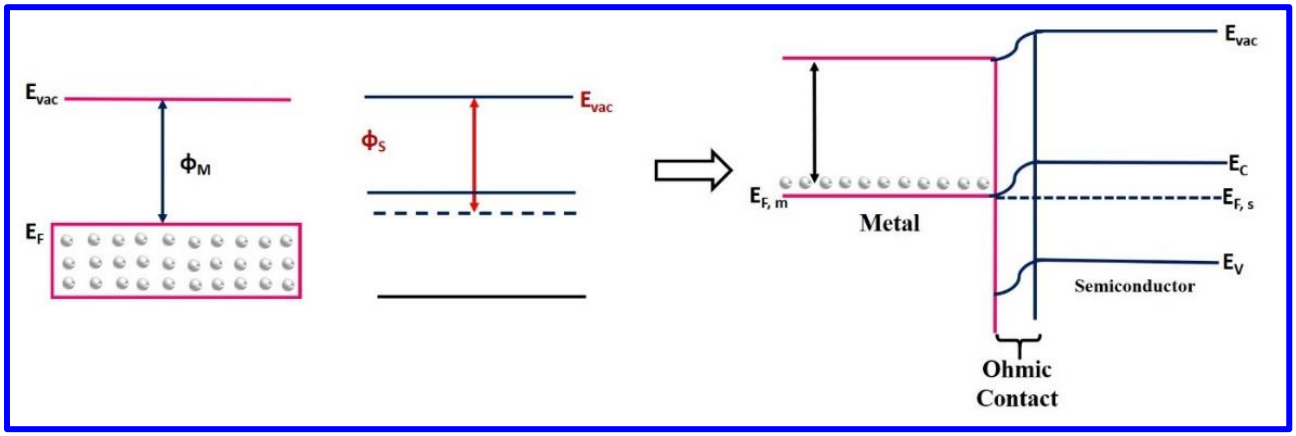

Figure 7.12Band structure of metal and semiconductor, when work function of metal is lower than semiconductor (Ohmic contact)

7.8 Charge Coupled Devices (CCD)

A charge-coupled device (CCD) is an image detector made up of an array of pixels that generates potential wells in response to applied clock signals, allowing charge packets to be stored and transported, as shown in figure 7.13. These charge packets are usually made of electrons created by the photoelectric effect from light photons or from the internal dark signal. Digital camera systems, integrating a diversity of charge-coupled device (CCD) detector configurations. Digital cameras substitute the sensitized film with CCD photon detector that capture and store information of image in the form of confined electrical charge that diverges with intensity of incident light. The adjustable electronic signal related with each picture pixel of the detector. These pixels are defined in one direction by gate structures on the silicon surface, and in the other way by electrical potentials from implants. In a specified pattern, a time-variable voltage sequence is conveyed to these gates which physically shifting the charge to an output amplifier, which works as a charge

to voltage converter. The output sequence of voltages is converted into a two-dimensional digital image by external circuit (typically a computer).

Full frame, frame transfer, and interline transfer are some of the different types of CCDs. A full-frame CCD collects light from the entire area (all pixels). This is the most popular astronomy detector and makes the best use of silicon area. These detectors necessitate the closing of the camera shutter during reading in order to prevent electrons during charge transfer, which would cause image streaking.

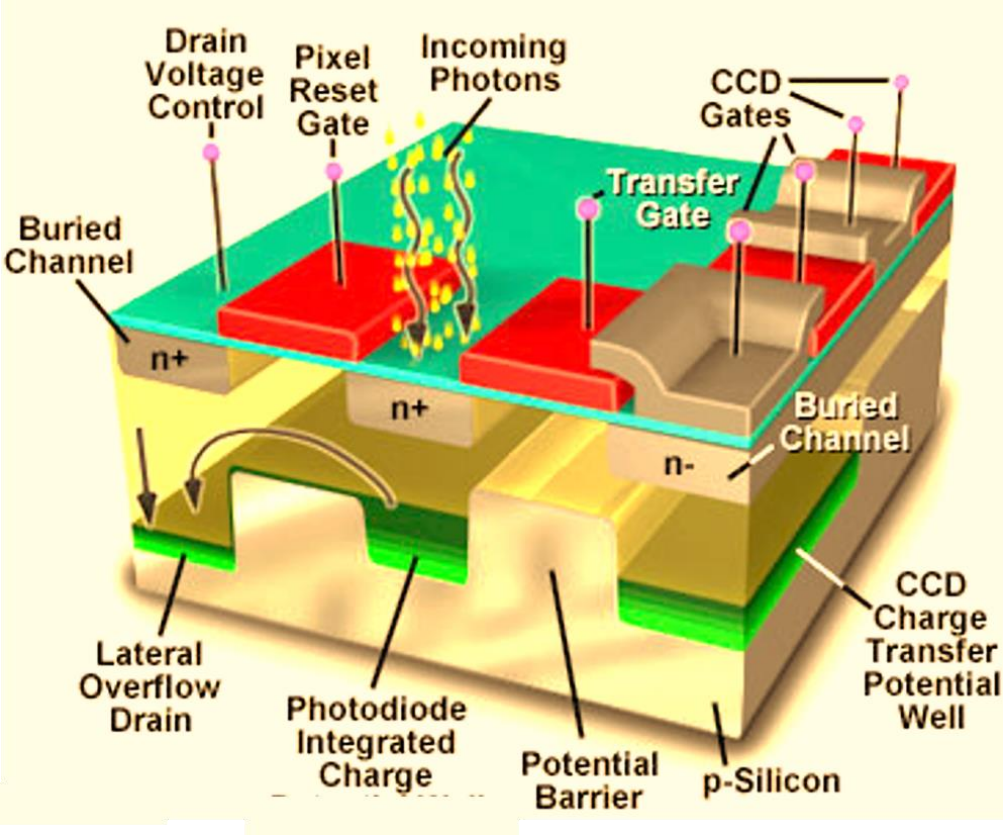

Figure 7.13 Working of charge coupled device

Frame transfer CCD cameras can capture at higher frame rates than full-frame cameras because exposure and readout might happen at the same time with varying degrees of timing overlap. They are comparable to full-frame devices in the structure of parallel register. However, an opaque mask

covers one-half of the rectangular pixel array and it is used as a storing buffer for photoelectrons collected by the unmasked light-sensitive region.

In Interline transfer CCD, columns of vigorous imaging pixels and masked storage-transfer pixels substitute over whole parallel register array. Because each photosensitive pixel column has a charge-transfer channel immediately adjacent to it, stored charge only needs to be relocated one column into the transfer channel.The interline-transfer design allows for very short integration periods through electronic management of exposure intervals.

7.9 Advantages and Disadvantages of Integrated Circuits (IC's)

7.9.1 Advantages

The advantages of integrated circuits over discrete circuits are as follows:

1. Due to the creation of numerous circuit elements in a single chip of semiconductor material, the size is extremely small.
2. Low power consumption.
3. Enhanced reliability owing to a fewer number of connections
4. Higher ability to operate at high and low temperatures.
5. Smaller space and weight prerequisite owing to the simplified circuit.
6. The layout of the circuit has been significantly simplified.
7. It is ideal for the functioning of small signals.
8. Low cost

7.9.2 Disadvantages

Drawbacks of the integrated circuits (IC's) are as follows:

1. High-power integrated circuits are impossible to manufacture.
2. In an IC, there is a deficiency of flexibility.
3. Inductors and transformers cannot be fabricated on the surface of a semiconductor chip.
4. If any component in an IC fails, the entire IC must be replaced with a new one.
5. High-voltage and low-noise operation are difficult to achieve.
6. It is not possible to assemble high-grade P-N-P.
7. Low temperature coefficients are difficult to attain.

7.10 Reference Books

1. Integrated Circuit Fabrication Technology by Shiban Tikuand Dhrubes Biswas
2. Electronic devices and circuits by Jacob Milliman and C. C. Halkais
3. Principles of electronics by V.K.Mehta
4. Electrical circuit and basic semiconductor electronics by Dr. J.P. Agarwal

7.11Terminal Questions

1. What is the difference between monolithic and hybrid ICs?
2. Advantages and disadvantages of ICs?
3. Summarize the photolithography?
4. What are the important IC technologies used?
5. Describe the process used in monolithic technology?
6. How is SiO_2 layer formed in a monolithic IC?
7. Describe the types of metal-semiconductor contacts?