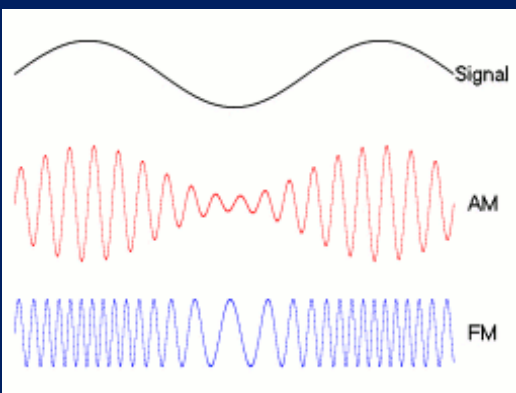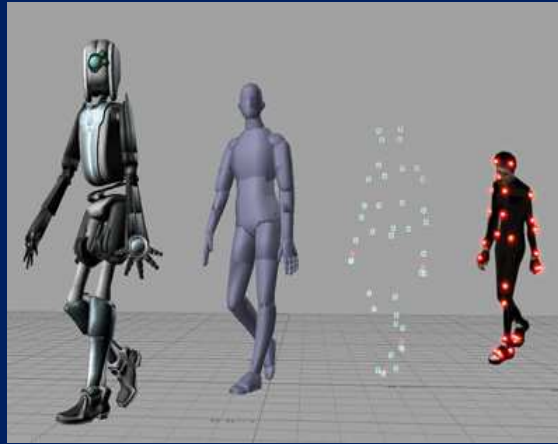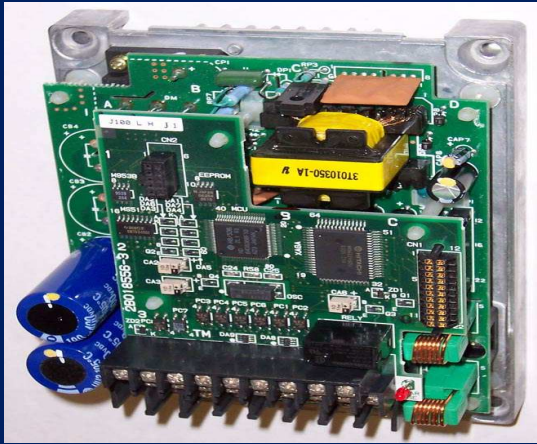**MSCPH521**

M. Sc. III SEMESTER

Digital Electronics and Communication System

DEPARTMENT OF PHYSICS

SCHOOL OF SCIENCES

UTTARAKHAND OPEN UNIVERSITY

Board of Studies

Prof. P. D. Pant
Director School of Sciences
Uttarakhand Open University, Haldwani
Prof. P. S. Bisht,
SSJ Campus, Kumaun University, Almora.
Dr. Kamal Devlal
Department of Physics
School of Sciences, Uttarakhand Open University

Prof. S.R. Jha,
 School of Sciences, I.G.N.O.U.,
Maidan Garhi, New Delhi
Prof. R. C. Shrivastva,
Professor and Head, Department of
Physics, CBSH, G.B.P.U.A.&T.
Pantnagar, India

Pogramme Coordinator : Dr. Kamal Devlal

Department of Physics (School of Sciences)
Dr. Kamal Devlal, Assistant Professor & Pogramme coordinator
Dr. Vishal Sharma, Assistant Professor   **Dr. Gauri Negi,** Assistant Professor
Dr. Meenakshi Rana, Assistant Professor (AC)   **Dr. Rajesh Mathpal,** Assistant Professor(AC)

Unit writing and Editing

Editing
Dr. Kamal Devlal
Department of Physics
School of Sciences, Uttarakhand Open
University

Writing
1. Dr. Rajesh Mathpal
Department of Physics
School of Sciences, Uttarakhand Open University
2. Dr. Mayur Agrawal
Department of Electronics and Communication
G B Pant University of Ag. And Tech. Pantnagar
US Nagar, Uttarakhand
3. Prof. Sanjay Mathur
Department of Electronics & Communication
Engineering, College of Technology,
G.B. Pant University of Agriculture & Technology,
Pantnagar
4. Dr. Hrishitosh Bisht
Department of Electronics and Communication
Engineering, College of Technology
G B Pant University of Ag. And Tech. Pantnagar
US Nagar Uttarakhand

Digital Electronics and Communication System

DEPARTMENT OF PHYSICS
SCHOOL OF SCIENCES
UTTARAKHAND OPEN UNIVERSITY
Phone No. 05946-261122, 261123
Toll free No. 18001804025
Fax No. 05946-264232, E. mail info@uou.ac.in
htpp://uou.ac.in

Contents

Course 13: Digital Electronics and Communication System   **Course code: MSCPH504**

                                                   Credit: 3

UNIT 1   Number Systems

Structure

1.1 INTRODUCTION

A number system is an ordered set of symbols and rules which are used to represent and manipulate different quantities. The total number of symbols used in a number system is called its radix (r), or base. In our day-to-day life, we use a number system which uses 10 symbols (0 to 9) to represent any quantity. As this number system uses 10 symbols, it is called decimal number system or a number system with radix 10.

In decimal number system, different numbers or quantities can be represented by putting these symbols at different positions; for example, 1234. Each symbol in a number is called a digit. The rightmost position of the number represents the unit position and called least significant digit. The successive positions from the unit position are called tens, hundreds, thousands, and so on. For example, in the decimal number 1234, the symbols 4, 3, 2 and 1 are at the unit position, tens position, hundreds position, and thousands position, respectively. Each position represents a specific power of the base (10) starting from '0' for unit position and increased by 1 for each successive position. For example, the number 1234 can be written as

$$1234 = 1 \times 10^3 + 2 \times 10^2 + 3 \times 10^1 + 4 \times 10^0$$

Decimal number system is used intensively in our daily life for counting, commercial and business data processing, the educational field and in many other areas. Digital computers and calculators are very useful in performing many types of complex calculations. However, these digital computers and calculators take the inputs and give the outputs in decimal form, there internal processing is not done in decimal number system. Various other number systems have been developed for the internal processing of digital computers. These number systems can be broadly classified as Binary (base 2), Octal (base 8), and Hexadecimal (base 16) number systems.

In this chapter, we will learn about the various number systems. We will learn the conversion of a number from one number system to another number system. We will discuss about different binary codes and binary arithmetic (addition and subtraction). We will also learn about the logic operations.

1.2 OBJECTIVES

After studying this unit, you will learn about-

- Different types of Number System
- Conversion of the numbers from one number system to another number system
- Binary Codes
- Binary arithmetic
- Logic functions

1.3 Binary Number System

Binary number system is a number system which uses only two symbols '0' and '1' to represent any quantity. The radix or base of the binary number system is '2'. In binary number system, a number is represented similar to decimal number systems by putting the digits '1' and '0' at different positions; for example, 110101. The digits in binary number are also called bits. The rightmost bit of the binary number is called Least Significant Bit (LSB). Similarly, the leftmost bit of the binary number is called Most Significant Bit (MSB). The equivalent binary form of first 16 decimal numbers is shown in Table 1.1.

Table 1.1
Numbers in Decimal and Binary number systems

Number in Decimal	Number in Binary	Number in Decimal	Number in Binary
0	0000	8	1000
1	0001	9	1001
2	0010	10	1010
3	0011	11	1011
4	0100	12	1100
5	0101	13	1101
6	0110	14	1110
7	0111	15	1111

Binary numbers with fractional part can be represented by putting a decimal point just before the fractional part similar to decimal number system. For example, 10110.1010 represents a binary number with integer part 10110 and fractional part .1010. As decimal number system is used in our daily life, therefore, it is necessary that students must understand the conversions from decimal to binary and binary to decimal.

1.3.1 Binary to Decimal Conversion

A binary number can be converted to its decimal equivalent by multiplying its digits with 2^0, 2^1, 2^2 successively, starting from rightmost digit (for binary integers). For example, the equivalent decimal value of the binary number 1110 can be calculated as

$$1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 =$$
$$1 \times 8 + 1 \times 4 + 1 \times 2 + 0 \times 1 = 14$$

To convert a binary number with fractional part into decimal the digits after (right side) to the decimal point are multiplied with 2^{-1}, 2^{-2}, 2^{-3} and so on, successively. For example decimal equivalent of .101 can be calculated as

$$1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} =$$
$$1 \times 0.5 + 0 \times 0.25 + 1 \times 0.125 =$$

$16 + 2 + 1 + 0.5 + 0.125 = 19.625$

Binary to decimal conversion can be best understood from the following examples.

Example 1.1: Convert the binary number 1101001 in to its equivalent decimal number.

Solution: The equivalent decimal number of the given binary number can be given as

$1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 =$
$1 \times 64 + 1 \times 32 + 0 \times 16 + 1 \times 8 + 0 \times 4 + 0 \times 2 + 1 \times 1 =$
$64 + 32 + 8 + 1 = 105$

Alternate solution: In the given binary number, 1 is present at 0th, 3rd, 5th and 6th positions from the right; therefore, equivalent decimal number can be given as

$1 \times 2^6 + 1 \times 2^5 + 1 \times 2^3 + 1 \times 2^0 =$
$64 + 32 + 8 + 1 = 105$

Example 1.2: Convert the binary number 1101.001 in to its equivalent decimal number.

Solution: Equivalent decimal number can be given as

$1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 0 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} = 13.125$
$8 + 4 + 1 + 0.125 = 13.125$

1.3.2 Decimal to binary conversion

A decimal integer can be converted into binary by dividing it by 2 (binary radix) successively until quotient becomes 0 and taking the reminders inr everse order (Last remainder as MSB and first remainder as LSB). The conversion can be understood by the following example.

Example 1.3: Convert the decimal number 89 into binary.

Solution: The binary equivalent of 89 can be calculated as

Division	Quotient	Remainder
$\dfrac{89}{2} =$	44	1
$\dfrac{44}{2} =$	22	0
$\dfrac{22}{2} =$	11	0
$\dfrac{11}{2} =$	5	1
$\dfrac{5}{2} =$	2	1

2	89	
	44	1
	22	0
	11	0
	5	1
	2	1
	1	0
	0	1

$\dfrac{2}{2}=$	1	0
$\dfrac{1}{2}=$	0	1

$$(89)_{10} = (1011001)_2$$

The conversion of a decimal fraction into binary is accomplished by multiplication instead of division. The fractional part of the given decimal number is multiplied with 2, and the integer of the output is accumulated as a binary bit. The remainder of the output is multiplied again with 2, and the integer of the output is accumulated as another binary bit. The successive multiplication should be takes place up to fractional part becomes 0. However, most of the times fractional part never reaches to 0 or it requires too many multiplications. Therefore, in practice, the multiplication is done only 4 to 5 times or as per required accuracy. The process can be understood by the following example.

Example 1.4: Convert the decimal number 0.854 into binary.
Solution: The binary equivalent of 0.854 can be calculated as

	Multiplication	Integer
$0.854 \times 2 =$	1.708	1
$0.708 \times 2 =$	1.416	1
$0.416 \times 2 =$	0.832	0
$0.832 \times 2 =$	1.664	1
$0.664 \times 2 =$	1.328	1
$0.328 \times 2 =$	0.656	0

$$(0.854)_2 = (0.110110)_2$$

To convert the decimal number having the both integer and fractional parts into binary number, the conversion of the integer and fractional parts is done separately and they are combined after the conversion to give final output. It can be understood from the following example.

Example 1.5: Convert the decimal number 76.548 into binary.

Solution: The binary equivalent of 76 can be calculated as

2	76	
	38	0
	19	0
	9	1
	4	1

2	0
1	0
0	1

The binary equivalent of 0.548 can be calculated as

	Multiplication	Integer
0.548 × 2 =	1.096	1
0.096 × 2 =	0.192	0
0.192 × 2 =	0.384	0
0.384 × 2 =	0.768	0
0.768 × 2 =	1.536	1
0.536 × 2 =	1.072	1

The binary equivalent of 76.548 can be given as

$$(76.548)_{10} = (1001100.100011)_2$$

Self Assessment Question (SAQ) 1: Convert the following binary numbers in to its decimal equivalent.

(a) 111011   (b) 0.11001   (c) 1100101.1001   (d) 10100.1011

Self Assessment Question (SAQ) 2: Convert the following binary numbers in to its decimal equivalent.

(a) 597   (b) 0.895   (c) 35.875   (d) 247.45

1.4 Other Number Systems

Binary number system is the largely used for the processing in digital computers. However, it becomes inconvenient to represent large numbers in binary as they require large number of bits. Therefore, some other number systems are also developed which are more convenient in some of the calculations/representations. Octal and Hexadecimal are the examples of these number systems. Now, you will learn about these number systems and their conversions to decimal and binary numbers.

1.4.1 Octal Number System

A number system which uses 8 symbols (from 0 to 7) to represent any quantity is called octal number system. The radix of octal number system is 8. The numbers in this number system are represented similar to decimal or binary number systems by putting the symbols at different positions. The first 16 decimal numbers in different number system can be represented as given in Table 1.2.

Table 1.2
First 16 decimal numbers in different number systems

Number in Decimal	Number in Binary	Number in Octal	Number in Hexadecimal
0	0000	00	0
1	0001	01	1
2	0010	02	2
3	0011	03	3
4	0100	04	4
5	0101	05	5
6	0110	06	6
7	0111	07	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

A number from the octal number system can be converted to its decimal equivalent similar to the binary to decimal conversion. The only difference is in the radix. In binary numbers, radix is 2, therefore, multiplication of digits is done by the power of 2's. In octal number system, radix is 8, therefore power of 8's are used for the multiplying with different digits. Conversion can be best understood by the following examples.

Example 1.6: Convert the octal number 506.25 in to its decimal equivalent.

Solution: The equivalent decimal number of the given binary number can be given as

$$5 \times 8^2 + 0 \times 8^1 + 6 \times 8^0 + 2 \times 8^{-1} + 5 \times 8^{-2}$$

$$= 5 \times 64 + 0 \times 8 + 6 \times 1 + \frac{2}{8} + \frac{5}{64}$$

$$= 326.328125$$

A decimal number can be converted into its octal equivalent number by adopting the process similar to decimal to binary conversion. Only difference is that the radix of binary numbers (2) is replaced with the radix of octal number (8) during division and multiplication. Conversion can be understood from the following example.

Example 1.7: Convert the decimal number 706.548 into octal.

Solution: The octal equivalent of 706 can be calculated as

8	706	
	88	2

11	0
1	3
0	1

$$(706)_{10} = (1302)_8$$

The octal equivalent of 0.548 can be calculated as

	Multiplication	Integer
$0.548 \times 8 =$	4.384	4
$0.384 \times 8 =$	3.072	3
$0.072 \times 8 =$	0.576	0
$0.576 \times 8 =$	4.608	4

The octal equivalent of 76.548 can be given as

$$(706.548)_{10} = (1302.4304)_8$$

1.4.2 Hexadecimal Number Systems

As name implies, hexadecimal number system has radix 16 (uses 16 symbols to represent any quantity). In hexadecimal number system initial 10 symbols are represented by 1 to 9 similar to decimal number system, and rest of the symbols is represented by English alphabets A to F (in capital letters) as given in Table 1.2.

The hexadecimal numbers can be converted to decimal numbers and vice-versa, similar to the octal to decimal and decimal to octal conversion. Only radix is changed from 8 to 16. Conversions can be understood by the following examples.

Example 1.8: Convert hexadecimal number 2B6.F1 in to its decimal equivalent.

Solution: The equivalent decimal number of the given binary number can be given as

$$2 \times 16^2 + 11 \times 16^1 + 6 \times 16^0 + 15 \times 16^{-1} + 1 \times 16^{-2}$$

$$= 2 \times 256 + 11 \times 16 + 6 \times 1 + \frac{15}{16} + \frac{1}{256}$$

$$= 694.94140625$$

Example 1.9: Convert the decimal number 706.548 into hexadecimal.

Solution: The hexadecimal equivalent of 706 can be calculated as

16	706	
	44	2
	2	12

0	2

$$(706)_{10} = (2C2)_{16}$$

The hexadecimal equivalent of 0.548 can be calculated as

	Multiplication	Integer
$0.548 \times 16 =$	8.768	8
$0.768 \times 16 =$	12.288	12
$0.288 \times 16 =$	4.608	4

The hexadecimal equivalent of 76.548 can be given as

$$(706.548)_{10} = (2C2.8C4)_{16}$$

1.4.3 Conversion to binary and vice-versa

The octal and hexadecimal numbers can be converted to binary numbers by first converting them into decimal and then into binary as given in the following example.

Example 1.10: Convert the octal number 506 and hexadecimal number 2B6 in binary.

Solution: The equivalent decimal number of the given octal number can be given as

$$5 \times 8^2 + 0 \times 8^1 + 6 \times 8^0 = 326$$

326 can be converted to binary as

2	326	
	163	0
	81	1
	40	1
	20	0
	10	0
	5	0
	2	1
	1	0
	0	1

$$(506)_8 = (101000110)_2$$

The equivalent decimal number of the given hexadecimal number can be given as

9

$$2 \times 16^2 + 11 \times 16^1 + 6 \times 16^0 = 694$$

694 can be converted to binary as

2	694	
	347	0
	173	1
	86	1
	43	0
	21	1
	10	1
	5	0
	2	1
	1	0
	0	1

(2B6)₁₆ = (1010110110)₂

Octal number can be converted into binary directly by putting 3 bit binary equivalent for each digit side by side. Similarly, hexadecimal number can be converted into binary by putting 4 bit binary equivalent for each digit side by side. Conversions are illustrated in the examples below.

Example 1.11: Convert the octal number 506 and hexadecimal number 2B6 into its decimal equivalent.

Solution: The equivalent binary number of the given octal and hexadecimal numbers can be calculated as


506
101000110

2B6
001010110110

Binary numbers can be converted to octal and hexadecimal by making the groups of three and four bits respectively and putting the octal and hexadecimal equivalent of these groups side by side. If required, 0's can be added to the binary number to make the groups.

In a binary number having decimal point, binary bits before and after decimal point are converted separately. Groups are made by starting the digits nearest to the decimal point and adding 0's to the extreme left part and right of decimal points for integer and fractional parts, respectively. These conversions can be better understood by the following example.

Example 1.12: Convert the binary number 1001011110.01011 in octal and hexadecimal.

Solution: The equivalent decimal number of the given octal and hexadecimal number can be given as

001001011110.010110

1136.26

001001011110.01011000

25E.58
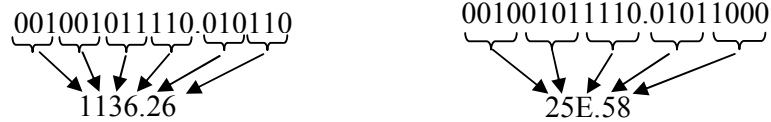
1.4.4 Conversion between octal and hexadecimal

Direct conversion between octal to hexadecimal and vice-versa is not possible. These conversions can be done by either converting them to binary or decimal. The conversions are more convenient by first converting them to binary.

Example 1.13: Convert the octal number 215.17 in hexadecimal.

Solution: The given octal number should be first converted into binary by putting three bit binary equivalent side by side and then into hexadecimal by making the group of four bits and putting their hexadecimal equivalent side by side as shown below.

$$(215.17)_8 = (010001101.001111)_2 = (08D.3C)_{16}$$

Example 1.14: Convert the hexadecimal number AC3.BC in octal.

Solution: The hexadecimal number is converted into octal by first converting it into binary as shown below.

$$(AC3.BC)_{16} = (101011000011.10111100)_2 = (5303.57)_8$$

1.4.3 Other Number Systems and their base conversions

Other number systems can also be used just by selecting a base and taking number of symbols equal to the base. For example, consider a number system with base 5; the number of symbols in this number system will be 0 to 4. The number from any number system can be converted to decimal similar to binary to decimal conversion and using the powers of its radix (2 in binary) for multiplication. Consider a number with radix r in more generalized form as

$$b_3 b_2 b_1 b_0 . b_{-1} b_{-2} b_{-3}$$

The b_j coefficients are one of the r digits (0, 1, 2, ... , r-1), where r is the radix of the number system, and the subscript value j gives the place value. This number can be converted to decimal by multiplying the coefficients with the power of r as

$$b_3 \times r^3 + b_2 \times r^2 + b_1 \times r^1 + b_0 \times r^0 + b_{-1} \times r^{-1} + b_{-2} \times r^{-2} + b_{-3} \times r^{-3}$$

The numbers from these number systems can be converted to binary by dividing the number successively by the radix of the number system similar to decimal to binary conversion. To convert a number from one number system to the number system (other than binary and

decimal), the number should be first converted to binary or decimal. The conversions can be understood by the following example.

Example 1.15: Convert the number $(321.43)_5$ in its equivalent number in the number system having base 6.

Solution: The equivalent decimal number of the given number can be given as

$$3 \times 5^2 + 2 \times 5^1 + 1 \times 5^0 + 4 \times 5^{-1} + 3 \times 5^{-2} = 90.92$$

$$(321.43)_5 = (90.92)_{10}$$

90 can be converted into base 6 as

6	90	
	15	0
	2	3
	0	2

$$(321)_5 = (90)_{10} = (230)_6$$

0.92 can be converted into the number system having base 6 as

	Multiplication	Integer
$0.92 \times 6 =$	5.52	5
$0.52 \times 6 =$	3.12	3
$0.12 \times 6 =$	0.72	0

$$(321.43)_5 = (90.92)_{10} = (230.53)_6$$

The conversion can also be done by first converting the base 5 number into binary.

Self Assessment Question (SAQ) 3: Convert the following numbers into decimal

(a) $(426.27)_8$ (b) $(A09.F6)_{16}$ (c) $(423.21)_5$ (d) $(123.21)_4$

Self Assessment Question (SAQ) 4: Convert the following numbers into binary

(a) $(426.27)_8$ (b) $(A09.F6)_{16}$ (c) $(423.21)_5$ (d) $(123.21)_4$

Self Assessment Question (SAQ) 5: Convert the base of the following numbers

(a) $(426.27)_8$ = ($)_{16}$ (b) $(35F.D8)_{16}$ = ($)_8$

(c) $(426.27)_8$ = ($)_4$ (d) $(425.25)_6$ = ($)_8$

Self Assessment Question (SAQ) 6: Which of the following numbers is not octal number?

(a) 453   (b) 236.51   (c) 457.28   (d) 101.101

Self Assessment Question (SAQ) 7: Choose the correct options-

(a) A number from any base can be converted to binary number directly.

(b) A number from any base can be converted to decimal number directly.

(c) A number from a number system can be converted to the number in any other number system directly.

(d) Hexadecimal and Octal number can be converted to binary directly.

(e) A number from a number system can be converted to the number system with different base by first converting it into decimal.

1.5 Binary Codes

Other than decimal numbers, many other discrete elements of information such as arithmetic operators and alphabets are used in the computers. To represent them distinctly, a unique binary code is assigned to each discrete elements. For convenience at some places, decimal digits are also assigned binary codes. These binary codes use binary bits 0 and 1 to represent discrete element of information; however, binary codes are different than binary numbers. The binary codes can be divided into two categories: decimal codes and alphanumeric codes. Decimal codes are used to represent decimal digits 0 to 9, while alphanumeric codes are used to represent letters and special symbols along with decimal digits. BCD and Excess-3 are the examples of decimal codes, and EBCDIC and ASCII codes are the examples of alphanumeric codes. The minimum number of bits required to code 2^n distinct quantities is n; however, there is no maximum limit of bits that may be used for representing binary code.

1.5.1 BCD Codes

Binary Coded Decimal (BCD) codes are used to represent decimal digits 0 to 9. As total number of symbols in decimal numbers are 10, a minimum of four bits are required to represent them distinctly. The BCD is a straight assignment of the binary equivalents of a decimal numbers. It can also be represented by assigning weights to the binary bits according to their positions. The weights in the BCD code are 8, 4, 2 and 1 from most significant bit to least significant bit, respectively. For example, the bit assignment 0110, can be interpreted by the weights as $0 \times 8 + 1 \times 4 + 1 \times 2 + 0 \times 1 = 6$. BCD equivalents of decimal numbers are tabulated in Table 1.3.

**Table 1.3**
BCD equivalents of decimal numbers

Decimal Numbers	BCD 8421
0	0000
1	0001
2	0010
3	0011

4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Decimal numbers can be represented in the BCD by putting a 4 digit BCD code of in place of every decimal digit directly. It does not require any calculation as in decimal to binary. For example, BCD equivalent of 769 can be given as 0111 0110 1001. Here it is important to understand that BCD equivalent of a decimal number is different than binary equivalent discussed above. For example, binary equivalent of 125 is 7 bit long as 1111101 which is different than its BCD equivalent (as 000100100101).

Example 1.16: Convert the decimal number 198.57 into equivalent BCD.

Solution: The given decimal number has five digits, therefore, its equivalent BCD has 5X4 = 20 bits and it can be represented as

$$1\ 9\ 8\ .\ 5\ 7$$
$$0001\,1001\,1000.0101\,011$$
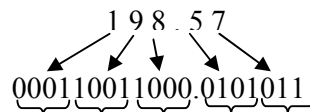
Example 1.17: Convert the BCD number 100101001.01010110 into equivalent decimal.

Solution: The given BCD number can be converted to decimal by adding three extra 0's at MSB side and making the groups of 4 bits as shown below.

$$000100101001.01010110$$
$$129.56$$
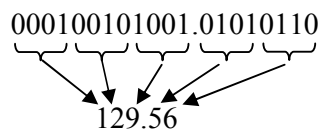
The conversion from BCD to decimal is similar to binary to hexadecimal conversion; however, 1010 to 1111 are invalid in BCD.

1.5.2 Excess-3 Codes

The excess-3 codes are also used to represent decimal digits. These codes are the non-weighted binary codes as they cannot be obtained by assigning the weights to different bits. Excess-3 codes for the decimal digits are obtained by adding 3 to the corresponding 4 bit BCD of each digit. Excess-3 equivalents of decimal numbers are tabulated in Table 1.4.

Table 1.4
Excess-3 equivalents of decimal numbers

Decimal Numbers	Excess-3 code

0	0011
1	0100
2	0101
3	0110
4	0111
5	1000
6	1001
7	1010
8	1011
9	1100

The advantage of Excess-3 codes is that these codes are self complementary codes as complement of decimal digit can be obtained by complementing the bits of its Eccess-3 code. For example, complement of 3 is 9 - 3 = 6 and complement of 0110 (Excess-3 code of 3) is 1001 (Excess-3 code of 6). Decimal numbers are represented in Excess-3 similar to BCD by putting a 4 digit code of every digit directly. For example, Excess-3 equivalent of 769 is 1010 1001 1100. Conversion can be understood by following examples.

Example 1.18: Compute the Excess-3 code for the decimal number 198.57.

Solution: The given decimal number has five digits, therefore, its equivalent Excess-3 code has 20 bits and it can be represented as

$$1\ 9\ 8\ .\ 5\ 7$$
$$010011001011.10001010$$

Example 1.19: A number in Excess-3 code is given as 10110101001.01010110. Find its equivalent decimal number.

Solution: The given Excess-3 code can be converted to decimal as

$$010110101001.01010110$$
$$276.23$$

1.5.3 Gray Codes

In many digital systems continuous number has to be converted into digital form. In these systems, it is convenient to use the Gray code shown in Table 1.5 to represent the digital data. The advantage of the Gray code over binary numbers is that only one bit in the code group changes when going from one number to the next. For example, in going from 7 to 8, the Gray code changes from 0100 to 1100; only the most significant bit changes from 0 to 1, the

other three bits remain the same. When comparing this with binary numbers, the change from 7 to 8 will be from 0111 to 1000, which causes all four bits to change their values.

Table 1.5
Equivalent Gray code of decimal numbers

Decimal	Binary	Gray	Decimal	Binary	Gray
0	0000	0000	8	1000	1100
1	0001	0001	9	1001	1101
2	0010	0011	10	1010	1111
3	0011	0010	11	1011	1110
4	0100	0110	12	1100	1010
5	0101	0111	13	1101	1011
6	0110	0101	14	1110	1001
7	0111	0100	15	1111	1000

Self Assessment Question (SAQ) 8: Convert the following decimal numbers into BCD and Excess-3.

(a) 876.27   (b) 254.21   (c) 541.29   (d) 891.56

Self Assessment Question (SAQ) 9: Convert the following codes into decimal

(a) $(100101100011.10010111)_{BCD}$ (b) $(010010000111.00011001)_{BCD}$

(c) $(101101111100.10110111)_{EX-3}$ (d) $(100111000100.10001001)_{EX-3}$

Self Assessment Question (SAQ) 10: Which of the following numbers is not a valid BCD?

(a) 10010111   (b) 10100111   (c) 01011000   (d) 00000001

1.6 Binary Arithmetic

Digital computers use binary numbers for their calculations. Binary arithmetic plays an important role in these calculations. Addition and subtractions are the basic arithmetic operations which are used in most of the calculations. Here, we will discuss the binary addition and subtraction.

1.6.1 Binary Addition

Binary addition is done similar to decimal addition. If the addition of two digits is greater than the largest binary number '1' (which is 9 in the case of decimal), a carry is produced which is added to the addition of next significant digits. Addition of two binary bits is given in Table 1.6.

Table 1.6: Addition of two binary bits

Addition	Carry	Sum
0 + 0	0	0

0 + 1	0	1
1 + 0	0	1
1 + 1	1	0

To add two binary numbers with more than one digit, an addition of the carry is also required with the addition of two bits. Therefore addition of three binary bits must be known. Addition of three binary bits is given in Table 1.7.

With the help of additions given in Table 1.6 and 1.7, addition of two binary numbers can be understood using following example.

Table 1.7: Addition of three binary bits

Addition	Carry	Sum
0 + 0 + 0	0	0
0 + 0 + 1	0	1
0 + 1 + 0	0	1
0 + 1 + 1	1	0
1 + 0 + 0	0	1
1 + 0 + 1	1	0
1 + 1 + 0	1	0
1 + 1 + 1	1	1

Example 1.20: Add the binary numbers $(111101)_2$ and $(101110)_2$.

Solution:

```
    1  1  1  0  0     Carry
    1  1  1  1  0  1  Augend
+   1  0  1  1  1  0  Addend
_____
1   1  0  1  0  1  1   Sum
```

The addition is started from the least significant side by adding 1 and 0 which produces 1 as sum and 0 as carry. The carry 0 is passed to the next significant addition as shown above. Now, the addition 0+0+1 is performed which also produces 1 as sum and 0 as carry. 0 carry is passed to the next significant addition. In this way the binary numbers are added and addition is obtained as shown above.

1.6.2 Binary Subtraction

Binary subtraction is also similar to the decimal subtraction. In the decimal arithmetic, a smaller digit is subtracted directly from the larger digit. Similarly in binary subtraction, 0 can be subtracted from 1 directly and produces 1 as a difference. However, if a larger number is subtracted from the smaller number, borrow has to be taken from the next significant digit and 1 has to be subtracted from the next significant digit of minuend. Similarly, if 1 is subtracted from 0, a borrow 1 is taken from the next significant minuend and a difference (10-1 =) 1 is produced. One bit subtraction is given in Table 1.8.

Table 1.8: One bit subtraction

Subtraction	Borrow	Difference
0 - 0	0	0
0 - 1	1	1
1 - 0	0	1
1 - 1	0	0

For higher bit subtractions one borrow bit has to be subtracted from next significant subtraction, subtraction of two bits from one bit is therefore required. A subtraction of two bits from one bit is given in Table 1.9.

Table 1.9: Subtraction of two bits from one bit

Subtraction	Borrow	Difference
0 - 0 - 0	0	0
0 - 0 - 1	1	1
0 - 1 - 0	1	1
0 - 1 - 1	1	0
1 - 0 - 0	0	1
1 - 0 - 1	0	0
1 - 1 - 0	0	0
1 - 1 - 1	1	1

With the help of Tables 1.8 and 1.9, subtraction can be performed which can be understood from the following examples.

Example 1.21: Subtract $(10111)_2$ from $(101101)_2$.

Solution:

```
  1 0 1 1 0       Borrow
  1 0 1 1 0 1   Minuend
-   1 0 1 1 1   Subtrahend
  0 1 0 1 1 0   Difference
```

In the subtraction, the subtraction should be done as Minuend - Subtrahend - Borrow. As subtraction starts from rightmost bit, 1-1 is done initially which produces 0 borrow and 0 difference which can be seen from Table 1.8. Now, the subtraction, 0 - 1 - 0 is done which gives 1 as borrow and 1 as difference. The borrow is passed to the next significant subtraction. In this way subtraction is done and final difference is obtained as 010110.

Self Assessment Question (SAQ) 11: Add the binary numbers $(100111)_2$ and $(101110)_2$.

Self Assessment Question (SAQ) 12: Add the binary numbers $(10101)_2$ and $(101011)_2$.

Self Assessment Question (SAQ) 13: Subtract the binary numbers $(10101)_2$ from $(101011)_2$.

Self Assessment Question (SAQ) 14: Subtract the binary numbers $(100111)_2$ from $(110001)_2$.

1.7 Logic Operations

Binary logic deals with variables that take only two discrete values logic '1' and logic '0'. These two values of the variables may also be called by different names such as true and false, yes and no, etc. These variables can designated by letters of the alphabet such as A, B, C, x, y, z, etc, to perform different binary operations. The binary operations done with binary variables and gives logic '1' or logic '0' as output, are designated as logical operations. The basic logical operations are AND, OR, and NOT operations which can be described as follows.

1. AND: This operation is represented by a dot or by the absence of an operator. For example, x·y = z or xy = z which is read "x AND y is equal to z." The logical operation AND is interpreted to mean that z = 1 if and only if x and y both are equal to 1; otherwise z = 0. In other words, if any of the input is 0, AND output is equal to 0.

2. OR: This operation is represented by a plus sign. For example, x + y = z which is read "x OR y is equal to z," meaning that z = 0 if and only if x and y both are equal to 0; otherwise z = 1. In other words, if any of the input is 1, OR output is equal to 1.

3. NOT: This operation is represented by a prime (sometimes by a bar). For example, x' = z (or $\bar{x} = z$) is read "not x is equal to z," meaning that z is what x is not. In other words, if x = 1, then z = 0; and z = 1, if x = 0.

Binary logic resembles binary arithmetic, and the operations AND and OR have some similarities with multiplication and addition, respectively. In fact, the symbols used for AND and OR are the same as those used for multiplication and addition. However, binary logic are different with binary arithmetic.

An arithmetic variable designated as a number may consists of many digits. However, a logic variable can have only one bit which can be either a 1 or a 0. For example, in binary arithmetic (addition), we have 1 + 1 = 10 (read: "one plus one is equal to 2"), whereas in binary logic (OR), we have 1 + 1 = 1 (read: "one OR one is equal to one").

For each combination of the values of x and y, there is a value of z specified by the definition of the logical operation. These definitions may be listed in a compact form using truth tables. A truth table is a table of all possible combinations of the variables showing the relation between the values that the variables may take and the result of the operation. For example, the truth tables for the operations AND and OR with variables x and y are obtained by listing all possible values that the variables may have when combined in pairs. The result of the operation for each combination is then listed in a separate coloumn. The truth tables for AND, OR, and NOT are listed in Table 1.10. These tables clearly demonstrate the definition of the operations.

Table 1.10
Equivalent Gray code of decimal numbers

AND		Output	OR		Output	NOT	Output
Inputs		Output	Inputs		Output	Input	Output
x	y	z = x.y	x	y	z = x + y	x	z = x'

0	0	0	0	0	0	0	1
0	1	0	0	1	1	1	0
1	0	0	1	0	1		
1	1	1	1	1	1		

1.8 SUMMARY

In this unit, you have studied about number systems, binary codes, binary arithmetic and logic functions. Initially, various types of number systems which are used in digital computers such as binary, octal and hexadecimal are discussed. As the decimal number system is more convenient for us to use in daily life, therefore, conversion of the numbers from any number systems to decimal and decimal to other number system is discussed. The computation in digital computers is mostly done in binary; therefore, the number conversion from all the number systems to binary and binary to other number systems is also discussed. Binary codes are also useful in many computer applications; therefore, various types of binary codes such as BCD, Exess-3 and gray codes are discussed. Thereafter, binary arithmetic such as binary addition and subtractions are discussed. Finally, logic functions such as AND, OR and NOT are discussed.

1.9 GLOSSARY

Base of a number system: - The number of distinct symbols (digits) used in a number system.

BCD (Binary-coded decimal): - A code for representing decimal numbers is which each decimal digit is represented by its 4-bit binary code.

Binary number system: - A number system with base (or radix) 2. The two digits used to represent any number are: 0, 1.

Bits: - Digits in binary number system are called bits.

Byte: - A group of eight bits.

Code: - A system of representation of numeric, alphabets or special characters in a binary form for processing and transmission using digital techniques.

Complement: - Inversion of the value of a binary number, variable, or expression.

Decimal number system: - A number system with base (or radix) 10. The ten digits used to represent any number are: 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9.

Excess-3 code: - A BCD code formed by adding 3(0011) to the BCD equivalent of the decimal number.

Gray code: - A code in which only one bit changes between successive numbers.

Hexadecimal number system: - A number system that uses digits 0 through 9 and the alphabets A through F. Its base (or radix) is 16.

Least significant bit (LSB): - The right-most bit of a binary number. It has the least weight.

Most significant bit (MSB): - The left-most bit of a binary number.

Nibble: - A group of four bits.

Non-weighted code: - A binary code which does not use weights for representing a number.

Octal number system: - A number system with base (or radix) 8 that uses digits 0, 1, 2, 3, 4, 5, 6, and 7.

Radix: - Same as the base.

Self complementary codes: - Complement of decimal digit can be obtained by complementing the bits of its code.

Weighted code: - A binary code in which weight is assigned to each position in the number.

1.10 REFERENCES

1. Digital Logic and Computer Design by M. Morris Mano, Pearson.

2. Modern Digital Electronics by R. P. Jain, TMH, 2010.

1.11 SUGGESTED READINGS

1. Digital Fundamentals,10th Ed, Floyd T L, Prentice Hall, 2009.

1.12 TERMINAL QUESTIONS

1.12.1 Short Answer type

1. What is radix in a number system?

2. Differentiate binary number system and Binary Coded Decimal.

3. Define terms MSB an LSB in binary number system.

5. Why Excess-3 codes are called non-weighted codes and what is the advantage of these codes?

6. Describe Gray codes. What is the advantage of Gray codes?

7. What is the difference between Arithmetic and Logic operations?

8. Define AND and OR logic operations with daily life examples.

1.12.2 Numerical Answer type

1. Determine the decimal numbers represented of the following binary numbers:

(a) 101001   (b) 111101   (c) 10001110

(d) 1100.100   (e) 101.0011   (f) 1110.1110

2. Convert the following decimal numbers into equivalent binary numbers:

(a) 57   (b) 255   (c) 31.90   (d) 26.25

3. Convert the following numbers from decimal to octal and hexadecimal.

(a) 875   (b) 9835   (c) 327.125

4. Convert the following numbers from binary to octal and hexadecimal.

(a) 11011100.101010   (b) 01010011.010101   (c) 10110011

5. Convert the base of the following numbers

(a) $(347.25)_8$ = ($)_{10}$ (b) $(F3.D8)_{16}$ = ($)_{10}$

(c) $(41.60)_8$ =   ($)_2$ (d) $(5B.A9)_{16}$ = ($)_2$

(e) $(507.25)_8$ = ($)_{16}$ (f) $(E3.B4)_{16}$ = ($)_8$

6. Encode the following decimal numbers in BCD and Excess-3 codes:

(a) 406   (b) 27.89   (c) 230.5

7. Convert the following BCD and Excess-3 codes in equivalent decimal:

(a) $(100001000111.10000101)_{BCD}$ (b) $(010110010111.10010001)_{BCD}$

(c) $(100111001000.10010101)_{EX-3}$ (d) $(101110000100.10101011)_{EX-3}$

8. Do the following arithmetic operations:

(a) 1101 + 1011   (b) 11010.1101 + 1001.01

(c) 11001 - 10010   (d) 101.1011 - 010.1110

1.12.3 Objective type questions

1. Which of the following binary numbers represents largest decimal number?

(a) 100000   (b) 11101   (c) 1000.1110   (d) 11111.111

2. Decimal equivalent of largest 3 digit octal number is

(a) 63   (b) 64   (c) 512   (d) 511

3. Which of the following numbers is not valid in the number system with radix 6?

(a) 13   (b) 64   (c) 512   (d) 011

4. Excess – 3 code of a decimal number can be obtained by

(a) Adding 3 to the equivalent binary number.

(b) Adding 3 to the equivalent BCD number.

(c) Adding 3 to the each digit in equivalent BCD number.

(d) All of Above.

1.13 ANSWERS

1.13.1 Self Assessment Questions (SAQs):

1(a) $2^5 + 2^4 + 2^3 + 2^1 + 2^0 = 59$

1(b) $2^{-1} + 2^{-2} + 2^{-5} = 0.78125$

1(c) $2^6 + 2^5 + 2^2 + 2^0 + 2^{-1} + 2^{-4} = 101.5625$

1(d) $2^4 + 2^2 + 2^{-1} + 2^{-3} + 2^{-4} = 20.6875$

2 (a)

2	597	
	298	1
	149	0
	74	1
	37	0
	18	1
	9	0
	4	1
	2	0
	1	0
	0	1

$(597)_{10} = (1001010101)_2$

2 (b)

	Multiplication	Integer
$0.895 \times 2 =$	1.79	1
$0.79 \times 2 -$	1.58	1
$0.58 \times 2 =$	1.16	1
$0.16 \times 2 =$	0.32	0
$0.32 \times 2 =$	0.64	0

$$(0.895)_{10} = (0.11100)_2$$

2 (c) $(35.875)_{10} = (100011.111)_2$ **(d)** $(247.45)_{10} = (1111011.0111)_2$

3 (a) $(426.27)_8 = (278.359375)_{10}$ **(b)** $(A09.F6)_{16} = (2569.9609375)_{10}$

  (c) $(423.21)_5 = (113.44)_{10}$ **(d)** $(123.21)_4 = (27.5625)_{10}$

4 (a) $(426.27)_8 = (100010110.010111)_2$

  (b) $(A09.F6)_{16} = (001101011111.11011000)_2$

  (c) $(423.21)_5 = (113.44)_{10} = (1110001.0111)_2$

  (d) $(123.21)_4 = (27.5625)_{10} = (11011.1001)_2$

5(a) $(426.27)_8 = (100010110.010111)_2 = (116.5C)_{16}$

  (b) $(35F.D8)_{16} = (001101011111.11011000)_2 = (1537.66)_8$

  (c) $(426.27)_8 = (100010110.010111)_2 = (10112.113)_4$

  (d) $(425.25)_6 = (161.4722)_{10} = (241.3616)_8$

6. Correct option is (c) 457.28 as it has 8 and 8 is not an octal number

7. Correct options are:

  (b) A number from any base can be converted to decimal number directly.

  (d) Hexadecimal and Octal number can be converted to binary directly.

  (e) A number from a number system can be converted to the number system with different base by first converting it into decimal.

8 (a) $(876.27)_{10} = (100001110110.00100111)_{BCD} = (101110101001.01011010)_{EX-3}$

  (b) $(254.21)_{10} = (001001010100.00100001)_{BCD} = (010110000111.01010100)_{EX-3}$

  (c) $(541.29)_{10} = (010101000001.00101001)_{BCD} = (100001110100.01011100)_{EX-3}$

  (d) $(891.56)_{10} = (100010010001.01010110)_{BCD} = (101111000100.10001001)_{EX-3}$

9 (a) $(100101100011.10010111)_{BCD} = (963.97)_{10}$

  (b) $(010010000111.00011001)_{BCD} = (487.19)_{10}$

  (c) $(101101111100.10110111)_{EX-3} = (849.84)_{10}$

  (d) $(100111000100.10001001)_{EX-3} = (691.56)_{10}$

10. Correct option is (b) 10100111 as 1010 is not a valid BCD code.

11.

		0	1	1	1	0		Carry
			1	0	0	1	1	1	Augend
	+	1	0	1	1	1	0	Addend
	1	0	1	0	1	0	1	Sum

12.

		1	1	1	1	1		Carry
			1	0	1	0	1	Augend
	+	1	0	1	0	1	1	Addend
	1	0	0	0	0	0	0	Sum

13.

	1	1	1	0	0		Borrow
	1	0	0	0	1	1	Minuend
-		1	0	1	0	1	Subtranend
	0	0	1	1	1	0	Difference

14.

		0	1	1	1	0		Borrow
		1	1	0	0	0	1	Minuend
-	1	0	0	1	1	1	Subtranend
		0	0	1	0	1	0	Difference

1.13.2 Terminal Questions: Numerical type questions

1(a) 41   **(b)** 61

 (c) 142   **(d)** 12.5

 (e) 5.1815   **(f)** 14.875

2(a) 111001   **(b)** 1111111

 (c) 11111.11101   **(d)** 11010.01

3(a) $(875)_{10} = (1553)_8 = (36B)_{16}$

 (b) $(9835)_{10} = (23153)_8 = (266B)_{16}$

 (c) $(327.125)_{10} = (507.1)_8 = (147.2)_{16}$

4(a) $(11011100.101010)_2 = (334.52)_8 = (DC.A8)_{16}$

 (b) $(01010011.010101)_2 = (123.25)_8 = (53.54)_{16}$

 (c) $10110011 = (263)_8 = (B3)_{16}$

5(a) $(347.25)_8 = (231.328125)_{10}$ **(b)** $(F3.D8)_{16} = (243.84375)_{10}$

(c) $(41.60)_8 = (100001.110000)_2$ **(d)** $(5B.A9)_{16} = (01011011.10101001)_2$

(e) $(507.25)_8 = (147.54)_{16}$ **(f)** $(E3.B4)_{16} = (343.56)_8$

6(a) $(406)_{10} = (010000000110)_{BCD} = (011100111001)_{EX-3}$

 (b) $(27.89)_{10} = (00100111.10001001)_{BCD} = (01011010.10111100)_{EX-3}$

 (c) $(230.5)_{10} = (001000110000.0101)_{BCD} = (010101100011.1000)_{EX-3}$

7(a) $(100001000111.10000101)_{BCD} = (847.85)_{10}$

 (b) $(010110010111.10010001)_{BCD} = (597.91)_{10}$

 (c) $(100111001000.10010101)_{EX-3} = (695.62)_{10}$

 (d) $(101110000100.10101011)_{EX-3} = (851.78)_{10}$

8(a) 11000   **(b)** 100100.0001   **(c)** 00111   **(d)** 010.11010

1.13.3 Objective type questions

1. The correct option is (a) 100000

2. The correct option is (d) 511

3. The correct option is (a) 63

4. The correct option is (c) Adding 3 to the each digit in equivalent BCD number.

UNIT 2   Combinational Circuits

Structure

2.1 INTRODUCTION

Designing of modern digital computers or digital circuits requires the implementation of complex Boolean functions or expressions. A Boolean expression is a combination of binary variables which can have one of two possible values, logic "0" and logic "1", and logical operators which are used to establish the relations between binary variables (such as AND, NOT, and OR).

Boolean algebra is a system that has its own set of rules or laws to deal with Boolean expressions. An expression of Boolean algebra can have an infinite number of variables all labelled individually to represent inputs to the expression. For example, in the logical expression of Y = BC + A', there are three input variables A, B, and C. Here, each of the variables can only be a '0' or a '1'.

Physical elements used to implement these functions (AND, OR and NOT) are called Logic Gates. Some other logic gates are also designed to reduce the implementation complexity of Boolean expressions. For example: NAND, NOR, XOR and XNOR gates. Size of the architecture depends upon the required number of logic gates. The hardware complexity can be reduced by minimizing the Boolean expressions. To minimize these expressions, different methods which are based on Boolean algebra's set of rules or laws, such as K-map minimization method are developed.

In this unit, Boolean algebra is introduced as a way to express logic functions algebraically. Initially, we will discuss about different laws of Boolean algebra. Then, we will learn about different forms of Boolean expression. Thereafter, different logic gates and how these gates are used to implement Boolean expressions will be discussed. Finally, we will learn the simplification Boolean functions to achieve economical gate implementations.

2.2 OBJECTIVES

After studying this unit, we will learn about-

- Boolean algebra
- Sum of Product (SOP) and Product of Sum (POS) forms
- Logic Gates
- Implementation of Boolean expressions using logic gates
- K- map Simplification

2.3 Boolean Algebra

In the middle of 19th century, an English mathematician George Boole developed rules for manipulations of binary variables, known as Boolean algebra. This is the basis of all digital systems like computers, calculators, etc.

2.3.1 Boolean Variables

A discreet variable that can have only two values is known as Boolean variable. If X is a Boolean variable, it can be denoted as:

$$X = \text{'0' or False}$$

$$X = \text{'1' or True}$$

2.3.2 Boolean Functions

A function which can be expressed in terms of binary variables, logic operators (AND, OR and NOT) and equal sign is known as Boolean function. For example, a Boolean function of three binary variables X_1, X_2 and X_3, can be given as:

$$f(X_1, X_2, X_3) = X_1.X_2 + X_1\overline{X_3}$$

A Boolean function can have only two values '0' and '1'. For a unique combination of inputs, Boolean function can be either '1' or '0'. In the previous example for the input combination, X_1 = '1', X_2 = '0' and X_3 = '0', the function output will be '1' and for the input combination, X_1 = '0', X_2 = '0' and X_3 = '0', the function output will be '0'. Sometimes the function and the binary variables are represented by English Alphabets. For example, the function given in the previous example can also be represented as:

$$Z = A.B + A.\overline{C}$$

2.3.3 Truth Table

A truth table is a table of all possible combinations of the input variables showing the relation between the values that input variables may take and the corresponding output of the Boolean function. For n input variables, total number of possible combinations are 2^n. For example, in the Boolean function $Z = A.B + A.\overline{C}$, the number of input variables are 3, therefore, total number of possible combinations are $2^3 = 8$. The truth table for this function can be given as Table 2.1.

Table 2.1
Truth Table of the Boolean expression $Z = A.B + A.\overline{C}$

Inputs	output

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

The values of the output in the truth table can be obtained by putting the values of A, B and C in the expression. For example, for ABC = "000", the expression will be F = 0.0 + 0.1 = 0. Similarly, for the input combination ABC = "001", the expression will be F = 0.0 + 0.0 = 1. In the same manner, output for all the input combinations can be filled in the truth table.

Example 2.1: Draw the truth table for the following functions:

$$F_1 = \bar{A}.B + B.C$$
$$F_2 = A + \bar{B}.C$$

Solution: For filling the truth table, the input values are put in the expression and function is calculated. For example, for ABC = "000", the expression will be F_1 = 1.0 + 0.0 = 0 and F_2 = 0 + 1.0 = 0. The final truth table of the functions can be given as

Table 2.2
Truth Table of the Boolean expression $F_1 = \bar{A}.B + B.C$ and $F_2 = A + \bar{B}.C$

Inputs			outputs	
A	B	C	F_1	F_2
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2.3.4 Fundamental Properties of Boolean Algebra

2.3.4.1 Conventions

Most of the properties of Boolean algebra are analogues to regular algebra. For example; the parentheses establish the calculation priorities as in regular algebra. All the properties can be

demonstrated through Perfect Induction, that is, by verifying the validity of each combination of values assumed by the variables in the expression. In the Boolean algebra, AND operation is prioritized over OR.

2.3.4.2 Literals

Literals are the number of input variables that make up a Boolean expression (not same as number of variables). For example in the expression

$$F = A\bar{B} + B\bar{A}$$

the number of variables are two A and B and number of literals are four A, B , $\bar{A}$, $\bar{B}$.

2.3.4.3 Laws of Boolean Algebra

A Boolean expression can be represented in various ways. A set of rules or laws of Boolean algebra which are followed to convert a Boolean expression from one form to another, commonly known as the Laws of Boolean Algebra. Basic laws of Boolean algebra are as follows:

i) Duality Principle

If a given expression is valid, its dual expression is also valid. The dual expression is obtained by switching the OR with the AND, and the '0' constants with the '1' constants from the original expression. For example

$$X + 1 = 1$$
$$\text{Dual:} \quad X.0 = 0$$

ii) Commutative Law

Commutative law states that the order in which ORing or ANDing of binary variables is done makes no difference. For example

$$A + B = B + A$$
$$A.B = B.A$$

iii) Associative Law

Associative law states that it makes no difference in what order the variables are grouped when ANDing or ORing of more than two variables is done. For example

$$A + (B + C) = (A + B) + C$$
$$A.(B.C) = (A.B).C$$

iv) Distributive Law

If both the operators (OR and AND) are involved with three or more literals than according to distributive law,

$$A.(B + C) = A.B + A.C$$
$$A+ (B.C) = (A + B).(A + C)$$

v) Annulment Law

According to Annulment law, a term ANDed with a '0' results in a '0', and ORed with a '1' results in '1'. For example

$$A + 1 = 1$$
$$A.0 = 0$$

vi) Identity Law

According to Identity law, a term ORed with a '0' or ANDed with a '1' will always equal that term. For example

$$A + 0 = A$$
$$A.1 = A$$

vii) Idempotent Law

According to Idempotent Law, An input that is ANDed or ORed with itself is equal to that input. For example

$$A + A = A$$
$$A.A = A$$

viii) Complement Law

According to Complement Law, A term ANDed with its complement equals '0', and a term ORed with its complement equals '1'. For example

$$A + \bar{A} = 1$$
$$A.\bar{A} = 0$$

ix) Double Negation Law

According to Double Negation Law, A term that is inverted twice is equal to the original term. For example

$$\bar{\bar{A}} = A$$

x) Absorption Law

This law enables a reduction in a complicated expression to a simpler one by absorbing like terms. For example

$$A + (A.B) = A$$

$$A.(A+B) = A$$

All the laws can be verified using truth tables as the output doesn't change after applying any of the laws of Boolean algebra. It can be observed using following example

Example 2.2: Verify the following laws using distributive law

i) Distributive law $A + (B.C) = (A + B).(A + C)$

ii) Absorption Law $A + (A.B) = A$

Solution: The expressions can be verified by considering L.H.S as F_1 and R.H.S as F_2 as given below:

i.
Table 2.3
Truth Table of the Boolean expression $F_1 = A + (B.C)$ and $F_2 = (A + B).(A + C)$

Inputs			Outputs	
A	B	C	F_1	F_2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

ii.
Table 2.4
Truth Table of the Boolean expression $F_1 = A + (A.B)$ and $F_2 = A$

Inputs		Outputs	
A	B	F_1	F_2
0	0	0	0
0	1	0	0
1	0	1	1
1	1	1	1

In the above truth tables F_1 and F_2 are same for all the input combinations, therefore, laws are verified.

These laws can be used to simplify the Boolean expressions. The procedure of simplification using Boolean algebra laws can be best understood using following examples.

Example 2.3: Simplify the following Boolean functions to a minimum number of literals.

(1) $x'y + xy$

(2) $xy + x'z + yz$

(3) x(x'+y)

(4) (x + y)(x' + z)(y + z)

Solution: 1. $x'y + xy - (x' + x)y$

$$= (1).y \text{ (Using Complement law x' + x =1)}$$

$$= y \text{ (Using Identity law 1.y = y)}$$

2. $xy + x'z + yz = xy + x'z + (1)yz$ (Using Identity law yz =1.yz)

$$= xy + x'z + (x + x')yz \text{ (Using Complement law x' + x}$$
=1)

$$= xy + xyz + x'z + x'yz \text{ (Using Associative law)}$$

$$= xy(1 + z) + x'z(1 + y)$$

$$= xy + x'z$$

3. $x(x' + y) - xx' + y$

$$= y \text{ (Using Complement law x'x =0 and using Identity law 0 + y =}$$
y)

4. $(x + y)(x' + z)(y + z)$

$$= (x + y)(x' + z)(xx' + y + z)$$
(Using identity law y + z = 0 + y + z and using Complement law xx'
=0)

$$- (x + y)(x' + z)(x + y + z)(x' + y + z)$$
 (Using Distributive law xx'+y+z = (x+y+z)(x'+y+z))

$$= (x + y)(1 + z)(x' + z)(1 + y)$$

$$= (x + y)(x' + z)$$

2.3.5 De Morgan's Law

A mathematician, De Morgan proposed two theorems that are an important part of Boolean algebra. In practical terms, De Morgan's theorems provide mathematical verification of the

equivalency of the NAND and negative-OR gates and the equivalency of the NOR and negative-AND gates. One of De Morgan's theorems is stated as follows:

"The complement of two or more ANDed variables is equivalent to the OR of the complements of the individual variables." The formula for expressing this theorem for two variables is

$$\overline{xy} = \bar{x} + \bar{y}$$

De Morgan's first law can be proved using the truth table 2.1.

Table 2.5
Truth Table to prove De Morgan's First Law

x	y	xy	$\overline{xy}$	$\bar{x}$	$\bar{y}$	$\bar{x} + \bar{y}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

De Morgan's second theorem is stated as follows:

The complement of two or more ORed variables is equivalent to the AND of the complements of the individual variables. The formula for expressing this theorem for two variables is

$$\overline{x + y} = \bar{x}.\bar{y}$$

De Morgan's Second law can also be proved using the Truth Table. De Morgan's law is very useful in finding the complement of a Boolean function. It can be seen from the following examples.

Example 2.4: Find the complement of the function $F = x'yz' + xy'z'$.

Solution: Complement of F can be written as

$$F' = (x'yz' + xy'z')'$$

Using De Morgan's Law

$$F' = (x'yz')'.(xy'z')'$$

$$F' = ((x')' + (y)' + (z')').((x)' + (y')' + (z')')$$

$$F' = (x + y' + z).(x' + y + z)$$

Example 2.5: Find the complement of the function $F = (x' + y + z').(x + y' + z')$.

Solution: Complement of F can be written as

$$F' = ((x'+y+z').(x+y'+z'))'$$

Using De Morgan's Law

$$F' = (x'+y+z')' + (x+y'+z')'$$

$$F' = ((x')'.(y)'.(z')') + ((x)'.(y')'.(z')')$$

$$F' = xy'z + x'yz$$

Self Assessment Question (SAQ) 1: Obtain the truth table of the following functions:

(a) (A' + B)(B' + C)

(b) wxy' + wxz' + w'x'z

Self Assessment Question (SAQ) 2: Simplify the following Boolean functions to a minimum number of literals.

(a) $x'y' + xy + xy'$

(b) $(x + y)(x' + y)$

(c) $x'y + xy' + xy + x'y'$

(d) $xy + x(wz + wz')$

Self Assessment Question (SAQ) 3: Find the complement of the following expressions:

(a) $xy' + x'y$

(b) $(x + y' + z)(x' + z')(x + y)$

2.4 SOP and POS forms

A binary expression can be represented in mainly two forms: one is Sum of Product (SOP) form and other is Product of Sum (POS) form. The description of these forms is as follows:

2.4.1 SOP (Sum of Product) form

When a binary expression is represented as OR of ANDed functions (Summing of products), it is called in Sum of Product form. For example:

$$F = XYZ + XY\bar{Z} + X\bar{Y}Z + \bar{X}\bar{Y}Z$$

In the above expression, all the terms contains all the three variables X, Y and Z. Each term in the expression is called minterm and the expression is called sum of minterms. This form of the Boolean expression is called Canonical form. This form can be obtained directly from the truth table as shown in the example below.

Example 2.6: Find the expression in the sum of minterms form for the Truth Table 2.6.

Table 2.6

Inputs			Output
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Solution: In the Table 2.6, the output is 1 for the input combinations ABC = 001, 011, 101 and 110. These terms can be expressed as $\bar{A}\bar{B}C$, $\bar{A}BC$, $A\bar{B}C$, $AB\bar{C}$ and the expression can be given as:

$$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + AB\bar{C}$$

In the canonical form, all the terms require all the variables; therefore the expression has many literals. However the Boolean expressions are represented as minimum number of literals to reduce the hardware complexity. The Boolean function in which a term can have any number of variables in a term is called in standard form. For example

$$F = XY + \bar{Y}Z$$

Standard form can be obtained from the Canonical form and vice versa using the laws of Boolean algebra given in Sec. 2.3. It can be seen in the following examples:

Example 2.7: Express the Boolean function $F = xy + x'z$ in the canonical form.

Solution: The expression can be converted in the canonical form as follows:

$$F = xy + x'z$$

$$F = xy(z + z') + x'z(y + y')$$

$$F = xyz + xyz' + x'zy + x'zy'$$

Example 2.8: Find the expression in the standard form (as minimum number of literals) for the Truth Table 2.6.

Solution: The expression in the canonical can be given as:

$$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + AB\bar{C}$$

It can be converted in the standard form as:

$$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + AB\bar{C}$$

$$F - \bar{A}\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C + A\bar{B}C + AB\bar{C} \qquad (A = A + A)$$

$$F = \bar{A}C(B + \bar{B}) + (\bar{A} + A)\bar{B}C + AB\bar{C}$$

$$F = \bar{A}C + BC + AB\bar{C} \qquad (\bar{A} = 1 \text{ and } B + \bar{B} = 1)$$

2.4.2 POS (Product of Sum) form

When a binary expression is represented as ANDed of ORed functions (Product of Sums), it is called in Product of Sum form. For example:

$$F = (X + Y + Z).(X + Y + \bar{Z}).(X + \bar{Y} + Z)(\bar{X} + \bar{Y} + Z)$$

In the above expression, all the terms contains all the three variables X, Y and Z. Each term in the expression is called Maxterm and the expression is called product of maxterms. Similar to the SOP form, this form of the Boolean expression is also called canonical form.

To obtain this form from the truth table conventions are changed as taken in SOP form. In this form, '0' is taken as variable and '1' as the complement of the variable, and AND of ORed terms with '0' output are taken to form the expression. It can be best understood from the following example.

Example 2.9: Find the expression in the sum of minterms form for the Truth Table 2.6.

Solution: In the Table 2.6, the output is 0 for the input combinations ABC = 000, 010, 100 and 111. These terms can be expressed as $A + B + C$, $A + \bar{B} + C$, $\bar{A} + B + C$ and $\bar{A} + \bar{B} + \bar{C}$, and the expression can be given as:

$$F = (A + B + C)(A + \bar{B} + C)(\bar{A} + B + C)(\bar{A} + \bar{B} + \bar{C})$$

Similar to SOP form, the Boolean function in which a term can have any number of variables in a tem is called in standard form. For example

$$F = (X + Y)(\bar{Y} + Z)$$

Similar to SOP form, standard POS form can be obtained from the canonical form and vice versa using the laws of Boolean algebra given in Sec. 2.3. It can be seen in the following examples:

Example 2.10: Express the Boolean function $F = (x+y)(x'+z)$ in the canonical form.

Solution: The expression can be converted in the canonical form as follows:

$$F = (x + y)(x' + z)$$

$$F = (x + y + zz')(x' + z + yy')$$

$$F = (x + y + z)(x + y + z')(x' + z + y)(x' + z + y')$$

Example 2.11: Find the expression in the standard POS form (as minimum number of literals) for the Truth Table 2.6.

Solution: The expression in the canonical can be given as:

$$F = (A + B + C)(A + \bar{B} + C)(\bar{A} + B + C)(\bar{A} + \bar{B} + \bar{C})$$

It can be converted in the standard form as:

$$F = (A + B + C)(A + \bar{B} + C)(\bar{A} + B + C)(\bar{A} + \bar{B} + \bar{C})$$

$$F = (A + B + C)(A + \bar{B} + C)(A + B + C)(\bar{A} + B + C)(\bar{A} + \bar{B} + \bar{C}) \qquad (A = A.A)$$

$$F = (A + B\bar{B} + C)(A\bar{A} + B + C)(\bar{A} + \bar{B} + \bar{C})$$

$$F = (A + C)(B + C)(\bar{A} + \bar{B} + \bar{C})$$

The SOP form can be converted in POS form and vice versa using the laws of Boolean algebra. A other form of Boolean algebra is also possible which uses combination of POS and SOP forms. For example; $(xy + y'z)(x'y + z)$.

Self Assessment Question (SAQ) 4: Obtain the Canonical POS and SOP expressions for the Truth Table 2.7 and convert them as minimum number of literals.

Table 2.7

Inputs			Output
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Self Assessment Question (SAQ) 5: Convert the following expressions in the Canonical forms.

(a) $x'y' + xz'$

(b) $(x + y' + z)(x' + z')(x + y)$

2.5 Logic Gates

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

Since Boolean functions are expressed in terms of AND, OR, and NOT operations, it is convenient to implement a Boolean function with these types of physical gates. Implementation of the large Boolean functions may be complex using the basic gates (AND, OR and NOT) only. Therefore, some other logic gates such that NAND, NOR, XOR and XNOR, are also designed. Other than these logic gates, a buffer is also used in some applications. Description of these gates is as follows:

2.5.1 Types of Logic Gates

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

1. AND gate: - AND gate is used to perform AND operation. The Basic AND gate has two input and one output. The output of AND gate is '0', if any of the input is '0'. A graphical symbol of two input AND gate and its truth table are shown in Fig. 2.1(a) and Fig. 2.1(b), respectively. A multiple input AND gate can also be designed, for which output is '1' only when all the inputs are '1'. A graphical representation of multi-input AND gate is shown in Fig. 2.1 (c).

2. OR gate: - OR gate is used to perform OR operation. The output of OR gate is '1' if any of the OR input is '1'. A two input OR gate symbol and its truth table are shown in Fig. 2.2(a) and Fig. 2.2(b), respectively. A multi-input

x	F

OR gate can also be designed, similar to multi-input AND gate. A graphical representation of multiple input OR gate is shown in Fig. 2.2 (c).

$F= xy$

$F= x_1x_2.....x_n$
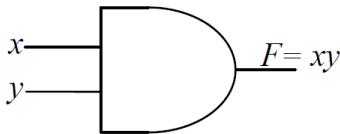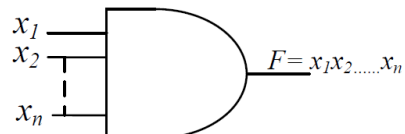
(a) (b) (c)

Fig 2.1 (a) 2-input AND gate, (b) Truth Table of AND gate (c) Multiple input AND gate

$F= x+y$

$F= x_1+x_2+...+x_n$
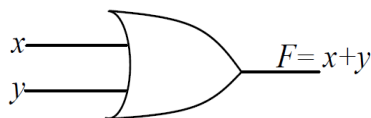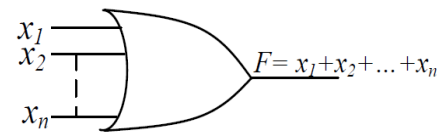
(a) (b) (c)

Fig 2.2 (a) 2-input OR gate, (b) Truth Table of OR gate (c) Multiple input OR gate

3. NOT gate: - NOT gate is used to invert the input. It has only one input and one output. The output of NOT gate is '1' if input is '0' and vice-versa. A NOT gate symbol and its truth table are shown in Fig. 2.3 (a) and Fig. 2.3 (b), respectively.

0	1
1	0

(a)   (b)
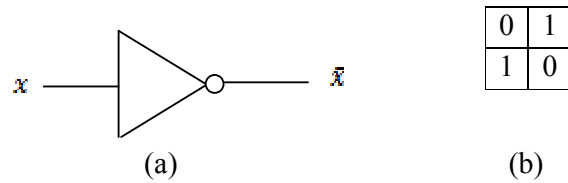
Fig 2.3 (a) NOT gate symbol, (b) Truth Table of NOT gate

4. Buffer: - Buffer provides same output as the input. It has only one input and one output similar to the NOT gate. It is used in some applications to provide delay or isolate the input and output. A buffer symbol and its truth table are shown in Fig. 2.4 (a) and Fig. 2.4 (b), respectively.

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

(a)   (b)

Fig 2.4 (a) Buffer symbol, (b) Truth Table of Buffer

5. NAND gate: - NAND gate provides complement of AND gate. It can be realized by adding an inverter at the output of AND gate. It is also called universal gate as all the other gates and Boolean expressions can be realised using NAND gates only. Its symbol and truth table are shown in Fig. 2.5(a) and Fig. 2.5(b), respectively.

$F = \overline{xy}$

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

(a)   (b)
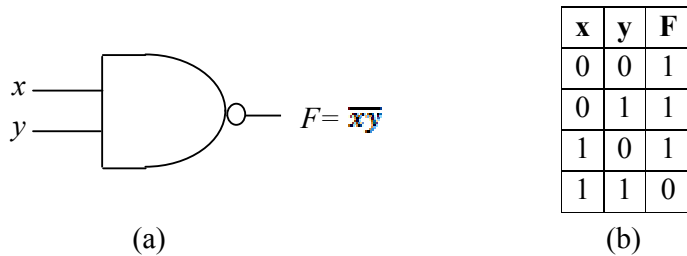
Fig 2.5 (a) 2-input NAND gate, (b) Truth Table of NAND gate

x	F
0	0
1	1

6. NOR gate: - NOR gate provides complement of OR gate and can be realized by adding an inverter at the output of OR gate. It is another universal gate which can be used to realise other gates and Boolean expressions. Its symbol and truth table are shown in Fig. 2.6(a) and Fig. 2.6(b), respectively.

$F = \overline{x + y}$

(a)   (b)
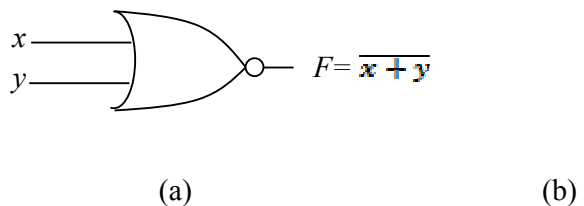
Fig 2.6 (a) 2-input NOR gate, (b) Truth Table of NOR gate

7. XOR gate: - XOR gate is sometimes called Exclusive OR gate or EX-OR gate. Two input XOR gate provides logic '1' at the output when both the inputs are different and logic '0' for same inputs. The logical expression of XOR gate can be given as $F = x\bar{y} + \bar{x}y$. Its symbol and truth table are shown in Fig. 2.7(a) and Fig. 2.7(b), respectively. A multiple input XOR gate provides output '1', if odd numbers of inputs are 1.

$$F = x\bar{y} + \bar{x}y$$
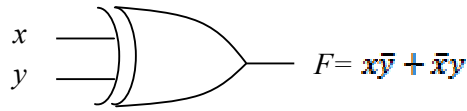
(a)   (b)

Fig 2.7 (a) 2-input XOR gate, (b) Truth Table of XOR gate

6. XNOR gate: - XNOR gate provides complement of XOR gate. A Two input XNOR gate provides logic '0' at the output when both the inputs are different and logic '1' for same inputs. The logical expression of XNOR gate can be given as $F = \bar{x}\bar{y} + xy$. Its symbol and truth table are shown in Fig. 2.8(a) and Fig. 2.8(b), respectively.

$$F = \bar{x}\bar{y} + xy$$

x	y	F
0	0	1
0	1	0
1	0	0
1	1	1
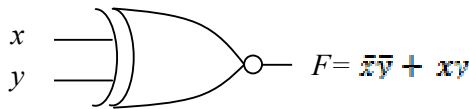
(a)   (b)

Fig 2.8 (a) 2-input XNOR gate, (b) Truth Table of XNOR gate

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

2.5.2 Implementation of Boolean expressions using Logic gates

A Boolean expression can be implement by directly putting the AND, OR and NOT gates as per the expression. Implementation can be understood using following examples.

Example 2.14: Implement the following Boolean expression using Logic gates.

$$F = AB + \bar{B}C$$

Solution: Implementation of the given function can be given as:

$$F = AB + \bar{B}C$$

42
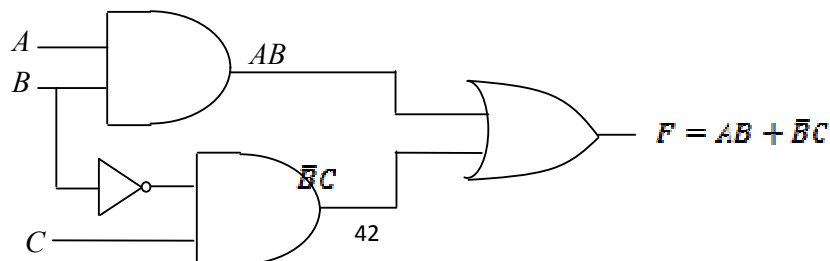
Example 2.15: Implement the following Boolean expressions using Logic gates.

$$F_1 = A + \bar{B}C$$
$$F_2 = B + CD$$

Solution: Implementation of the given function can be given as:
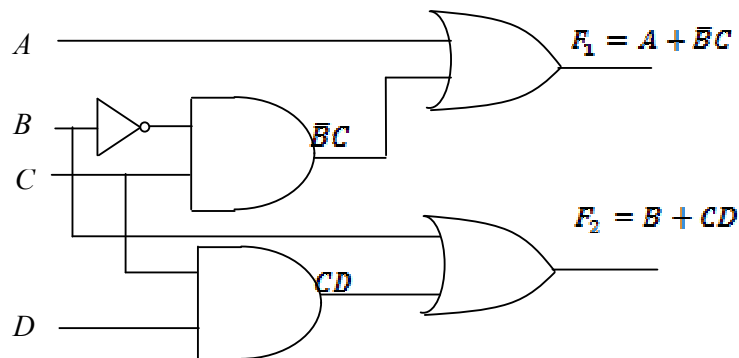
Self Assessment Question (SAQ) 6: Which of these logic gates produces output as logic '1' only when all the inputs are at logic '0'?

(a) AND   (b) OR   (c) NAND   (d) NOR

Self Assessment Question (SAQ) 7: Implement XOR gate using AND, OR and NOT gates.

Self Assessment Question (SAQ) 8: Which of these gates are called Universal Gate?

(a) NAND and NOR   (b) AND and OR   (c) XOR and XNOR   (d) NOT

Self Assessment Question (SAQ) 9: Implement the following Boolean functions using Logic gates.

(a) $x'y' + xz'$

(b) $(x + y' + z)(x' + z')(x + y)$

2.6 Simplification of Boolean Functions

In the implementation of Boolean functions, hardware complexity is directly related to the complexity of the algebraic expression from which the function is implemented. Although the truth table representation of a function is unique, it can appear in many different forms. Boolean functions may be simplified by means of Boolean algebraic laws as discussed in Section 2.3. However, this procedure is complicated and sometimes it becomes difficult to get fully minimized expression using this procedure. Karnaugh Map or K-Map method is an effective method of minimization of Boolean function for the five or less variables.

2.6.1 K-Map Simplification

K-Map is a diagram made up of squares. Each square represents a unique combination of all the input variables. The number of squares in the K-Map is equal to the number of possible combinations with all input variables. i.e., for n input variables, number of squares will be 2^n. For two variables, the number of squares is $2^2 = 4$ which are arranged as shown in Fig. 2.9.
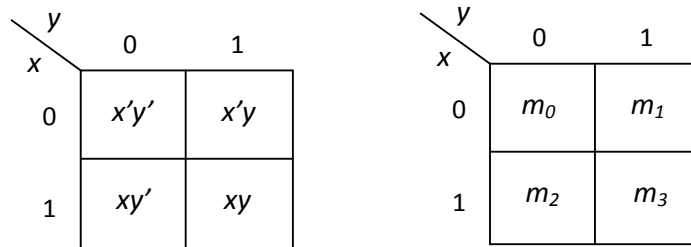
Fig 2.9 2-Variable K-map in terms of (a) variables, and (b) minterms

A two variable expression $F = AB + A'B$ can be represented using K-map by filling 1 at the place of these combinations as given in 2.10 (a). To minimize the expression, grouping of nearby 1's is done as shown in 2.10 (b).
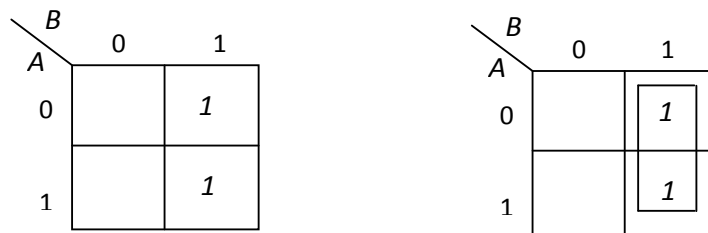
Fig 2.10 K-map for the expression $F = AB + A'B$ (a) before grouping, and (b) after grouping

Now, the expression for a group can be obtained by considering the literals which remain constant within group. The literals which change within the group are not considered. In the group of fig. 2.10 (b), value of B is constant as '1', while A is changing as 0 and 1 both. Therefore, the minimized expression can be taken as

$$F = B$$

Here, 1 is considered as variable while 0 is considered as the complement of the variable. The groups in the K-map cannot be made by taking any number of 1's. In a group, the possible number of 1's should be in the power of 2. For example: 2, 4, 8, 16 etc.

2.6.2 3-variable K-Map

As name implies, 3-variable K-map is used to reduce the expressions having 3-variables. The number of squares in 3-variable K-map are $2^3 = 8$ which are arranged as shown in Fig. 2.11. Fig. 2.11(a) shows the combinations of the variable and Fig. 2.11(b) shows these

combinations as minterms with a decimal number. These decimal numbers can be obtained by converting the input binary values into decimal. For example: input "000" can be referred to as '0', input "001" can be referred to as '1', input "010" can be referred to as '2' and so on.

yz \ x	00	01	11	10
0	x'y'z'	x'y'z	x'yz	x'yz'
1	xy'z'	xy'z	xyz	xyz'

yz \ x	00	01	11	10
0	m_0	m_1	m_3	m_2
1	m_4	m_5	m_7	m_6

Fig 2.11 3-Variable K-map in terms of (a) variables, and (b) minterms

To minimize the expression using 3-variable K-map, the pairs or quad can be made by grouping 2 or 4 nearby 1's, respectively. In the minimized expression, the literals which remain constant within the group are taken. To make the groups, 1's in first and last rows or 1's in first and last columns can also be considered as nearby '1'. To minimize the Boolean expression up to minimum number of literals, the grouping is started with largest group possible and all the ones should be grouped. If a '1' could not be grouped with any other '1' then group of single '1' is made. The minimization can be best understood from following examples.

Example 2.16: Minimize the following expression using K-map.

$$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + AB\bar{C}$$

Solution:

$$F = \bar{A}C + \bar{B}C + AB\bar{C}$$
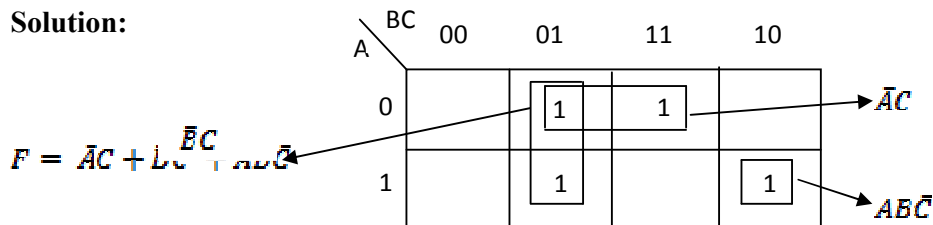
In the K-map 1's are filled at the places of the minterms given in the expression. After that groups of nearby 1's are made. In the first group, it can be seen that BC = "01" is constant while A is changing, therefore the expression of the group will be $\bar{B}C$. Similarly, other terms will be $\bar{A}C$. 1 for $AB\bar{C}$ could not be paired with any other 1, therefore, it will be taken as it is. The minimized expression will be

$$F = \bar{B}C + \bar{A}C + AB\bar{C}$$

Most of the time, the expression is given as the summation of decimal numbers equivalent to the minterms. To minimize these types of expressions, 1's are filled at the places according to the fig. 2.11(b) and minimization is done as described above. It can be seen from the following example.

Example 2.17: Minimize the following expression using K-map.

$$F = \Sigma(0,2,4,6,7)$$

Solution:

$$F = AB + \bar{C}$$
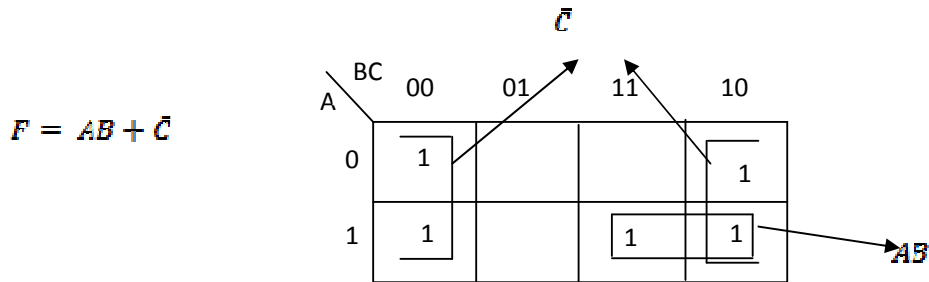
In the K-map 1's are filled at the places of the minterms given in the summation and grouping is done. Largest group contains four 1's and other group contains two 1's. In the quad 0 corresponding to C is unchanged, therefore, its expression will be $\bar{C}$. Similarly, for the pair expression will be AB and the minimized expression will be

$$F = AB + \bar{C}$$

2.6.3 4-variable K-Map

In 4-variable K-map, the number of squares are $2^4 = 16$ which are arranged as shown in Fig. 2.12.

AB\CD	00	01	11	10
00	A'B' C'D'	A'B' C'D	A'B' CD	A'B' CD'
01	A'B C'D'	A'B C'D	A'B CD	A'B CD'
11	AB C'D'	AB C'D	AB CD	AB CD'
10	AB' C'D'	AB' C'D	A'B CD	A'B CD'

AB\CD	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}
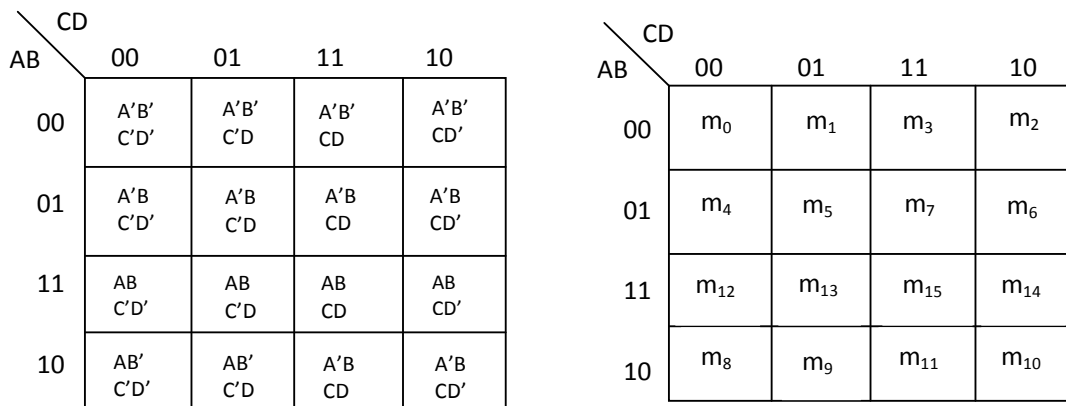
Fig 2.12 4-Variable K-map in terms of (a) variables, and (b) minterms

To minimize the expression using 4-variable K-map, the pairs, quad or octet can be made by grouping 2, 4 or 8 nearby minterms, respectively similar to 3-variable K-map. In 4-variable K-map, 1's at the four corners can also be taken to form a group. The minimization can be best understood from the following examples.

Example 2.18: Minimize the following expression using K-map.

$$F = A'B'C'D' + A'B'C'D + A'B'CD' + A'BCD' + AB'C'D + AB'CD' + AB'C'D'$$

Solution:

In the above K-map, there a   the first group all the corner 1's are included which gives expression $B'D'$. The second group contains 2 ones in first row and 2 ones in last row and gives $B'C'$. The third group is a pair which gives $A'CD'$. The final expression is

$$F = A'CD' + B'C' + B'D'$$

Example 2.19: Minimize the following expression using K-map.

$$F = \sum m(1,2,3,5,7,9,11,13,15)$$

Solution:

In the above K-map, there are 2 groups, 1 octet and one pair. The Octet gives expression B. Pair gives $A'B'C$. The final expression is

$$F = D + A'B'C'$$

2.6.4 POS Simplification

Product of sum form of the simplified Boolean function can be obtained by a minor modification in the K-map. The 1's placed in the different squares of the map represent the minterms while the vacant squares denote the complement of the function which can be filled with 0's. To obtain the simplified POS expression these 0's are grouped in place of 1's. The grouping method remains the same as described above. The only change occurs in the convention. In POS form '0' is treated as variable while '1' is treated as complement of the variable. POS simplification can be understood using following examples.

Example 2.20: Simplify the following expression in product of sum form using K-map.

$$F = \sum m(1,2,3,5,7,9,11,13,15)$$

Solution: The above expression in POS form can be written as

$$F = \prod (0,4,6,8,10,12,14)$$

It can be filled in K-map as follows

CD AB	00	01	11	10
00	0			
01	0			0
11	0			0
10	0			0

In the above K-map, there are 3 quads. 1'st quad is first column and in other two quads two 0's are from first column and two from last column. In first column 0's corresponding to C and D are unchanged, therefore, the expression will be $C + D$, similarily, expressions for other two quads will be $\bar{B} + D$ and $\bar{A} + D$, and the final expression will be

$$F = (C + D)(\bar{B} + D)(\bar{A} + D)$$

2.6.5 Don't Care Condition

Till now, we have discussed the Boolean functions which specify the conditions under which the function is equal to '1' and it is considered that the function is equal to '0' for the rest of the minterms. However, in some applications, the function is not specified for certain combinations of the variables. For example, in BCD, binary values of 10 to 15 are not specified. Functions that have unspecified outputs for some input combinations are called don't care terms. These don't-care conditions can be used on a map to provide further simplification of the Boolean expression.

In K-Map, don't care terms are specified with X. It is not necessary to consider these X for making the groups however, don't care terms are taken in the groups if these are helpful in the reduction of the expression. It can be understood from the following example.

Example 2.21: Minimize the following expression using K-map.

$$F(A, B, C, D) = \sum (0, 1, 2, 3, 7, 8, 10)$$

$$d(A, B, C, D) = \sum (5, 6, 11, 15)$$

Solution: In the K-map, 1's are filled in the squares corresponding to the minterms given in F and X are filled in the squares corresponding o the minterms given in d. Groups are then made by taking all the 1's in account and X which helps in minimization. The K-map is given below.

In the K-map given above, there are 3 quads. only 1 don't care term 6 is considered in making the groups as using this one pair of 3 and 7 is converted to a quad and provides reduced expression. The final expression is

$F = A'B' + B'D' + A'C$

Self Assessment Question (SAQ) 10: Minimize the following expression using K-map.

$$F(x, y, z) = \sum (1, 2, 3, 4, 7)$$

Self Assessment Question (SAQ) 11: Minimize the following expression using K-map in SOP and POS forms.

$$F(A, B, C, D) = \sum (0, 1, 2, 3, 4, 7, 11, 15)$$

Self Assessment Question (SAQ) 12: Minimize the following expression using K-map.

$$F(w, x, y, z) = \sum (1,2,3,5,7,9,11,13,15)$$

$$d(w, x, y, z) = \sum (4, 6, 8, 10)$$

2.7 SUMMARY

In this unit, you have studied about Boolean algebra, minimization of Boolean functions, logic gates and implementation of Boolean functions using logic gates. Initially, various laws of Boolean algebra are discussed. Thereafter, simplification of Boolean functions using these laws is discussed. After that, different types of representations of Boolean expressions such as SOP and POS, and Canonical and standard forms are discussed. After that, different types of logic gates and implementation of Boolean functions using logic gates are discussed. K-

Map method is an effective tool of minimization of Boolean function which is also discussed in this unit.

2.8 GLOSSARY

Binary Variables: - Variables that can take one of two binary values '0' or '1'.

Boolean Algebra: - Rules for manipulations of binary variables.

Boolean Functions: - An expression which is formed using binary variables, logic operations and equal sign.

Canonical form: In SOP or POS forms, if every term has all the variables, the form is called canonical form.

K- map: - Karnaugh map.

Literals: - The number of input variables that make up a Boolean expression..

Logic Gates: - Physical circuits used to implement logic functions.

Maxterms: - In the POS form if every term has all the input variables, each term in the expression is called maxterm.

Minterms: - In the SOP form if every term has all the input variables, each term in the expression is called minterm.

POS: - Product of Sum form.

SOP: - Sum of Product form.

2.9 REFERENCES

1. Digital Logic and Computer Design by M. Morris Mano, Pearson.

2. Modern Digital Electronics by R. P. Jain, TMH, 2010.

2.10 SUGGESTED READINGS

1. Digital Fundamentals,10th Ed, Floyd T L, Prentice Hall, 2009.

2.11 TERMINAL QUESTIONS

2.11.1 Short Answer type

1. What is the significance of Boolean algebra in digital system?

2. Describe associative law and prove it using truth table..

3. Differentiate between variable and literals.

4. What is the difference between canonical and standard form?

5. Differentiate between SOP and POS forms.

6. What is the difference between Arithmetic and Logic operations?

7. Why NAND and NOR gate are called universal gates?

2.11.2 Numerical Answer type

1. Using the theorems of Boolean algebra, minimize the following logical expression:

(a) $A + BA + BC + \bar{B}C$

(b) $\bar{A}(A + B) + \bar{C} + BC$

(c) $\bar{x}\bar{y} + xy + \bar{x}y$

(d) $(x + y)(x + y')$

2. Using De Morgan's theorem, find the complement of the following expressions:

(a) $F = x'y' + x'z + y'z$ (b) $F = (y + z')(x + y)(y' + z)$

3. For the truth table given below, find the expression in

(a) Canonical SOP form   (b) Standard SOP form

(c) Canonical POS form   (d) Standard POS form

Table 2.8

Inputs			Output
x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

4. Implement the following functions using logic gates

(a) $Y = (A + B) + \overline{AB}$

(b) $F = x(y + z)z'$

(c) $Z = xy\overline{(y+z)}$

(d) $y = \overline{x_1\overline{x_2}\overline{x_3}} + x_1(\overline{x_2} + x_2\overline{x_3})$

5. Minimize the following expressions using K-map

(a) $F(A, B, C) = \Sigma(0, 2, 3, 4, 6)$

(b) $F = xyz' + xyz + x'y'z' + x'yz'$

(c) $F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 9, 10)$

(d) $F(A, B, C, D) = \Sigma(0, 1, 2, 8, 10, 11, 14, 15)$, $d(A, B, C, D) = \Sigma(4, 5, 6, 9)$

2.11.3 Objective type questions

1. Which of the following is not true:

(a) $xy(z + x') = xyz$ (b) $xyz + xy' + x = x$

(c) $x.\overline{xy} = 0$ (d) $x\overline{y} + \overline{x}y = \overline{x}\overline{y} + xy$

2. In a 4-variable K-map, if all the squares are filled with 1, the output will be

(a) 1   (b) x   (c) 0   (d) $\bar{x}$

3. For a two input logic gate, which of these gates has output 1 if all the inputs are 1?

(a) AND   (b) OR   (c) XNOR   (d) All of the above

4. Two design a three input NAND gate, how many two-input NAND gates are required?

(a) 2   (b) 3   (c) 4   (d) 5

5. Which of these gates produces an output 1 if odd number of inputs are 1?

(a) AND   (b) XOR   (c) XNOR   (d) OR

2.12 ANSWERS

2.12.1 Self Assessment Questions (SAQs):

1 Obtain the truth table of the following functions:

(a) If F = (A' + B)(B' + C), the truth table can be given as

52

Inputs			Output
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(b) If F = wxy' + wxz' + x'z, the truth table can be given as

Inputs				Output
w	x	y	z	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

2. (a) $x'y' + xy + xy'$

$$= x'y' + xy' + xy + xy'$$
$$= (x' + x)y' + x(y + y')$$
$$= y' + x$$

(b) $(x + y)(x' + y)$

$$= (xx' + y)$$
$$= y$$

(c) $x'y + xy' + xy + x'y'$

$$= (x + x')y + (x + x')y'$$
$$= y + y'$$

(d) $xy + x(wz + wz')$

$$= xy + xw(z + z')$$
$$= x(y + w)$$
$$= x$$

3. (a) $F = xy' + x'y$

$F' = (xy' + x'y)'$

$F' = (xy')'(x'y)'$

$F' = (x' + y'')(x'' + y')$

$F' = (x' + y)(x + y')$

(b) $F = (x + y' + z)(x' + z')(x + y)$

$F' = ((x + y' + z)(x' + z')(x + y))'$

$F' = (x + y' + z)' + (x' + z')' + (x + y)'$

$F' = x'yz' + xz + x'y'$

4. Canonical SOP expressions can be given as

$F = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + ABC$

Canonical POS expressions can be given as

$F = (A + \bar{B} + C)(\bar{A} + B + C)(\bar{A} + \bar{B} + C)$

Standard SOP expressions can be given as

$F = \bar{A}\bar{B} + BC + AC$

Standard POS expressions can be given as

$F = (\bar{B} + C)(\bar{A} + C)$

5. (a) $x'y'z' + x'y'z + xy'z' + xyz'$

(b) $(x + y' + z)(x' + y + z')(x' + y' + z')(x + y + z')(x + y + z)$

6. The correct answer is (d) NOR

7. Implement XOR gate using AND, OR and NOT gates.

8. The correct answer is (a) NAND and NOR

9. Implement the following Boolean functions using Logic gates.

(a) $x'y' + xz'$
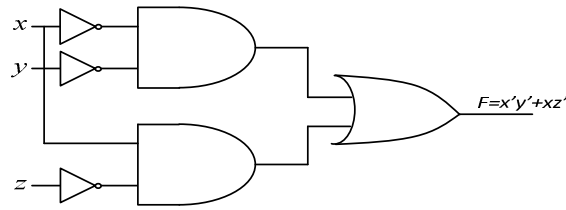
(b) $(x + y' + z)(x' + z')(x + y)$
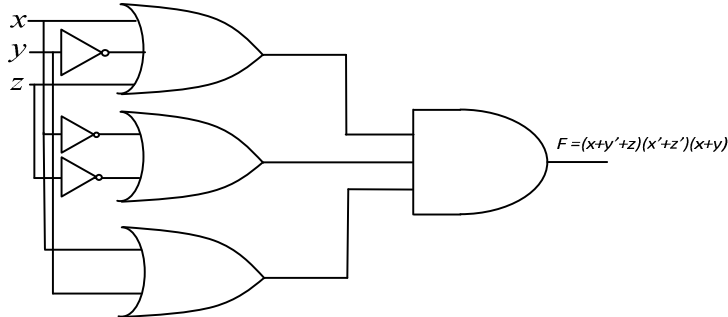
10. $F(x, y, z) = \Sigma(1,2,3,4,7)$
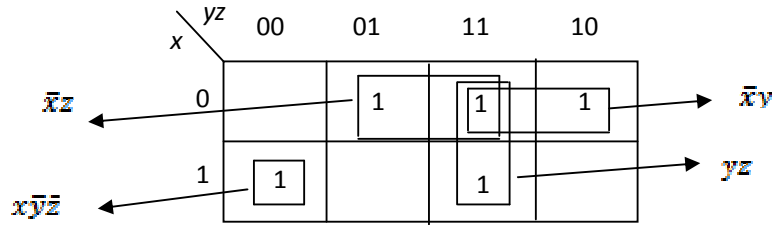
$F = \bar{x}z + \bar{x}y + yz + x\bar{y}\bar{z}$

11. $F(A, B, C, D) = \Sigma(0, 1, 2, 3, 4, 7, 11, 15)$

In SOP form
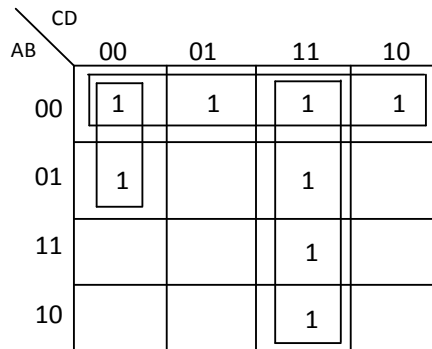
$F = \bar{A}\bar{B} + CD + \bar{A}\bar{C}\bar{D}$

In POS form
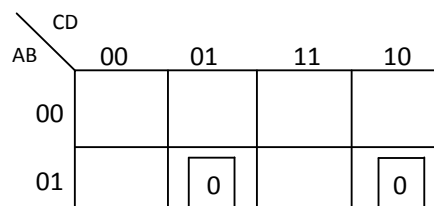
$$F - (\bar{A} + C)(\bar{A} + D)(\bar{B} + C + \bar{D})(\bar{B} + \bar{C} + D)$$

12. $F(w, x, y, z) = \sum(1,2,3,5,7,9,11,13,15), d(w, x, y, z) = \sum(4,6,8,10,14)$

wx\\yz	00	01	11	10
00		1	1	1
01	X	1	1	X
11		1	1	X
10	X	1	1	X

$$F = y + z$$

2.12.2 Terminal Questions: Numerical type questions

1(a) $A + C$

 (b) $\bar{C} + B\,C$

 (c) $\bar{x}\bar{y} + y$

 (d) x

2(a) $F' = (x + y)(x + z')(y + z')$

 (b) $F = y'z + x'y' + yz'$

3(a) $F = x'y'z + x'yz + xy'z + xyz' + xyz$

 (b) $F = (x + y + z)(x + y' + z)(x' + y + z)$

 (c) $F = z + xy$

 (d) $F = (x + z)(y + z)$

5(a) $F = A'B + C'$

(b) $F = x'z' + xy$

(c) $F = B'D' + B'C' + A'C'D$

(d) $F = CD' + AC + B'C'$ or $AC + B'D' + B'C'$ or $AC + B'D' + A'C'$

2.12.3 Objective type questions

1. The correct option is (c) $x.\overline{xy} = 0$

2. The correct option is (a) 1

3. The correct option is (d) All of the above

4. The correct option is (b) 3

4. The correct option is (c) XOR

UNIT 3   Flip Flop

3.1 INTRODUCTION

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information a bistable multivibrator. Flip-flops and latches are used as data storage elements. Flip-flops can be either level-triggered (asynchronous, transparent or opaque) or edge-triggered (synchronous, or clocked). Here we will learn about various types of flip flops.

The input must be held steady in a period around the rising edge of the clock known as the aperture. Flip-flops are subject to a problem called metastability, which can happen when two inputs, such as data and clock or clock and reset, are changing at about the same time. The metastability in flip-flops can be avoided by ensuring that the data and control inputs are held valid and constant for specified periods before and after the clock pulse, called the setup time (t_{su}) and the hold time (t_h) respectively.

A multiplexer is a combinational circuit that has 2^n input lines and a single output line. De-Multiplexer is a combinational circuit that performs the reverse operation of Multiplexer.

An Encoder is a combinational circuit that performs the reverse operation of Decoder. Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines.

3.2 OBJECTIVES

After studying this unit, you will learn about-

- Flip flops
- Different types of Flip flop
- Different types of Multiplexer
- Different types of De- Multiplexer
- Encoder
- Decoder

3.3 FLIP-FLOP: In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops and latches are used as data storage elements. A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic in electronics. When used in a finite state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.
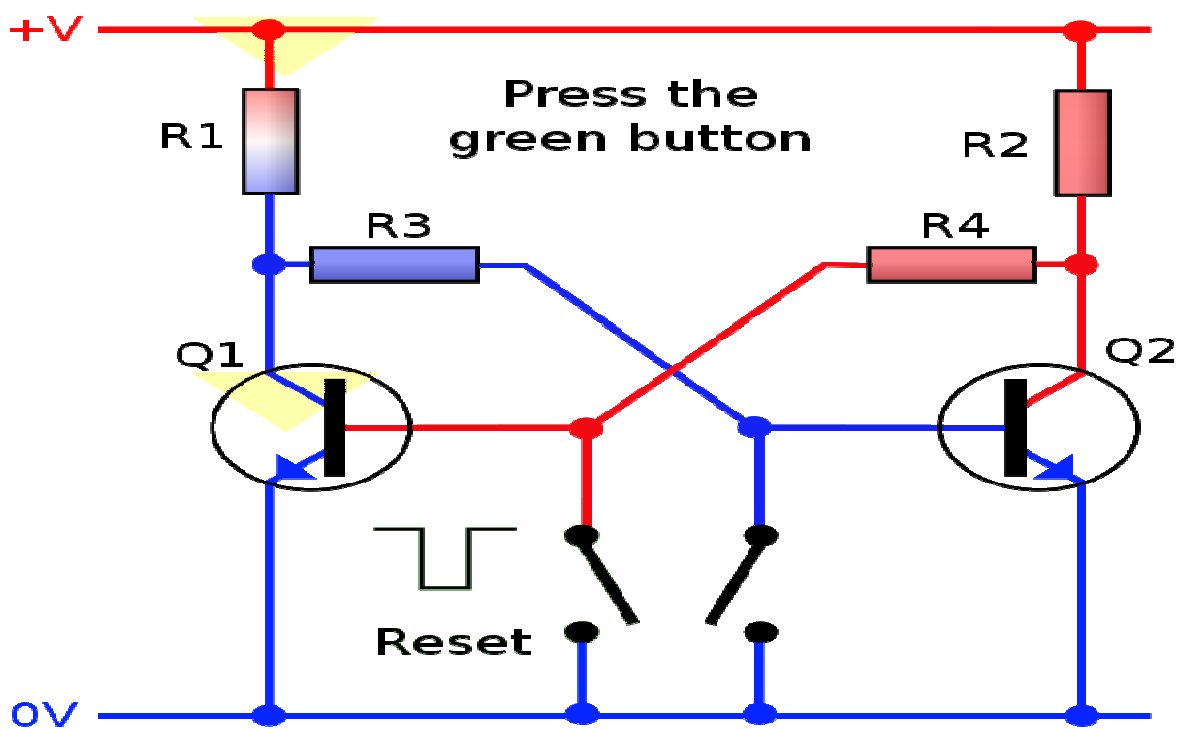
Fig. 1: SR latch

Flip-flops can be either level-triggered (asynchronous, transparent or opaque) or edge-triggered (synchronous, or clocked). The term flip-flop has historically referred generically to both level-triggered and edge-triggered circuits that store a single bit of data using gates. Recently, some authors reserve the term flip-flop exclusively for discussing clocked circuits; the simple ones are commonly called transparent latches. Using this terminology, a level-sensitive flip-flop is called a transparent latch, whereas an edge-triggered flip-flop is simply called a flip-flop. Using either terminology, the term "flip-flop" refers to a device that stores a

single bit of data, but the term "latch" may also refer to a device that stores any number of bits of data using a single trigger. The terms "edge-triggered", and "level-triggered" may be used to avoid ambiguity.

When a level-triggered latch is enabled it becomes transparent, but an edge-triggered flip-flop's output only changes on a single type (positive going or negative going) of clock edge.

3.4 FLIP-FLOP TYPES

There are following types of Flip-flops -

1) the **SR** ("set-reset"),
2) **D** ("data" or "delay"),
3) **T** ("toggle"),
4) **JK**.

3.4.1. SIMPLE SET-RESET LATCHES: When using static gates as building blocks, the most fundamental latch is the simple SR latch, where S and R stand for set and reset. It can be constructed from a pair of cross-coupled NOR or NAND logic gates the stored bit is present on the output marked Q.

3.4.2. S-R NOR LATCH: While the R and S inputs are both low, feedback maintains the Q and Q outputs in a constant state, with Q the complement of Q. If S (Set) is pulsed high while R (Reset) is held low, then the Q output is forced high, and stays high when S returns to low; similarly, if R is pulsed high while S is held low, then the Q output is forced low, and stays low when R returns to low.
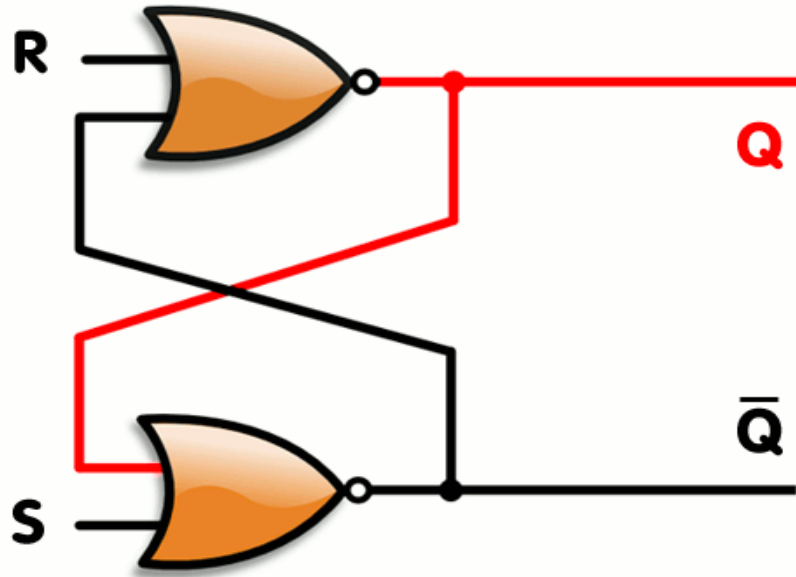
Fig.2: SR latch, constructed from a pair of cross-coupled NOR gates

SR latch Operation							
Characteristics table				Excitation table			
S	R	Qnext	Action	Q	Qnext	S	R
0	0	Q	Hold state	0	0	0	X
0	1	0	Reset	0	1	1	0
1	0	1	Set	1	0	0	1
1	1	X	Not allowed	1	1	X	0

Note: X means don't care, that is, either 0 or 1 is a valid value.

The R = S = 1 combination is called a restricted combination or a forbidden state because, as both NOR gates then output zeros, it breaks the logical equation Q = not Q. The combination is also inappropriate in circuits where both inputs may go low simultaneously (i.e. a transition

from restricted to keep). The output would lock at either 1 or 0 depending on the propagation time relations between the gates (a race condition).

To overcome the restricted combination, one can add gates to the inputs that would convert (S, R) = (1, 1) to one of the non-restricted combinations. That can be:

- Q = 1 (1, 0) – referred to s an S (dominated)-latch
- Q = 0 (0, 1) – referred to as an R (dominated)-latch

This is done in nearly every programmable logic controller.

- Keep state (0, 0) – referred to as an E-latch

Alternatively, the restricted combination can be made to toggle the output. The result is the JK latch.

3.4.3. $\overline{\text{SR}}$ NAND LATCH: The circuit shown below is a basic NAND latch. The inputs are generally designated S and R for Set and Reset respectively. Because the NAND inputs must normally be logic 1 to avoid affecting the latching action, the inputs are considered to be inverted in this circuit (or active low).
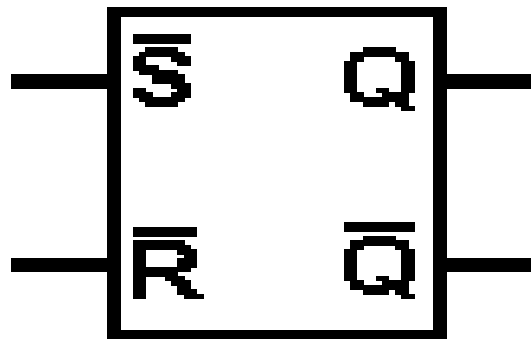
Fig.4: Symbol of $\overline{\text{SR}}$ NAND latch

The circuit uses feedback to "remember" and retain its logical state even after the controlling input signals have changed. When the S and R inputs are both high, feedback maintains the Q outputs to the previous state.
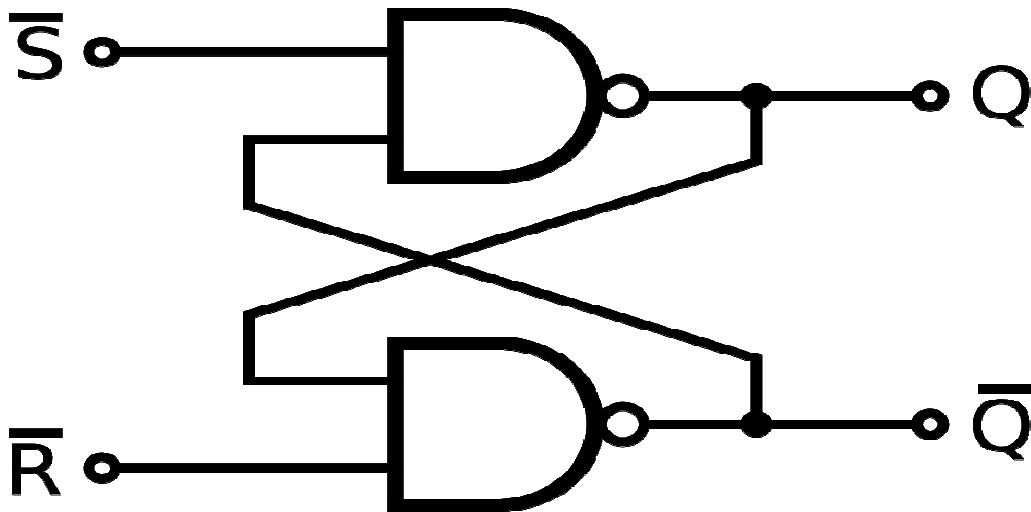
Fig.5: An SR latch constructed from cross-coupled NAND gates

$\overline{SR}$ latch operation		
S	**R**	**Action**
0	0	Q=0, Q=1, Not allowed
0	1	Q=1
1	0	Q=0
1	1	No change

3.4.4. SR AND-OR LATCH: SR latches drawn as a pair of cross-coupled components (transistors, gates, tubes, etc.) is often hard to understand for beginners. A didactically easier to understand way is to draw the latch as a single feedback loop instead of the cross-coupling. The following is an SR latch built with an AND gate with one inverted input and an OR gate. Note that the inverter is not needed for the latch functionality, but rather to make both inputs High-active.
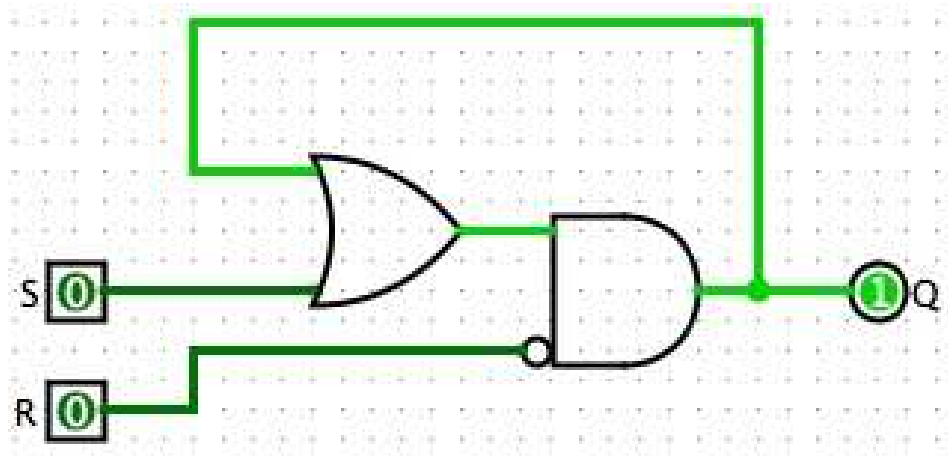
Fig.6: SR AND-OR latch

SR AND- OR latch operation		
S	R	Action
0	0	No change
0	1	Q=1
X	1	Q=0

Note that the SR AND-OR latch has the benefit that S = 1, R = 1 is well defined. In above version of the SR AND-OR latch it gives priority to the R signal over the S signal. If priority of S over R is needed, this can be achieved by connecting output Q to the output of the OR gate instead of the output of the AND gate.

The SR AND-OR latch is easier to understand, because both gates can be explained in isolation. When neither S or R is set, then both the OR gate and the AND gate are in "hold mode", i.e., their output is the input from the feedback loop. When input S = 1, then the output of the OR gate becomes 1, regardless of the other input from the feedback loop ("set mode"). When input R = 1 then the output of the AND gate becomes 0, regardless of the other input from the feedback loop ("reset mode"). And since the output Q is directly connected to the output of the AND gate, R has priority over S. Latches drawn as cross-coupled gates may look less intuitive, as the behaviour of one gate appears to be intertwined with the other gate.

3.4.5. JK LATCH: The JK latch is much less frequently used than the JK flip-flop. The JK latch follows the following state table:

JK latch truth table			
J	K	Qnext	Comment
0	0	Q	No change
0	1	0	Reset
1	0	1	Set
1	1	Q	Toggele

Hence, the JK latch is an SR latch that is made to toggle its output (oscillate between 0 and 1) when passed the input combination of 11. Unlike the JK flip-flop, the 11 input combination for the JK latch is not very useful because there is no clock that directs toggling.

3.5. D FLIP-FLOP: The D flip-flop is widely used. It is also known as a "data" or "delay" flip-flop.

The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero- order hold, or a delay line
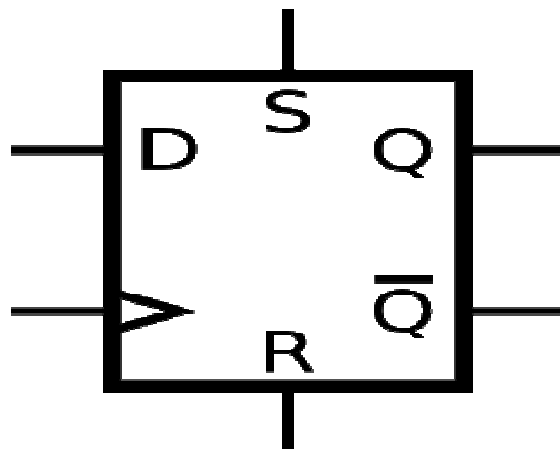
Fig.7: D flip-flop symbol

(X denotes a don't care condition, meaning the signal is irrelevant)

Most D-type flip-flops in ICs have the capability to be forced to the set or reset state (which ignores the D and clock inputs), much like an SR flip-flop. Usually, the illegal $S = R = 1$ condition is resolved in D-type flip-flops. Setting $S = R = 0$ makes the flip-flop behave as described above. Here is the truth table for the other possible S and R configurations:

Input			Output	
S	R	D	Q	Q'
0	1	X	0	1
1	0	X	1	0
1	1	X	1	1

These flip-flops are very useful, as they form the basis for shift register, which are an essential part of many electronic devices. The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. An exception is that some flip-flops have a "reset" signal input, which will reset Q (to zero), and may be either asynchronous or synchronous with the clock.

The above circuit shifts the contents of the register to the right, one bit position on each active transition of the clock. The input X is shifted into the leftmost bit position.

3.5.1. MASTER–SLAVE EDGE-TRIGGERED D FLIP-FLOP: A master–slave D flip-flop is created by connecting two gated D latches in series, and inverting the enable input to one of them. It is called master–slave because the master latch controls the slave latch's output value Q and forces the slave latch to hold its value whenever the slave latch is enabled, as the slave latch always copies its new value from the master latch and changes its value only in response to a change in the value of the master latch and clock signal.
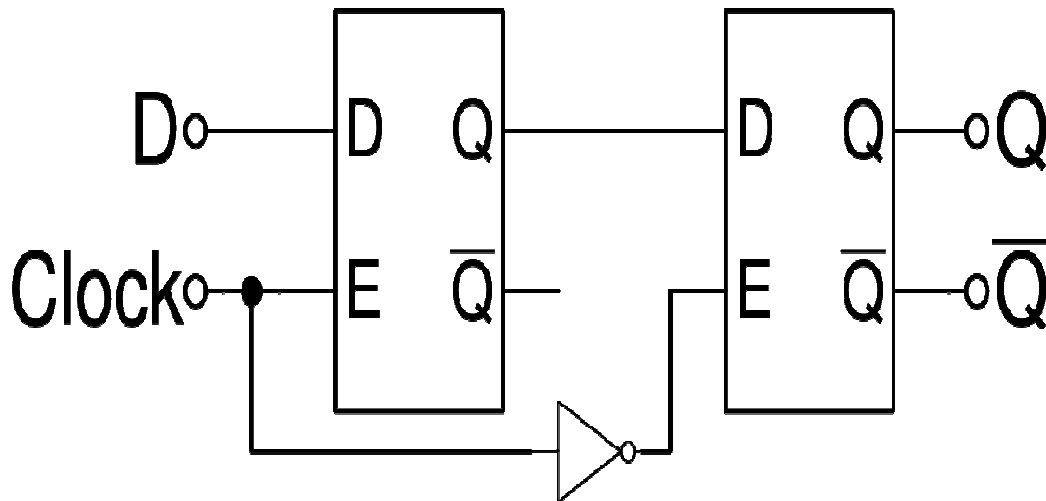
Fig.8: A master–slave D flip-flop

For a positive-edge triggered master–slave D flip-flop, when the clock signal is low (logical 0) the "enable" seen by the first or "master" D latch (the inverted clock signal) is high (logical 1). This allows the "master" latch to store the input value when the clock signal transitions from low to high. As the clock signal goes high (0 to 1) the inverted "enable" of the first latch goes low (1 to 0) and the value seen at the input to the master latch is "locked". Nearly simultaneously, the twice inverted "enable" of the second or "slave" D latch transitions from low to high (0 to 1) with the clock signal. This allows the signal captured at the rising edge of the clock by the now "locked" master latch to pass through the "slave" latch. When the clock signal returns to low (1 to 0), the output of the "slave" latch is "locked", and the value seen at the last rising edge of the clock is held while the "master" latch begins to accept new values in preparation for the next rising clock edge
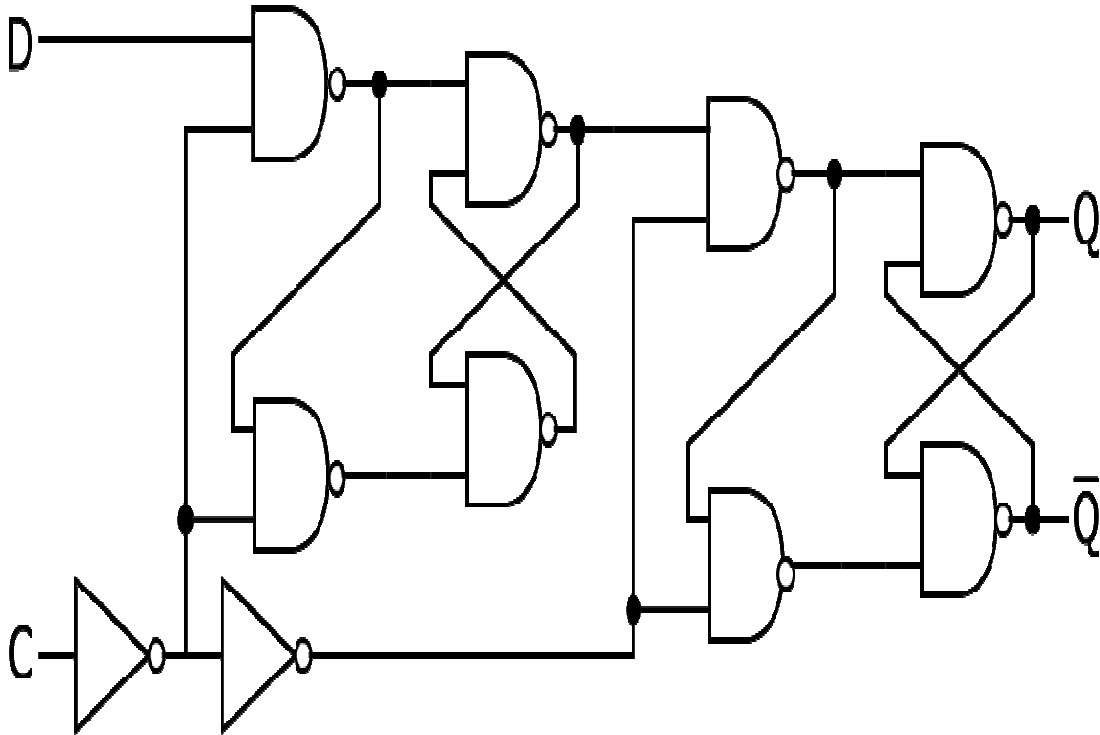
 Fig.9: An implementation of a master–slave D flip-flop that is triggered on the rising edge of the clock

Removing the leftmost inverter in the circuit creates a D-type flip-flop that strobes on the falling edge of a clock signal. This has a truth table like this:

D	Q	Qnext
0	X	0
1	X	1

3.6. T FLIP FLOP: Just like JK flip-flop, T flip flop is used. Unlike JK flip flop, in T flip flop, there is only single input with the clock input. The T flip flop is constructed by connecting both of the inputs of JK flip flop together as a single input.
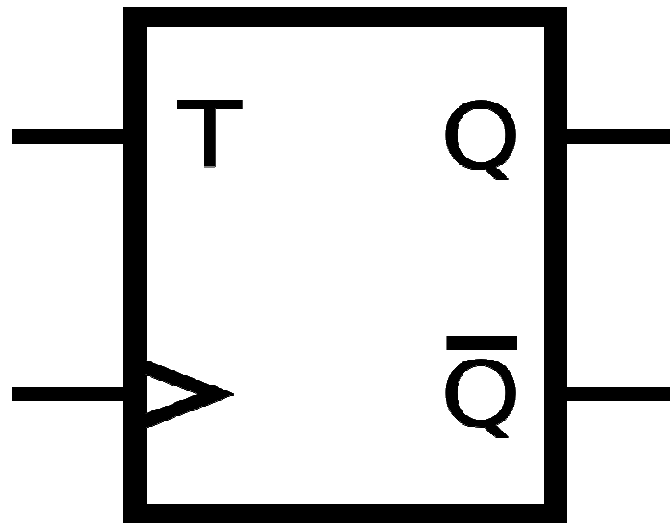
Fig.10: Symbol for a T-type flip-flop
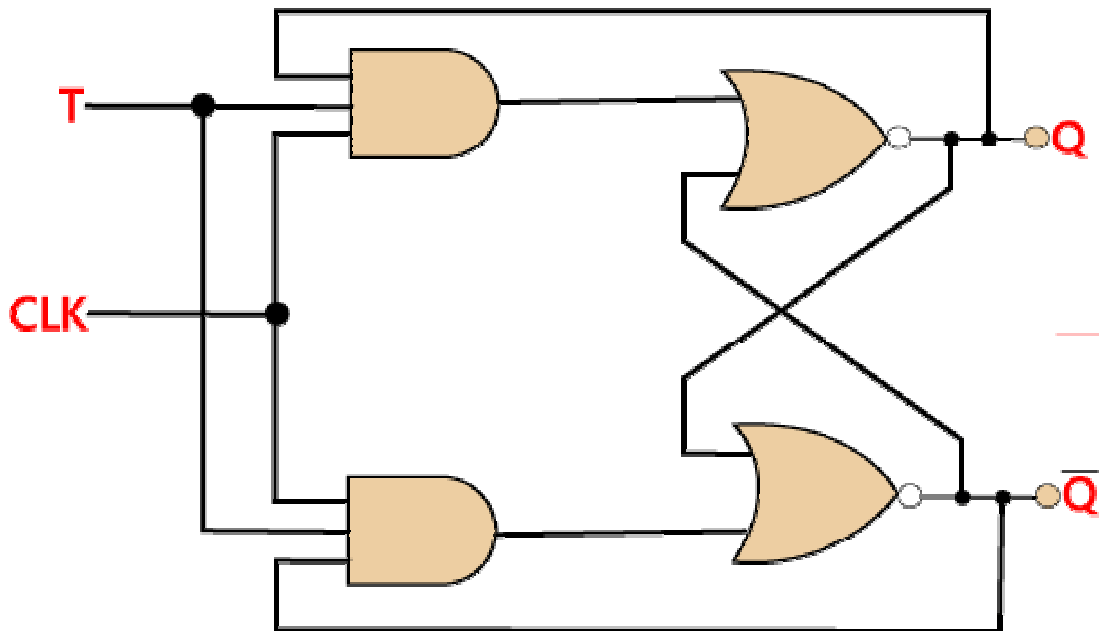
Fig.11: Toggle flip-flop

The T flip flop is also known as **Toggle flip-flop**. These T flip-flops are able to find the complement of its state.

Truth Table:

T	Y	Y'
0	0	0
1	0	1
0	1	1
1	1	0

3.7. J-K FLIP – FLOP: The JK flip flop is used to remove the drawback of the S-R flip flop, i.e., undefined states. The JK flip flop is formed by doing modification in the SR flip flop.
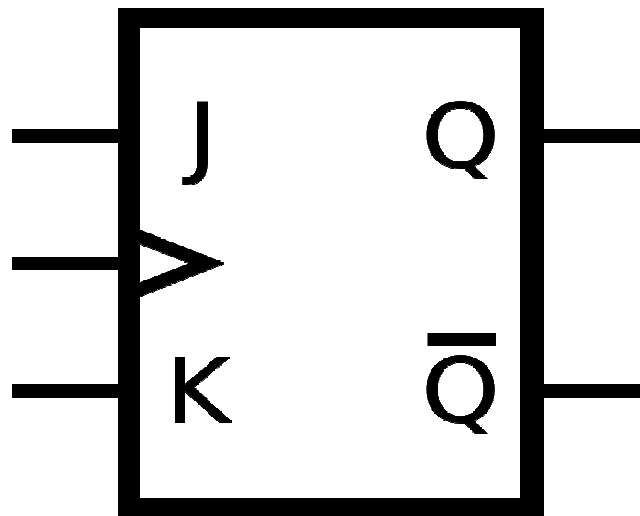
Fig.12:   A circuit symbol for a positive-edge-triggered JK flip-flop

The S-R flip flop is improved in order to construct the J-K flip flop. When S and R input is set to true, the SR flip flop gives an inaccurate result. But in the case of JK flip flop, it gives the correct output.

In J-K flip flop, if both of its inputs are different, the value of J at the next clock edge is taken by the output Y. If both of its input is low, then no change occurs, and if high at the clock edge, then from one state to the other, the output will be toggled. The JK Flip Flop is a Set or Reset Flip flop in the digital system.
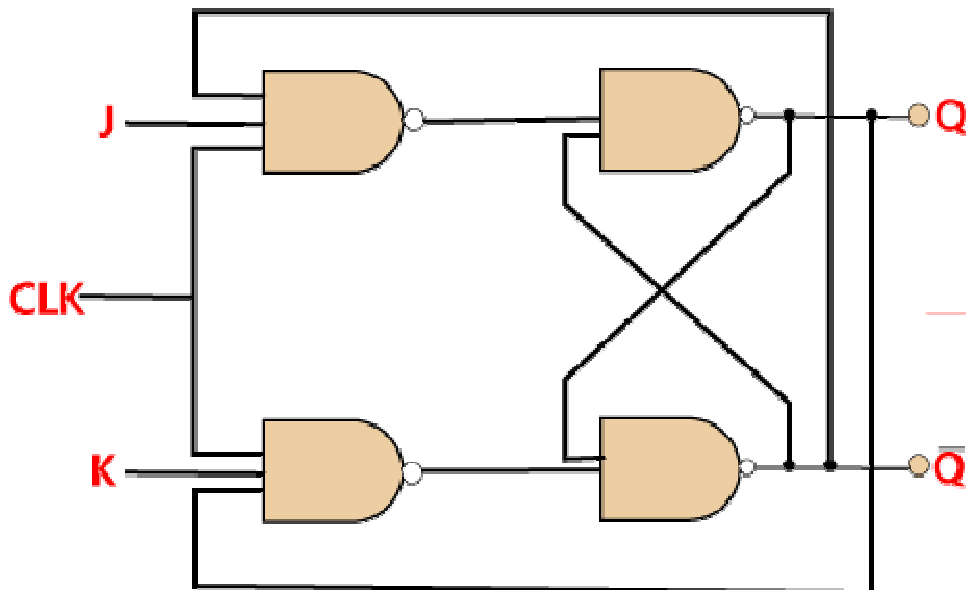
Fig.13: J-K flip flop

Truth Table:

J	K	Y	Y'
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	1
0	1	1	0

1	0	1	1
1	1	1	0

3.8. TIMING CONSIDERATIONS: The input must be held steady in a period around the rising edge of the clock known as the aperture. Imagine taking a picture of a frog on a lily-pad. Suppose the frog then jumps into the water. If you take a picture of the frog as it jumps into the water, you will get a blurry picture of the frog jumping into the water—it's not clear which state the frog was in. But if you take a picture while the frog sits steadily on the pad (or is steadily in the water), you will get a clear picture. In the same way, the input to a flip-flop must be held steady during the **aperture** of the flip-flop.
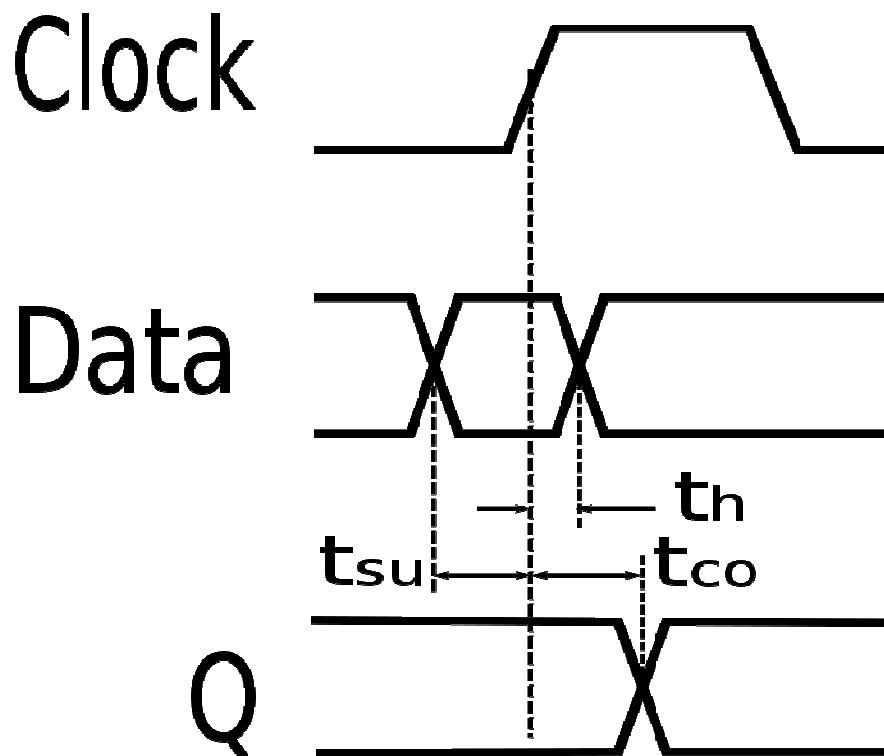
Fig.14: Flip-flop setup, hold and clock-to-output timing parameters

Setup time is the minimum amount of time the data input should be held steady **before** the clock event, so that the data is reliably sampled by the clock.

Hold time is the minimum amount of time the data input should be held steady **after** the clock event, so that the data is reliably sampled by the clock.

Aperture is the sum of setup and hold time. The data input should be held steady throughout this time period.

Recovery time is the minimum amount of time the asynchronous set or reset input should be inactive **before** the clock event, so that the data is reliably sampled by the clock. The recovery time for the asynchronous set or reset input is thereby similar to the setup time for the data input.

Removal time is the minimum amount of time the asynchronous set or reset input should be inactive **after** the clock event, so that the data is reliably sampled by the clock. The removal time for the asynchronous set or reset input is thereby similar to the hold time for the data input.

Short impulses applied to asynchronous inputs (set, reset) should not be applied completely within the recovery-removal period, or else it becomes entirely indeterminable whether the flip-flop will transition to the appropriate state. In another case, where an asynchronous signal simply makes one transition that happens to fall between the recovery/removal time, eventually the flip-flop will transition to the appropriate state, but a very short glitch may or may not appear on the output, dependent on the synchronous input signal. This second situation may or may not have significance to a circuit design.

Set and Reset (and other) signals may be either synchronous or asynchronous and therefore may be characterized with either Setup/Hold or Recovery/Removal times, and synchronicity is very dependent on the design of the flip-flop.

Differentiation between Setup/Hold and Recovery/Removal times is often necessary when verifying the timing of larger circuits because asynchronous signals may be found to be less critical than synchronous signals. The differentiation offers circuit designers the ability to define the verification conditions for these types of signals independently.

Metastability: Flip-flops are subject to a problem called metastability, which can happen when two inputs, such as data and clock or clock and reset, are changing at about the same time. When the order is not clear, within appropriate timing constraints, the result is that the output may behave unpredictably, taking many times longer than normal to settle to one state or the other, or even oscillating several times before settling. Theoretically, the time to settle down is not bounded. In a computer system, this metastability can cause corruption of data or a program crash if the state is not stable before another circuit uses its value; in particular, if two different logical paths use the output of a flip-flop, one path can interpret it as a 0 and the other as a 1 when it has not resolved to stable state, putting the machine into an inconsistent state.

The metastability in flip-flops can be avoided by ensuring that the data and control inputs are held valid and constant for specified periods before and after the clock pulse, called the **setup time** (t_{su}) and the **hold time** (t_h) respectively. These times are specified in the data sheet for the device, and are typically between a few nanoseconds and a few hundred picoseconds for modern devices. Depending upon the flip-flop's internal organization, it is possible to build a device with a zero (or even negative) setup or hold time requirement but not both simultaneously.

Unfortunately, it is not always possible to meet the setup and hold criteria, because the flip-flop may be connected to a real-time signal that could change at any time, outside the control of the designer. In this case, the best the designer can do is to reduce the probability of error to a certain level, depending on the required reliability of the circuit. One technique for suppressing metastability is to connect two or more flip-flops in a chain, so that the output of each one feeds the data input of the next, and all devices share a common clock. With this method, the probability of a metastable event can be reduced to a negligible value, but never to zero. The probability of metastability gets closer and closer to zero as the number of flip-flops connected in series is increased. The number of flip-flops being cascaded is referred to as the "ranking"; "dual-ranked" flip flops (two flip-flops in series) is a common situation.

So called metastable hardened flip-flops are available, which work by reducing the setup and hold times as much as possible, but even these cannot eliminate the problem entirely. This is because metastability is more than simply a matter of circuit design. When the transitions in the clock and the data are close together in time, the flip-flop is forced to decide which event happened first. However fast the device is made, there is always the possibility that the input

events will be so close together that it cannot detect which one happened first. It is therefore logically impossible to build a perfectly metastable-proof flip-flop. Flip-flops are sometimes characterized for a maximum settling time (the maximum time they will remain metastable under specified conditions). In this case, dual-ranked flip-flops that are clocked slower than the maximum allowed metastability time will provide proper conditioning for asynchronous (e.g., external) signals.

Propagation delay: Another important timing value for a flip-flop is the clock-to-output delay (common symbol in data sheets: t_{CO}) or propagation delay (t_P), which is the time a flip-flop takes to change its output after the clock edge. The time for a high-to-low transition (t_{PHL}) is sometimes different from the time for a low-to-high transition (t_{PLH}).

When cascading flip-flops which share the same clock (as in a shift register), it is important to ensure that the t_{CO} of a preceding flip-flop is longer than the hold time (t_h) of the following flip-flop, so data present at the input of the succeeding flip-flop is properly "shifted in" following the active edge of the clock. This relationship between t_{CO} and t_h is normally guaranteed if the flip-flops are physically identical. Furthermore, for correct operation, it is easy to verify that the clock period has to be greater than the sum $t_{su} + t_h$.

3.9. Multiplexer:
A multiplexer is a combinational circuit that has 2^n input lines and a single output line. Simply, the multiplexer is a multi-input and single-output combinational circuit. The binary information is received from the input lines and directed to the output line. On the basis of the values of the selection lines, one of these data inputs will be connected to the output.

Unlike encoder and decoder, there are n selection lines and 2^n input lines. So, there is a total of 2^N possible combinations of inputs. A multiplexer is also treated as Mux.

There are various types of the multiplexer which are as follows:

3.9.1. 2×1 Multiplexer:
In 2×1 multiplexer, there are only two inputs, i.e., A0 and A1, 1 selection line, i.e., S0 and single outputs, i.e., Y. On the basis of the combination of inputs which are present at the selection line S0, one of these 2 inputs will be connected to the output. The block diagram and the truth table of the 2×1 multiplexer are given below.

Block Diagram:
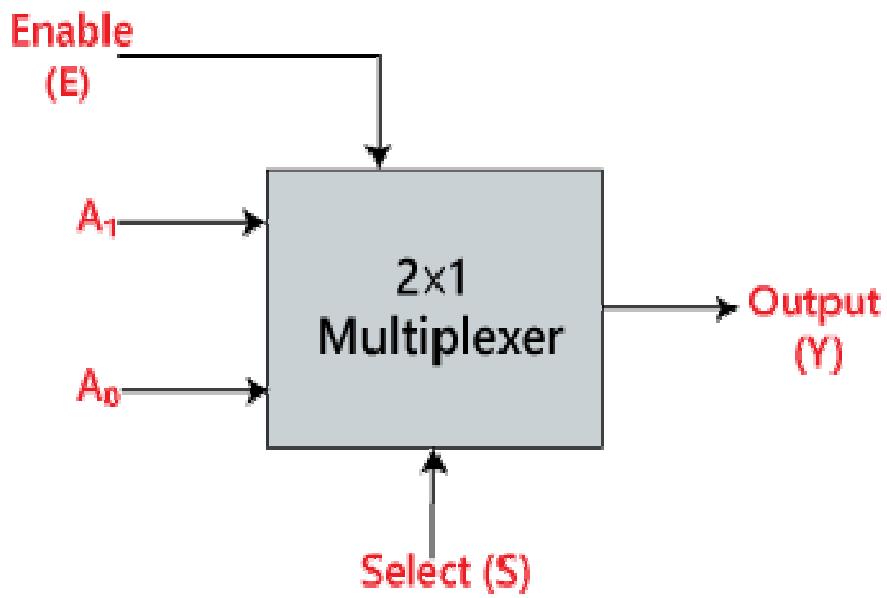
Fig.15: 2×1 multiplexer

Truth Table:

Inputs	Outputs
S0	Y
0	A0
1	A1

Logic Circuit:
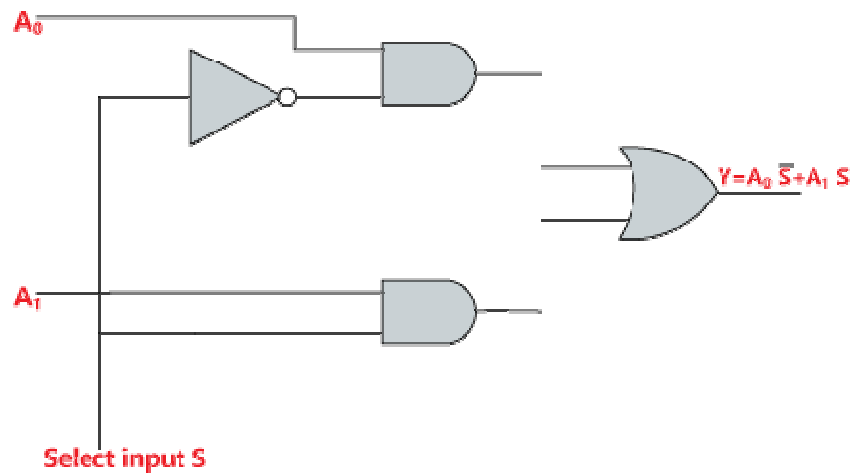
Fig.16: 2×1 multiplexer

3.9.2. 4×1 Multiplexer: In the 4×1 multiplexer, there is a total of four inputs, i.e., A0, A1, A2, and A3, 2 selection lines, i.e., S0 and S1 and single output, i.e., Y. On the basis of the combination of inputs that are present at the selection lines S0 and S1, one of these 4 inputs are connected to the output. The block diagram and the truth table of the 4×1 multiplexer are given below.

Block Diagram:
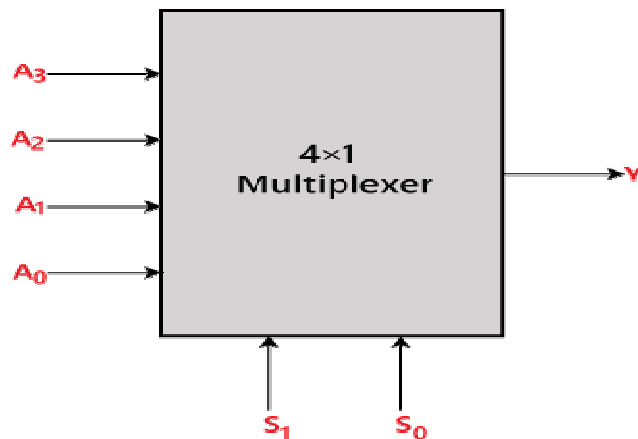
Fig.16: 4×1 multiplexer

Truth Table:

Inputs		Outputs
S1	**S0**	**Y**
0	0	A0
0	1	A1
1	0	A2
1	1	A3

Logic circuit:
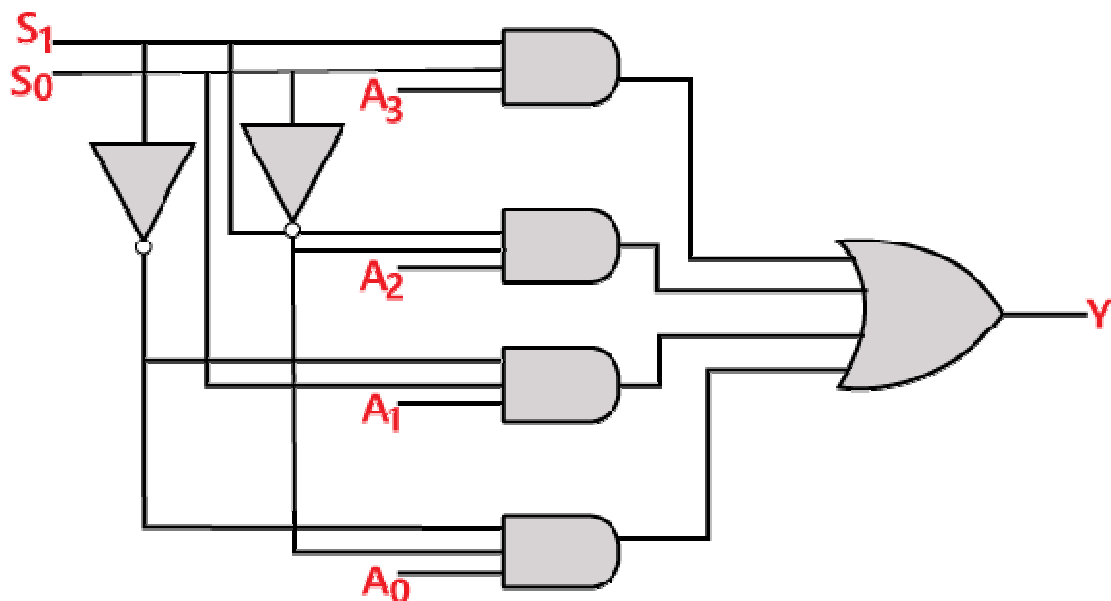
Fig.17: 4×1 Multiplexer

3.10. De-Multiplexer: De-Multiplexer is a combinational circuit that performs the reverse operation of Multiplexer. It has single input, 'n' selection lines and maximum of 2^n outputs. The input will be connected to one of these outputs based on the values of selection lines.

Since there are 'n' selection lines, there will be 2^n possible combinations of zeros and ones. So, each combination can select only one output. De-Multiplexer is also called as **De-Mux**.

3.10.1. 1x4 De-Multiplexer: 1x4 De-Multiplexer has one input I, two selection lines, s_1 & s_0 and four outputs Y_3, Y_2, Y_1 & Y_0. The **block diagram** of 1x4 De-Multiplexer is shown in the following figure.
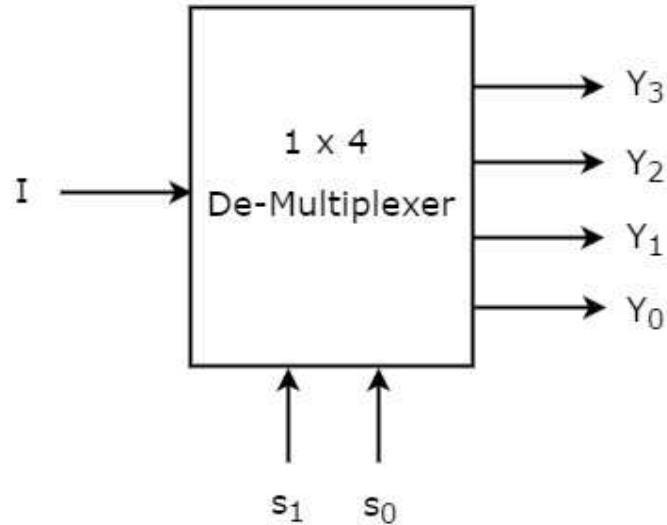
Fig.18: 4×1 De-multiplexer

The single input 'I' will be connected to one of the four outputs, Y_3 to Y_0 based on the values of selection lines s_1 & s0. The **Truth table** of 1x4 De-Multiplexer is shown below.

Selection Inputs		Output			
S1	S0	Y3	Y2	Y1	Y0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Circuit Diagram:
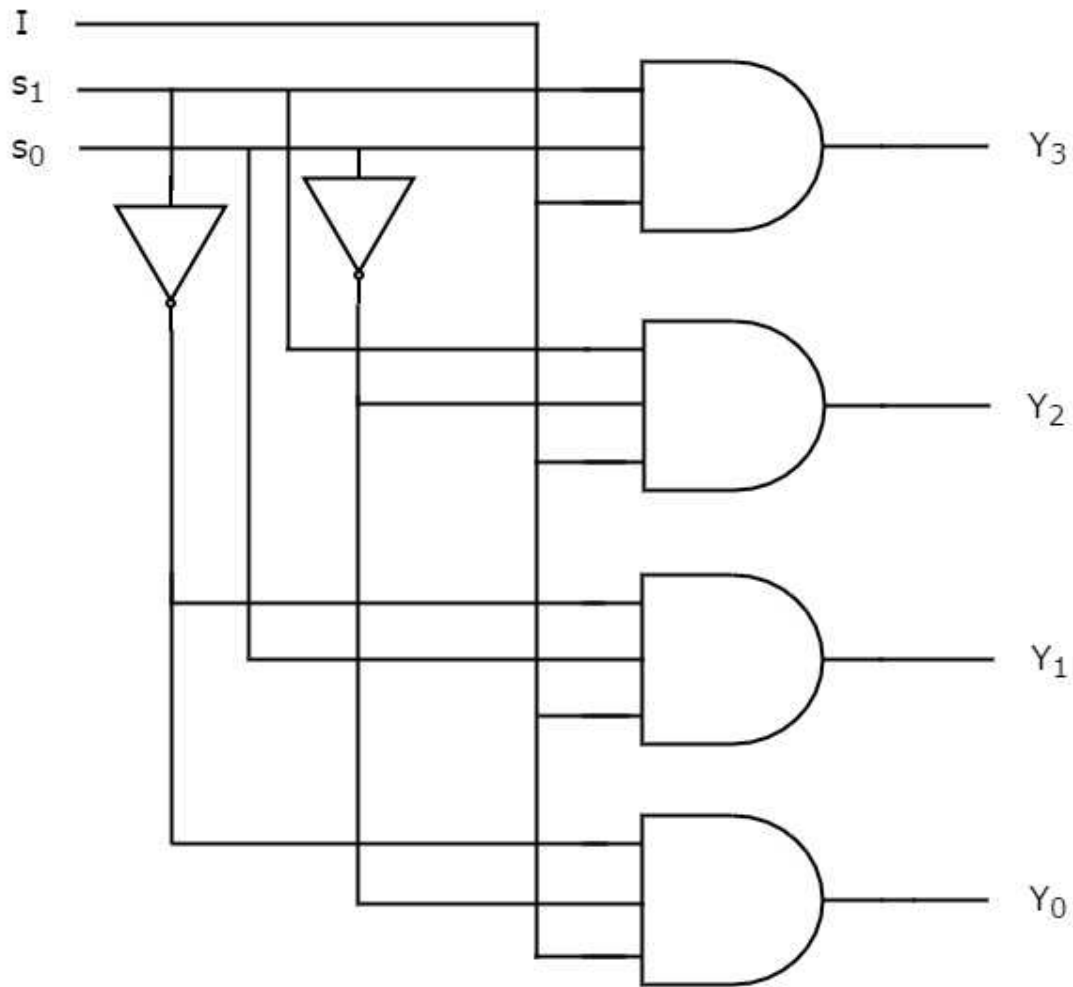
Fig.19: 4×1 De-multiplexer

3.11. Encoder: An **Encoder** is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2^n input lines and 'n' output lines. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2^n input lines with 'n' bits. It is optional to represent the enable signal in encoders.

3.11.1. 4 to 2 Encoder: Let 4 to 2 Encoder has four inputs Y_3, Y_2, Y_1 & Y_0 and two outputs A_1 & A_0. The block diagram of 4 to 2 Encoder is shown in the following figure.
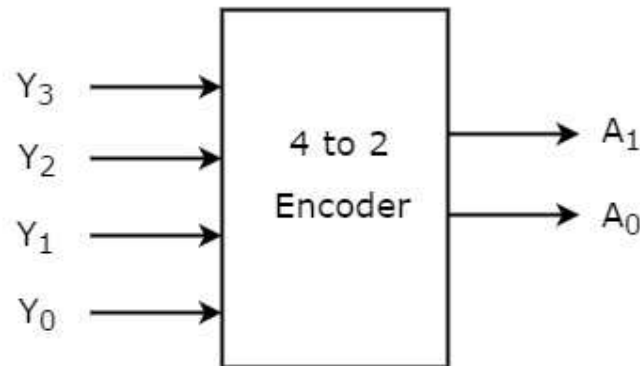
Fig.20: 4×1 Encoder

At any time, only one of these 4 inputs can be '1' in order to get the respective binary code at the output. The **Truth table** of 4 to 2 encoder is shown below.

Inputs				Outputs	
Y3	Y2	Y1	Y0	A1	A0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Circuit Diagram:
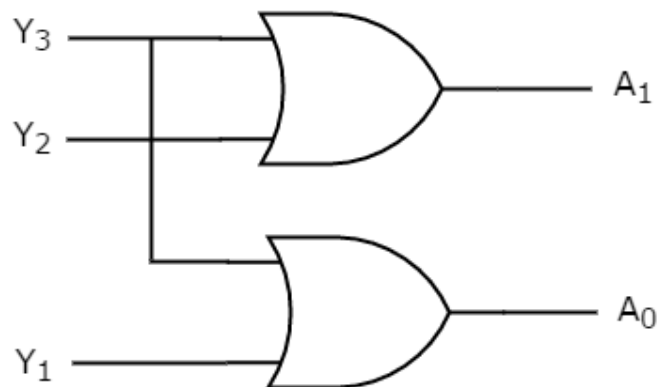
Fig.21: Encoder

3.12. Decoder: Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines. One of these outputs will be active High based on the

combination of inputs present, when the decoder is enabled. That means decoder detects a particular code.

3.12.1. 2 to 4 Decoder: Let 2 to 4 Decoder has two inputs A_1 & A_0 and four outputs Y_3, Y_2, Y_1 & Y_0. The block diagram of 2 to 4 decoder is shown in the following figure.
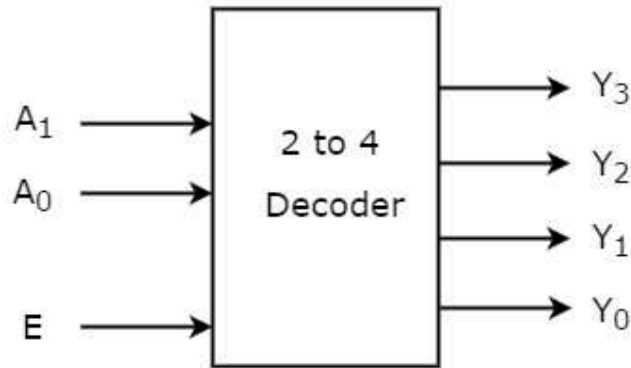
Fig.22: Decoder

One of these four outputs will be '1' for each combination of inputs when enable, E is '1'. The **Truth table** of 2 to 4 decoder is shown below.

Enable	Inputs		Outputs			
E	A1	A0	Y3	Y2	Y1	Y0
0	x	x	0	0	0	0
1	0	00	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	

Circuit Diagram:
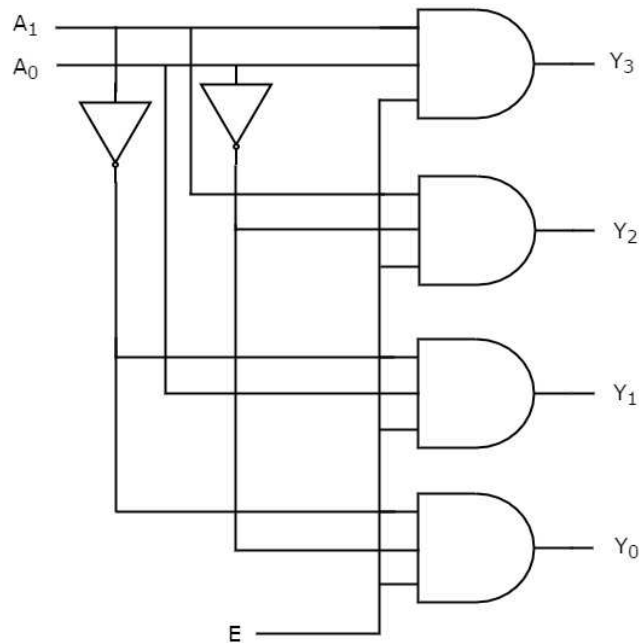
Fig.23: Decoder

Therefore, the outputs of 2 to 4 decoder are nothing but the min terms of two input variables A1 & A0, when enable, E is equal to one. If enable, E is zero, then all the outputs of decoder will be equal to zero.

Similarly, 3 to 8 decoder produces eight min terms of three input variables A2, A1 & A0 and 4 to 16 decoder produces sixteen min terms of four input variables A3, A2, A1 & A0.

3.13 SUMMARY

In this unit, you have studied about Flip flops, various types of flip flop, timing consideration of flip flop , multiplexer, de-multiplexer, encoder, decoder. Initially, various types of flip flop

which are used in digital computers are discussed. Here we have discussed various types of flip flop by different combination. Then timing consideration of flip flop is discussed. We learnt how one signal is converted into many and many into one by studying Multiplexer and de multiplexer.

3.14 GLOSSARY

S-R: -SET- RESET.

T: -Toggele.

3.15 REFERENCES

1. Digital Logic and Computer Design by M. Morris Mano, Pearson.

2. Nonlinear Electronics 2: Flip-Flops, ADC, DAC and PLL

3.16 SUGGESTED READINGS

1. Digital Fundamentals,10th Ed, Floyd T L, Prentice Hall, 2009.

3.17 TERMINAL QUESTIONS

3.17.1 Short Answer type

1. What do you understand by flip flops?

2. Discuss various types of flip flops.

3. Define terms Encoder.

4. Define terms Decoder.

5. Describe Multiplexer.

6. Describe De- multiplexer

UNIT 4   Register and Counter

4.1 INTRODUCTION

Registers are a type of computer memory used to quickly accept, store, and transfer data and instructions that are being used immediately by the CPU. The computer needs processor registers for manipulating data and a register for holding a memory address. The primary function of a computer system is to execute a program, sequence of instructions. These instructions are stored in computer memory.

Flip flops can be used to store a single bit of binary data (1or 0). However, in order to store multiple bits of data, we need multiple flip flops. N flip flops are to be connected in an order to store n bits of data. A **shift register** is a type of digital circuit using a cascade of flip-flops where the output of one flip-flop is connected to the input of the next.

The registers which will shift the bits to left are called "Shift left registers". The registers which will shift the bits to right are called "Shift right registers". A special type of sequential circuit used to count the pulse is known as a counter, or a collection of flip flops where the clock signal is applied is known as counters.

In the Asynchronous counter, the present counter's output passes to the input of the next counter. So, the counters are connected like a chain. Ripple counter is a special type of **Asynchronous** counter in which the clock pulse ripples through the circuit.

4.2 OBJECTIVES

After studying this unit, you will learn about-

- Different types of Register
- counters
- shift register
- Asynchronous counter

4.3. REGISTER: Registers are a type of computer memory used to quickly accept, store, and transfer data and instructions that are being used immediately by the CPU. The registers used by the CPU are often termed as Processor registers.

A processor register may hold an instruction, a storage address, or any data (such as bit sequence or individual characters).

The computer needs processor registers for manipulating data and a register for holding a memory address. The register holding the memory location is used to calculate the address of the next instruction after the execution of the current instruction is completed.

4.3.1. TYPES OF REGISTER:

4.3.1.1. MAR STAND FOR MEMORY ADDRESS REGISTER: This register holds the memory addresses of data and instructions. This register is used to access data and instructions from memory during the execution phase of an instruction. Suppose CPU wants to store some data in the memory or to read the data from the memory. It places the address of the-required memory location in the MAR.

4.3.1.2. PROGRAM COUNTER: The program counter (PC), commonly called the instruction pointer (IP) in Intel x86 microprocessors, and sometimes called the instruction address register, or just part of the instruction sequencer in some computers, is a processor register

It is a 16 bit special function register in the 8085 microprocessor. It keeps track of the the next memory address of the instruction that is to be executed once the execution of the current instruction is completed. In other words, it holds the address of the memory location of the next instruction when the current instruction is executed by the microprocessor.

4.3.1.3. ACCUMULATOR REGISTER: This Register is used for storing the Results those are produced by the System. When the CPU will generate Some Results after the Processing then all the Results will be Stored into the AC Register.

4.3.1.4. MEMORY DATA REGISTER: MDR is the register of a computer control unit that contains the data to be stored in the computer storage (e.g. RAM), or the data after a fetch from the computer storage. It acts like a buffer and holds anything that is copied from the memory ready for the processor to use it.

4.3.1.5. INDEX REGISTER: A hardware element which holds a number that can be added to (or, in some cases, subtracted from) the address portion of a computer instruction to form an effective address. Also known as base register. An index register in a computer's CPU is a processor register used for modifying operand addresses during the run of a program.

4.3.1.6. MEMORY BUFFER REGISTER: MBR stand for Memory Buffer Register. This register holds the contents of data or instruction read from, or written in memory. It means that this register is used to store data/instruction coming from the memory or going to the memory.

4.3.2 DATA REGISTER: A register used in microcomputers to temporarily store data being transmitted to or from a peripheral device.

The Memory unit has a capacity of 4096 words, and each word contains 16 bits.

1. The Data Register (DR) contains 16 bits which hold the operand read from the memory location.

2. The Memory Address Register (MAR) contains 12 bits which hold the address for the memory location.

3. The Program Counter (PC) also contains 12 bits which hold the address of the next instruction to be read from memory after the current instruction is executed.

4. The Accumulator (AC) register is a general purpose processing register.

5. The instruction read from memory is placed in the Instruction register (IR).

6. The Temporary Register (TR) is used for holding the temporary data during the processing.

7. The Input Registers (IR) holds the input characters given by the user.

8. The Output Registers (OR) holds the output after processing the input data.

Register	Symbol	No. of bits	Function
Data Register	DR	16	Hold memory operand
Address Register	AR	12	Hold address for the memory
Accumulator	AC	16	Processor Register
Instruction Register	IR	16	Hold instruction code
Program Counter	PC	12	Hold instruction of address
Temporary Register	TR	16	Hold temporary data
Input Register	IRPR	08	Carries input character
Output Register	OUTR	08	Carries output character

4.3.2.1. BASIC OPERATION:

1. The primary function of a computer system is to execute a program, sequence of instructions. These instructions are stored in computer memory.

2. These instructions are executed to process data which are already loaded in the computer memory through some input devices.

3. After processing the data, the result is either stored in the memory for further reference, or it is sent to the outside world through some output port.

4. To perform the execution of an instruction, in addition to the arithmetic logic unit, and control unit, the processor contains a number of registers used for temporary storage of data and some special function registers.

5. The special function registers include program counters (PC), instruction registers (IR), memory address registers (MAR) and memory and memory data registers (MDR).

6. The Program counter is one of the most critical registers in CPU.

7. The Program counter monitors the execution of instructions. It keeps track on which instruction is being executed and what the next instruction will be.

8. The instruction register IR is used to hold the instruction that is currently being executed.

9. The contents of IR are available to the control unit, which generate the timing signals that control, the various processing elements involved in executing the instruction.

10. The two registers MAR and MDR are used to handle the data transfer between the main memory and the processor.

11. The MAR holds the address of the main memory to or from which data is to be transferred.

12. The MDR contains the data to be written into or read from the addressed word of the main memory.

13. Whenever the processor is asked to communicate with devices, we say that the processor is servicing the devices. The processor can service these devices in one of the two ways.

14. One way is to use the polling routine, and the other way is to use an interrupt.

15. Polling enables the processor software to check each of the input and output devices frequently. During this check, the processor tests to see if any devices need servicing or not.

16. Interrupt method provides an external asynchronous input that informs the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device.

4.4. SHIFT REGISTER:
Flip flops can be used to store a single bit of binary data (1or 0). However, in order to store multiple bits of data, we need multiple flip flops. N flip flops are to be connected in an order to store n bits of data. A **Register** is a device which is used to store such information. It is a group of flip flops connected in series used to store multiple bits of data.

A **shift register** is a type of digital circuit using a cascade of flip-flops where the output of one flip-flop is connected to the input of the next. They share a single clock signal, which causes the data stored in the system to shift from one location to the next. By connecting the last flip-flop back to the first, the data can cycle within the shifters for extended periods, and in this form they were used as a form of computer memory. In this role they are very similar

to the earlier delay line memory systems and were widely used in the late 1960s and early 1970s to replace that form of memory.

The information stored within these registers can be transferred with the help of **shift registers**. Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data.

In most cases, several parallel shift registers would be used to build a larger memory pool known as a bit array. Data was stored into the array and read back out in parallel, often as a computer word, while each bit was stored serially in the shift registers. There is an inherent trade-off in the design of bit arrays; putting more flip-flops in a row allows a single shifter to store more bits, but requires more clock cycles to push the data through all of the shifters before the data can be read back out again.

Shift registers can have both parallel and serial inputs and outputs. These are often configured as "serial-in, parallel-out" (SIPO) or as "parallel-in, serial-out" (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also "bidirectional" shift registers, which allow shifting in both directions: L → R or R → L. The serial input and last output of a shift register can also be connected to create a "circular shift register". A PIPO register (parallel in, parallel out) is very fast – an output is given within a single clock pulse.

The registers which will shift the bits to left are called "Shift left registers". The registers which will shift the bits to right are called "Shift right registers".

Shift registers are basically of 4 types. These are:

1. Serial IN Serial Out shift register
2. Serial In parallel Out shift register
3. Parallel In Serial Out shift register
4. Parallel In parallel Out shift register

4.4.1. SERIAL IN SERIAL OUT SHIFT REGISTER: The shift register, which allows serial input (one bit after the other through a single data line) and produces a serial output is known as Serial-In Serial-Out shift register. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, thus the name Serial-In Serial-Out Shift Register.

The logic circuit given below shows a serial-in serial-out shift register. The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.
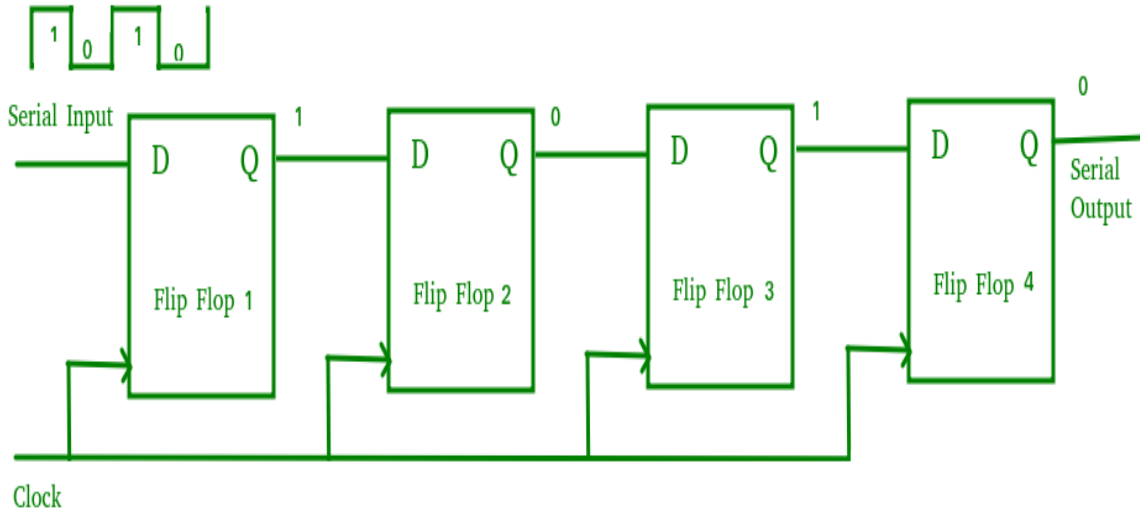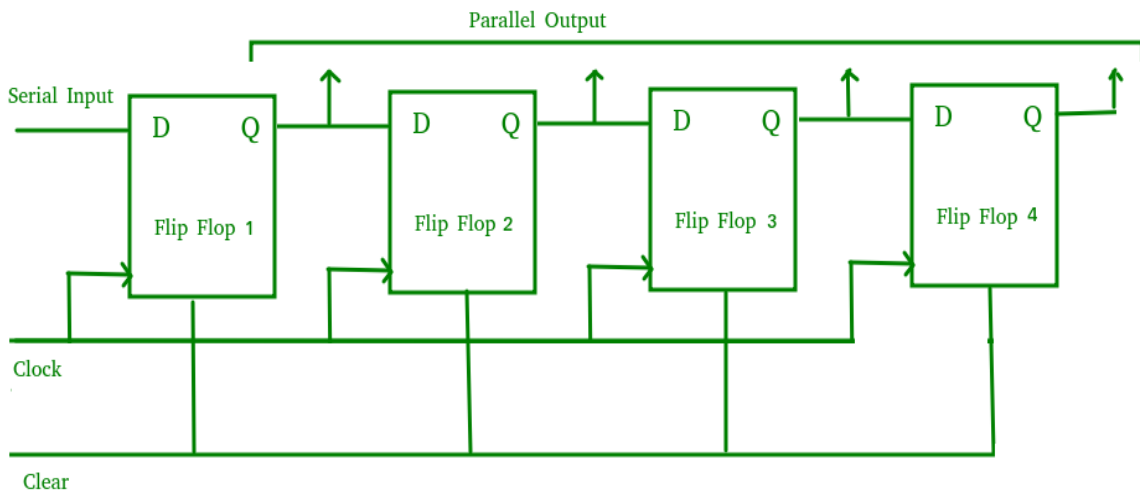
Fig. 1: Serial IN Serial Out shift register

The above circuit is an example of shift right register, taking the serial data input from the left side of the flip flop. The main use of a SISO is to act as a delay element.

4.4.2. SERIAL IN PARALLEL OUT SHIFT REGISTER: The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as Serial-In Parallel-Out shift register.

The logic circuit given below shows a serial-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal is connected in addition to the clock signal to all the 4 flip flops in order to RESET them. The output of the first flip flop is connected to the input of the next flip flop and so on. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

Fig. 2: Serial In parallel Out shift register

The above circuit is an example of shift right register, taking the serial data input from the left side of the flip flop and producing a parallel output. They are used in communication lines where demultiplexing of a data line into several parallel lines is required because the main use of the SIPO register is to convert serial data into parallel data.

4.5. UNIVERSAL SHIFT REGISTER: A register where the data is shifted in one direction is known as the **"uni-directional"** shift register. A register in which the data is shifted in both the direction is known as **"bi-directional"** shift register. A **"Universal"** shift register is a special type of register that can load the data in a parallel way and shift that data in both directions, i.e., right and left.

The input M, i.e., the mode control input, is set to 1 to perform the parallel loading operation. If this input set to 0, then the serial shifting operation is performed. If we connect the mode control input with the ground, then the circuit will work as a **"bi-directional"** register. The diagram of the universal shift register is given below. When the input is passed to the **serial input**, the register performs the "serial left" operation. When the input is passed to the input **D**, the register performs the serial right operation.

4.5.1. BLOCK DIAGRAM:
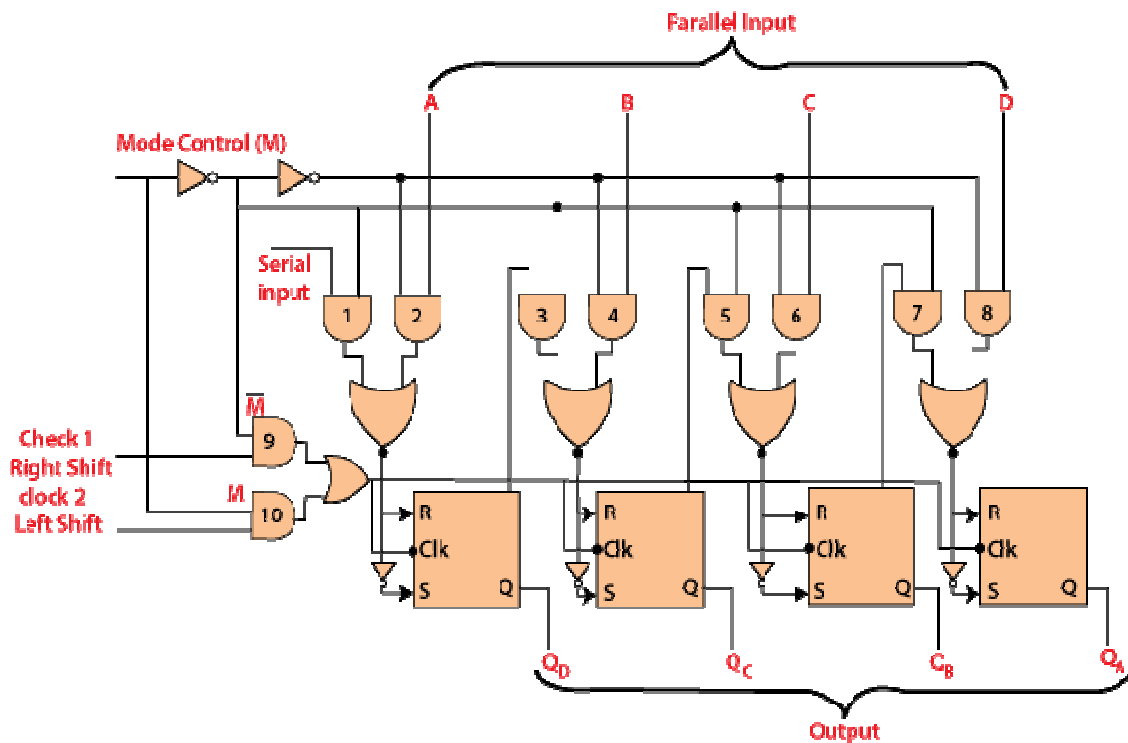
Fig. 3: Universal Shift Register

4.6. COUNTERS: A special type of sequential circuit used to count the pulse is known as a counter, or a collection of flip flops where the clock signal is applied is known as counters.

The counter is one of the widest applications of the flip flop. Based on the clock pulse, the output of the counter contains a predefined state. The number of the pulse can be counted using the output of the counter.

TRUTH TABLE:

Clock	Conter Output		State Number	Decimal counter output
	QB	QA		
Initially	0	0	-	0
1st	0	1	1	1
2nd	1	0	2	2
3rd	1	1	3	3
4th	0	0	4	0

There are the following types of counters:

- Asynchronous Counters
- Synchronous Counters

4.6.1. ASYNCHRONOUS OR RIPPLE COUNTERS: The **Asynchronous counter** is also known as the **ripple counter**. Below is a diagram of the 2-bit **Asynchronous counter** in which we used two T flip-flops. Apart from the T flip flop, we can also use the JK flip flop by setting both of the inputs to 1 permanently. The external clock pass to the clock input of the first flip flop, i.e., FF-A and its output, i.e., is passed to clock input of the next flip flop, i.e., FF-B.

Block Diagram:
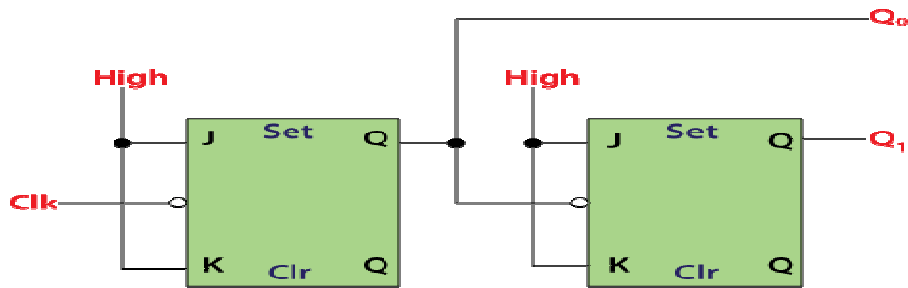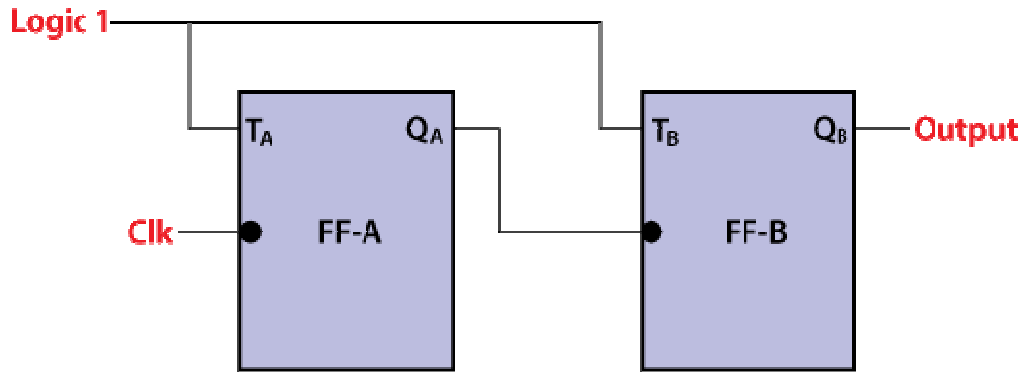
Signal Diagram:
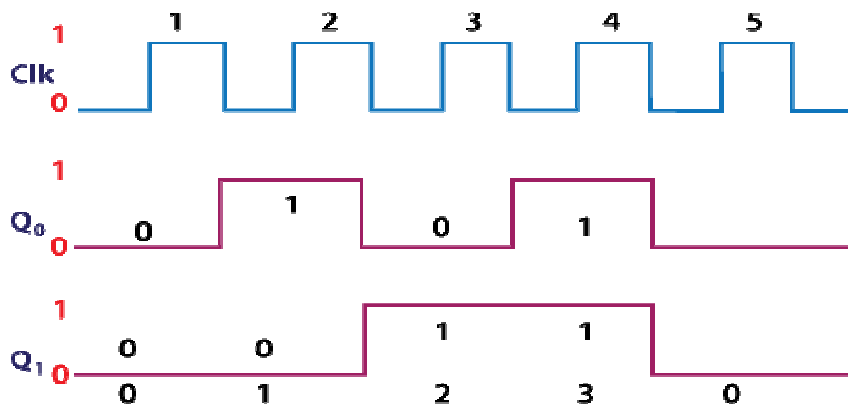
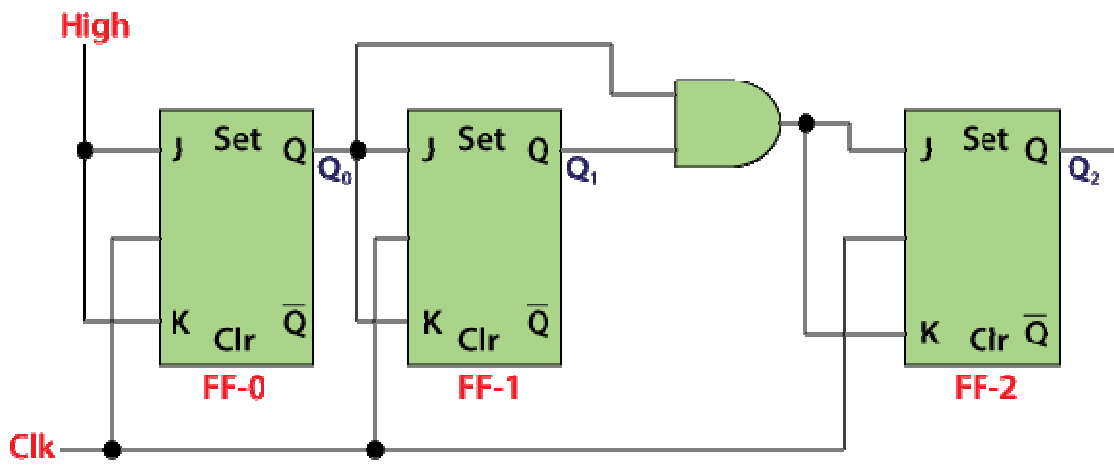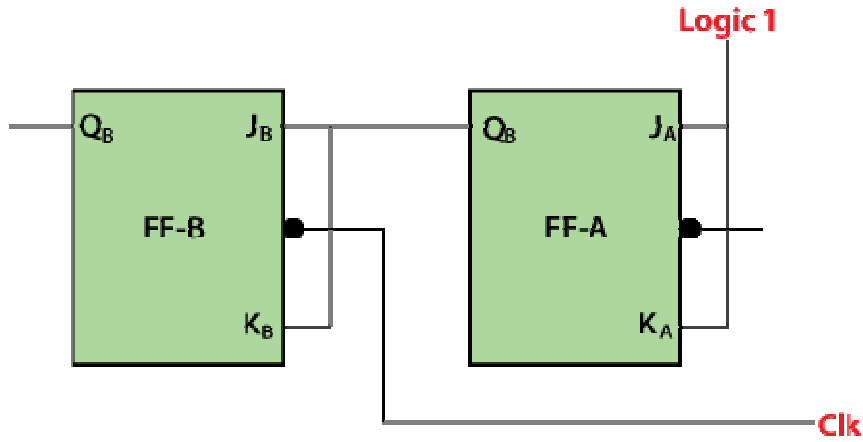**Fig. 4: Asynchronous or ripple counters**

Operation:

1. **Condition 1:** When both the flip flops are in reset condition.
   Operation: The outputs of both flip flops, i.e., Q_A Q_B, will be 0.

2. **Condition 2:** When the first negative clock edge passes.
   Operation: The first flip flop will toggle, and the output of this flip flop will change from 0 to 1. The output of this flip flop will be taken by the clock input of the next flip flop. This output will be taken as a positive edge clock by the second flip flop. This input will not change the second flip flop's output state because it is the negative edge triggered flip flop.
   So, $Q_A = 1$ and $Q_B = 0$

3. **Condition 3:** When the second negative clock edge is applied.
   Operation: The first flip flop will toggle again, and the output of this flip flop will change from 1 to 0. This output will be taken as a negative edge clock by the second flip flop. This input will change the second flip flop's output state because it is the negative edge triggered flip flop.
   So, $Q_A = 0$ and $Q_B = 1$.

4. **Condition 4:** When the third negative clock edge is applied.
   Operation: The first flip flop will toggle again, and the output of this flip flop will change from 0 to 1. This output will be taken as a positive edge clock by the second flip flop. This input will not change the second flip flop's output state because it is the negative edge triggered flip flop.
   So, $Q_A = 1$ and $Q_B = 1$

Condition 5: When the fourth negative clock edge is applied.
Operation: The first flip flop will toggle again, and the output of this flip flop will change from 1 to 0. This output will be taken as a negative edge clock by the second flip flop. This input will change the output state of the second flip flop.
So, $Q_A = 0$ and $Q_B = 0$

4.6.2. SYNCHRONOUS COUNTER: In the Asynchronous counter, the present counter's output passes to the input of the next counter. So, the counters are connected like a chain. The drawback of this system is that it creates the counting delay, and the propagation delay also occurs during the counting stage. The synchronous counter is designed to remove this drawback.

In the synchronous counter, the same clock pulse is passed to the clock input of all the flip flops. The clock signals produced by all the flip flops are the same as each other. Below is the diagram of a 2-bit synchronous counter in which the inputs of the first flip flop, i.e., FF-A, are set to 1. So, the first flip flop will work as a toggle flip-flop. The output of the first flip flop is passed to both the inputs of the next JK flip flop.
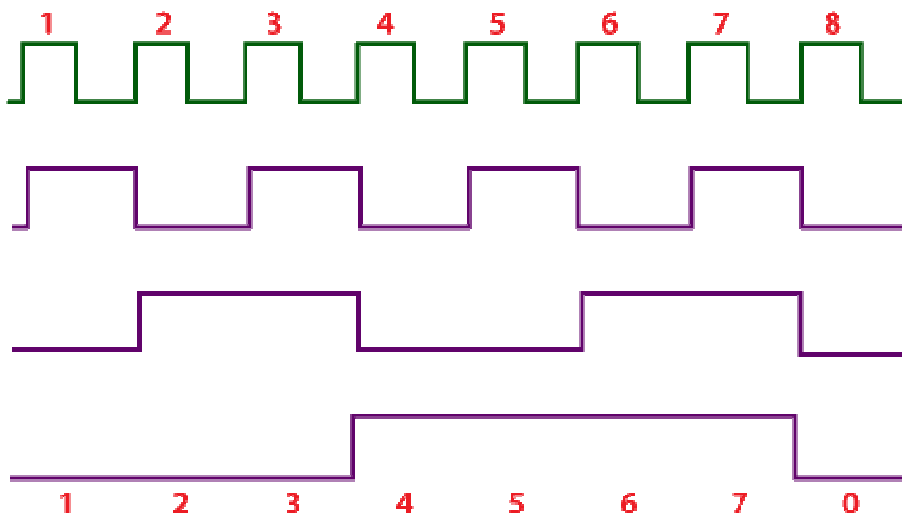
Logical Diagram:

Signal Diagram:

Fig. 5: Synchronous counter

Operation:

1. **Condition 1:** When both the flip flops are in reset condition.
   Operation: The outputs of both flip flops, i.e., $Q_A Q_B$, will be 0. So, $Q_A = 0$ and $Q_B = 0$

2. **Condition 2:** When the first negative clock edge passes.
   Operation: The first flip flop will be toggled, and the output of this flip flop will be changed from 0 to 1. When the first negative clock edge is passed, the output of the first flip flop will be 0. The clock input of the first flip flop and both of its inputs will set to 0. In this way, the state of the second flip flop will remain the same. So, $Q_A = 1$ and $Q_B = 0$.

3. **Condition 2:** When the second negative clock edge is passed.
   Operation: The first flip flop will be toggled again, and the output of this flip flop will be changed from 1 to 0. When the second negative clock edge is passed, the output of the first flip flop will be 1. The clock input of the first flip flop and both of its inputs will set to 1. In this way, the state of the second flip flop will change from 0 to 1. So, $Q_A = 0$ and $Q_B = 1$.

4. **Condition 2:** When the third negative clock edge passes.
   Operation: The first flip flop will toggle from 0 to 1, but at this instance, both the inputs and the clock input set to 0. Hence, the outputs will remain the same as before So, $Q_A = 1$ and $Q_B = 1$.

5. **Condition 2:** When the fourth negative clock edge passes.
   Operation: The first flip flop will toggle from 1 to 0. At this instance, the inputs and the clock input of the second flip flop set to 1. Hence, the outputs will change from 1 to 0. So, $Q_A = 0$ and $Q_B = 0$.

4.7. RIPPLE COUNTER: Ripple counter is a special type of **Asynchronous** counter in which the clock pulse ripples through the circuit. The n-MOD ripple counter forms by combining n number of flip-flops. The n-MOD ripple counter can count 2n states, and then the counter resets to its initial value.

Features of the Ripple Counter:

o Different types of flip flops with different clock pulse are used.

o It is an example of an asynchronous counter.

o The flip flops are used in toggle mode.

o The external clock pulse is applied to only one flip flop. The output of this flip flop is treated as a clock pulse for the next flip flop.

o In counting sequence, the flip flop in which external clock pulse is passed, act as LSB.

Based on their circuitry design, the counters are classified into the following types:

Up Counter

The up-counter counts the states in ascending order.

Down Counter

The down counter counts the states in descending order.

Up-Down Counter

The up and down counter is a special type of bi-directional counter which counts the states either in the forward direction or reverse direction. It also refers to a reversible counter.

4.7.1. BINARY RIPPLE COUNTER: A **Binary counter** is a **2-Mod counter** which counts up to 2-bit state values, i.e., 22 = 4 values. The flip flops having similar conditions for toggling like T and JK are used to construct the **Ripple counter**. Below is a circuit diagram of **a binary ripple counter**.In the circuit design of the binary ripple counter, two JK flip flops are used. The high voltage signal is passed to the inputs of both flip flops. This high voltage input maintains the flip flops at a state 1.
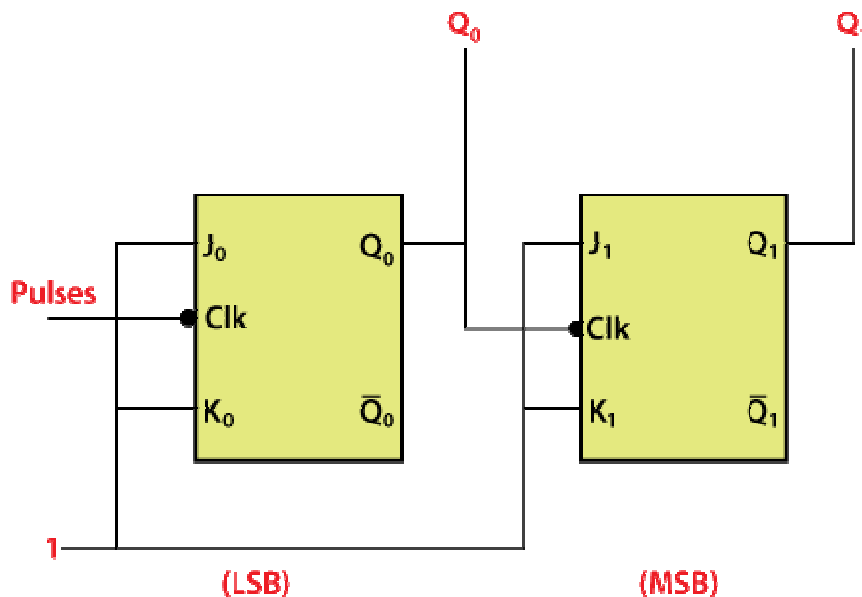
Fig. 6: Binary Ripple Counter

The outputs Q_0 and Q_1 are the LSB and MSB bits, respectively. The truth table of JK flip flop helps us to understand the functioning of the counter.

Jn	Kn	Qn+1
0	0	Qn
1	0	1
1	1	0
1	1	Qn

When the high voltage to the inputs of the flip flops, the fourth condition is of the JK flip flop occurs. The flip flops will be at the state 1 when we apply high voltage to the input of the flip-flop. So, the states of the flip flops passes are toggled at the negative going end of the clock pulse. In simple words, the flip flop toggle when the clock pulse transition takes place from 1 to 0.
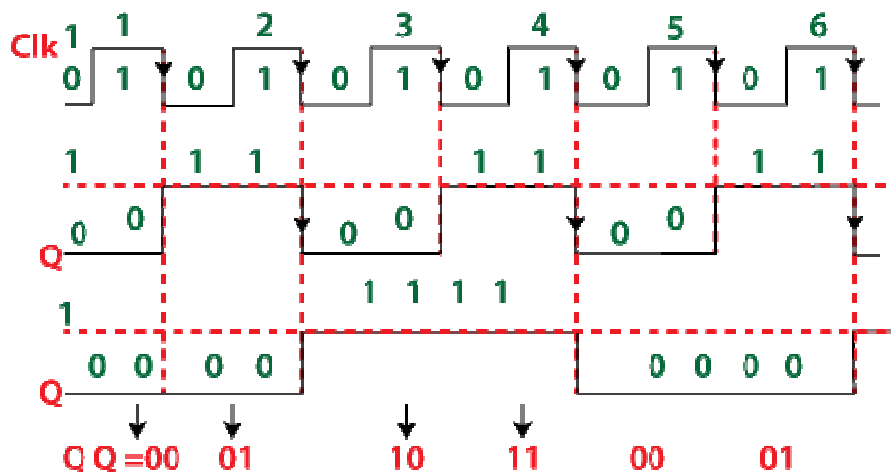

Fig. 7: Binary Ripple Counter

The state of the output Q_0 change when the negative clock edge passes to the flip flop. Initially, all the flip flops are set to 0. These flip flop changes their states when the passed clock goes from 1 to 0. The JK flip flop toggles when the inputs of the flip flops are one, and then the flip flop changes its state from 0 to 1. For all the clock pulse, the process remains the same.

Number of inputs pulses	Q1	Q0
0	-	-
1	0	0
2	0	1
3	1	0
4	1	1

The output of the first flip flop passes to the second flip flop as a clock pulse. From the above timing diagram, it is clear that the state of the second flip flop is changed when the output

Q_0 goes transition from 1 to 0. The outputs Q_0 and Q_1 treat as LSB and MSB. The counter counts the values 00, 01, 10, 11. After counting these values, the counter resets itself and starts counting again from 00, 01, 10, and 1. The count values until the clock pulses are passed to J_0K_0 flip flop.

4.8 SUMMARY

In this unit, you have studied about Registers and their types You learnt the primary function of a computer system is to execute a program, sequence of instructions. These instructions are stored in computer memory.

You have also studied Flip flops can be used to store a single bit of binary data (1or 0). However, in order to store multiple bits of data, we need multiple flip flops. N flip flops are to be connected in an order to store n bits of data. A shift register is a type of digital circuit using a cascade of flip-flops where the output of one flip-flop is connected to the input of the next.

In this unit you learnt about Asynchronous counter and Ripple counter is a special type of Asynchronous counter in which the clock pulse ripples through the circuit.

4.9 REFERENCES

1. Digital Logic and Computer Design by M. Morris Mano, Pearson.

2. Modern Digital Electronics by R. P. Jain, TMH, 2010.

4.10 SUGGESTED READINGS

1. Digital Fundamentals,10th Ed, Floyd T L, Prentice Hall, 2009.

2. You tube

3. NPTL website

4. Online tutorials

4.11 TERMINAL QUESTIONS

4.11.1 Short Answer type

1. What do you understand Register?

2. What do you understand by counters?

3. What do you understand by shift register?

4. Discuss about Asynchronous counter.

UNIT 5: Analog to digital (A / D) and digital to Analog (D/A) conversion

Structure

5.1 INTRODUCTION

Analogue to Digital Converter, or ADC, is a data converter which allows digital circuits to interface with the real world by encoding an analogue signal into a binary code.

Parallel of "Flash" A/D converters use a series of interconnected but equally spaced comparators and voltage references generated by a series network of precision resistors for generating an equivalent output code for a particular n-bit resolution.

Signals are mainly classified into two types i.e. Analog & Digital signal. The data or information that we perceive in real world exists in analog form while the digital devices such as cellphone, calculator & computer can only understand a data signal in digital domain.

In order to understand the data that we process in a digital domain, we need to convert it into analog domain. An example of that would be the process of audio & video editing.

5.2 OBJECTIVES

After studying this unit, you will learn about-

- Conversion analog to digital
- Conversion digital to analog

5.3. ANALOGUE TO DIGITAL CONVERTER: Analogue to Digital Converter, or ADC, is a data converter which allows digital circuits to interface with the real world by encoding an analogue signal into a binary code.

The **Analogue-to-Digital Converter**, (ADCs) allow micro-processor controlled circuits, Arduinos, Raspberry Pi, and other such digital logic circuits to communicate with the real world. In the real world, analogue signals have continuously changing values which come from various sources and sensors which can measure sound, light, temperature or movement, and many digital systems interact with their environment by measuring the analogue signals from such transducers.
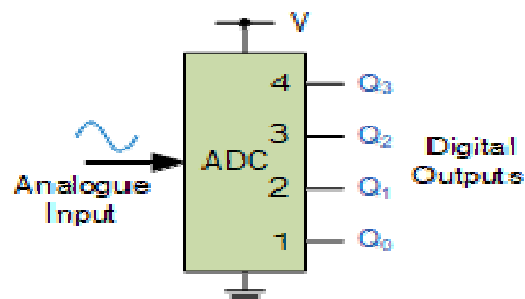

Fig.: 5.1 Analogue-to-Digital Converter

While analogue signals can be continuous and provide an infinite number different voltage values, digital circuits on the other hand work with binary signal which have only two

discrete states, a logic "1" (HIGH) or a logic "0" (LOW). So it is necessary to have an electronic circuit which can convert between the two different domains of continuously changing analogue signals and discrete digital signals, and this is where *Analogue-to-Digital Converters* (A/D) come in.

Basically an analogue to digital converter takes a snapshot of an analogue voltage at one instant in time and produces a digital output code which represents this analogue voltage. The number of binary digits, or bits used to represent this analogue voltage value depends on the resolution of an A/D converter.

For example a 4-bit ADC will have a resolution of one part in 15, $(2^4 - 1)$ whereas an 8-bit ADC will have a resolution of one part in 255, $(2^8 - 1)$. Thus an analogue to digital converter takes an unknown continuous analogue signal and converts it into an "n"- bit binary number of 2^n bits.

But first let us remind ourselves of the differences between an analogue (or analog) signal and a digital signal as shown:

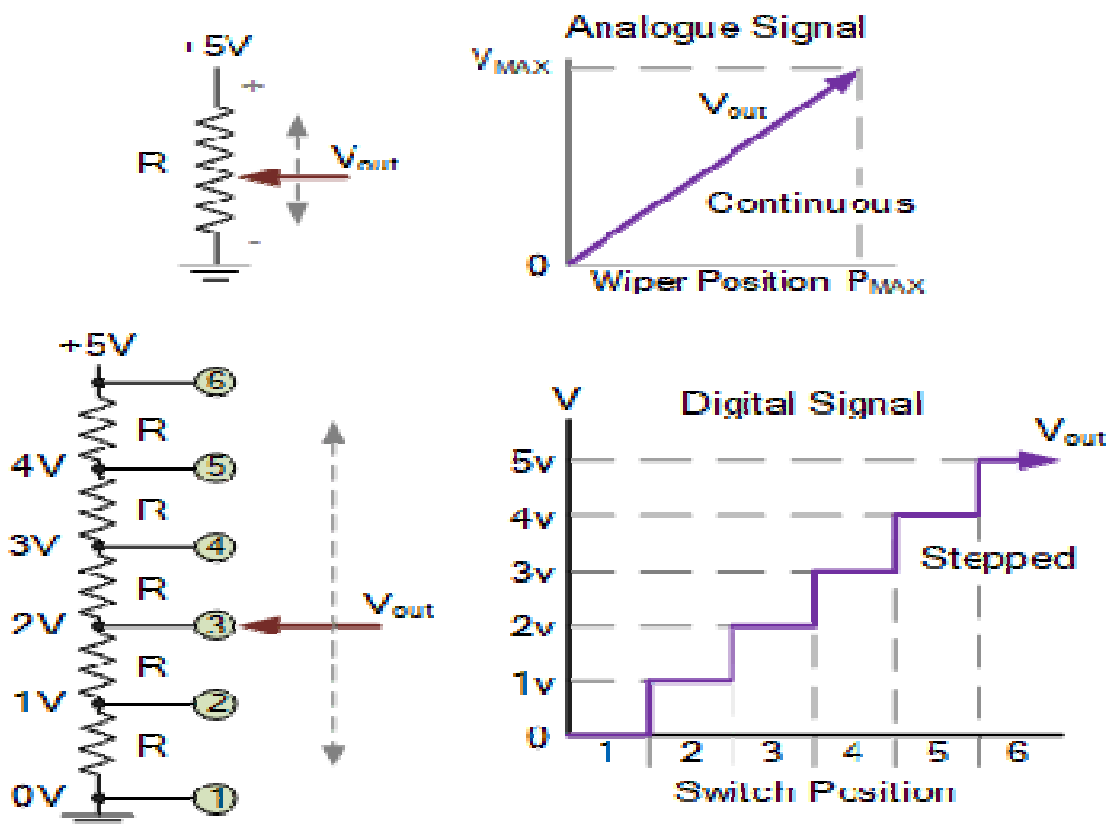## 5.3.1. ANALOGUE AND DIGITAL SIGNALS:

Fig. 5.2 Analogue and Digital Signals

Here we can see that as the wiper terminal of the potentiometer is rotated between between 0 volts and V_{MAX}, it produces a continuous output signal (or voltage) which has an infinite number of output values relative to the wiper position. As the potentiometers wiper is adjusted from one position to the next, there is no sudden or step change between the two voltage levels thereby producing a continuously variable output voltage. Examples of analogue signals include temperature, pressure, liquid levels and light intensity.

For a digital circuit the potentiometer wiper has been replaced by a single rotary switch which is connected in turn to each junction of the series resistor chain, forming a basic potential divider network. As the switch is rotated from one position (or node) to the next the output voltage, V_{OUT} changes quickly in discrete and distinctive voltage steps representing multiples of 1.0 volts on each switching action or step as shown.

So for example, the output voltage will be 2 volts, 3 volts, 5 volts, etc. but NOT 2.5V, 3.1V or 4.6V. Finer output voltage levels could easily be produced by using a multi-positional switch and increasing the number of resistive elements within the potential divider network, therefore increasing the number of discrete switching steps.

Then we can see that the major differences between an analogue signal and a digital signal is that an "Analogue" quantity is continuously changing over time while a "Digital" quantity has discrete (step by step) values. "LOW" to "HIGH" or "HIGH" to "LOW".

The process of taking an analogue voltage signal and converting it into an equivalent digital signal can be done in many different ways, and while there are many analogue-to-digital converter chips.

One simple and easy way is by using parallel encoding, also known as *flash*, *simultaneous*, or *multiple comparator* converters in which comparators are used to detect different voltage levels and output their switching state to an encoder.

Parallel of "Flash" A/D converters use a series of interconnected but equally spaced comparators and voltage references generated by a series network of precision resistors for generating an equivalent output code for a particular n-bit resolution.

The advantage of parallel or flash converters is that they are simple to construct and do not require any timing clocks as the instant an analogue voltage is applied to the comparator inputs, it is compared against a reference voltage. Consider the comparator circuit below.

5.3.2. COMPARATOR CIRCUIT: An analogue comparator such as the LM339N which has two analogue inputs, one positive and one negative, and which can be used to compare the magnitudes of two different voltage levels.
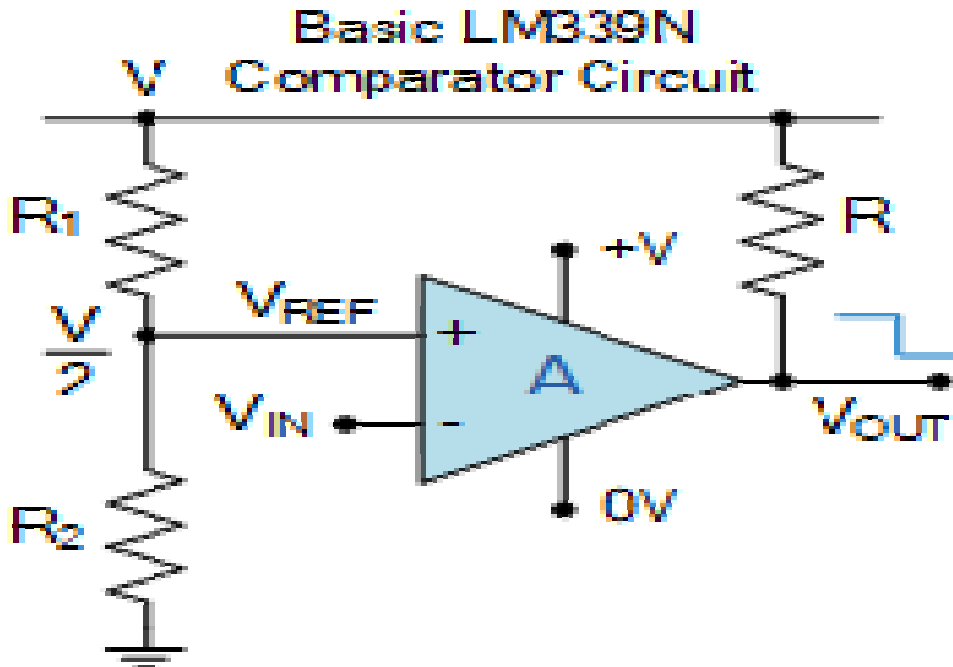

Fig.5.3. Comparator Circuit

A voltage input, (V_{IN}) signal is applied to one input of the comparator, while a reference voltage, (V_{REF}) to the other. A comparison of the two voltage levels at the comparator's input is made to determine the comparators digital logic output state, either a "1" or a "0".

The reference voltage, V_{REF} is compared against the input voltage, V_{IN} applied to the other input. For an LM339 comparator, if the input voltage is less than the reference voltage, ($V_{IN} < V_{REF}$) the output is "OFF", and if it is greater than the reference voltage, ($V_{IN} > V_{REF}$) the output will be "ON". Thus a comparator compares two voltage levels and determines which one of the two is higher.

In our simple example above, V_{REF} is obtained from the voltage divider network setup by R_1 and R_2. If the two resisors are of equal values, that is $R_1 = R_2$, then clearly the reference voltage level will be equal to half the supply voltage, or V/2. So for a comparator with an open-collector output, if V_{IN} is less than V/2, the output is HIGH, and if V_{IN} is greater than V/2, the output is LOW acting as a 1-bit ADC.

But by adding more resistors to the voltage divider network we can effectively "divide" the supply voltage by an amount determined by the resistances of the resistors. However, the more resistors we use in the voltage divider network the more comparators will be required.

In general, $2^n - 1$ comparators would be required for conversion of an "n"-bit binary output, where "n" is typically in the range from 8 to 16. In our example above, the single bit ADC used $2^1 - 1$, which equals "1" comparator to determine if V_{IN} was greater or smaller than the V/2 reference voltage.

If we now create a 2-bit ADC, then we will need $2^2 - 1$ which is "3" comparators as we need four different voltage levels corresponding to the 4 digital values required for a 4-to-2 bit encoder circuit as shown.

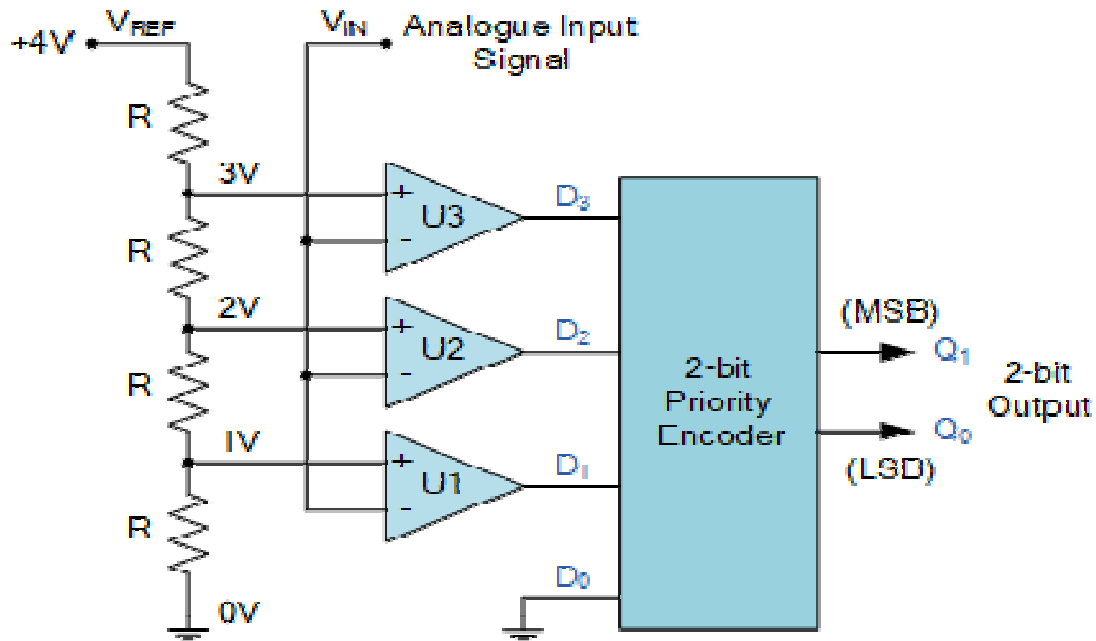### 5.3.3. 2-BIT ANALOGUE TO DIGITAL CONVERTER CIRCUIT:

Fig. 5.4. Analogue to Digital Converter Circuit

This will give us a 2-bit output code for all four possible values of analogue input of:

5.3.3.1. 2-BIT A/D CONVERTER OUTPUT:

Analog input voltage	Comparator Outputs				Digital Outputs	
	D3	D2	D1	D0	Q1	Q0
0 to 1 V	0	0	0	0	0	0
1 to 2 V	0	0	1	X	0	1
2 to 3 V	0	1	X	X	1	0
3 to 4 V	1	X	X	X	1	1

Where: "X" is a "don't care", that is either a logic "0" or a logic "1" condition.

So how does this *analogue-to-digital converter* work. For an A/D converters to be useful it has to produce a meaningful digital representation of the analogue input signal. Here in this simple 2-bit ADC example we have assumed for simplicity that the input voltage V_{IN} is between 0 and 4 volts, so have set V_{REF} and the resistive voltage-divider network to drop 1 volt across each resistor.

When V_{IN} is between 0 and 1 volt, (<1V) the input on all three comparators will be less than the reference voltage, so their outputs will be LOW and the encoder will output a binary zero (00) condition on pins Q_0 and Q_1. When V_{IN} increases and exceeds 1 volt but is less than 2 volts, ($1V<V_{IN}<2V$) comparator U1 which has a reference voltage input set at 1 volt, will detect this voltage difference and produce a HIGH output. The priority encoder which is used as the 4-to-2 bit encoding detects the change of input at D_1 and produces a binary output of "1" (01).

Note that a **Priority Encoder** such as the TTL 74LS148 allocates a priority level to each individual input. The priority encoders output corresponds to the currently active input which has the highest priority. So when an input with a higher priority (D_1 compared to D_0) is present, all other inputs with a lower priority will be ignored. So if there are two or more inputs at logic level "1" at the same time, the actual output code on D_0 and D_1 would only correspond to the input with the highest designated priority.

So now as V_{IN} increases above 2 volts, the next reference voltage level, comparator U2 detects the change and produces a HIGH output. But because input D_2 has a higher priority than inputs D_0 or D_1, the priority encoder outputs a binary "2" (10) code, and so on when V_{IN} exceeds 3 volts producing a binary code output of "3" (11). Clearly as V_{IN} reduces or changes between each reference voltage level, each comparator will output either a HIGH or a LOW condition to the encoder which inturn produces a 2-bit binary code between 00 and 11 relative to V_{IN}.

This is all well and good, but priority encoders are not available as 4-to-2 bit devices, and if we use a commercially available one such as the TTL 74LS148 or its CMOS 4532 equivalent which are both 8-bit devices, then six of the binary bits would not be used. But a simple encoder circuit can be made using digital Ex-OR gates and a matrix of signal diodes as shown.

5.4. DIGITAL TO ANALOG CONVERTER (DAC): Signals are
mainly classified into two types i.e. Analog & Digital signal. The data or information that we perceive in real world exists in analog form while the digital devices such as cellphone, calculator & computer can only understand a data signal in digital domain. Analog to Digital(ADC) & **Digital to analog converter (DAC)** are the two types of converters that we use in our daily life to convert the signals into each other.
Digital to analog converter is an electronic circuit that converts any digital signal (such as binary signal) into an analog signal (voltage or current).

The digital signal such as the binary signal exist in the form of bits & it is the combination of 1's & 0's (or High & low voltage levels). The DAC converts these bits into an analog voltage or current.
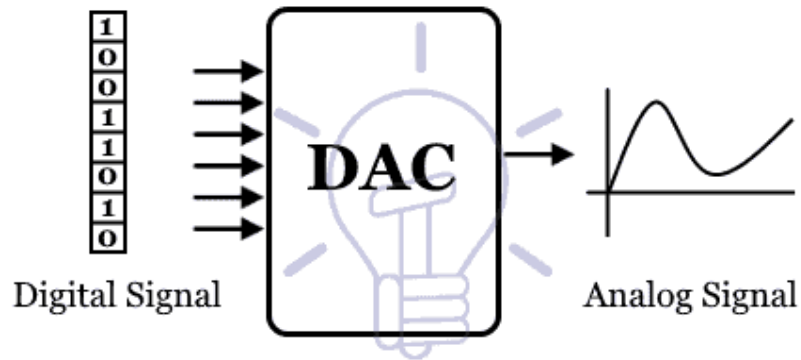
Fig. 5.5 Digital to analog convertor

The DAC has several digital inputs & a single analog output.

5.4.1. NEED OF DAC: The information exist in real world is in analog form. Why we convert them into digital form in the first place if we want to convert them back? The processing speed of a digital computer is very fast & can compute or process any data in a matter of micro seconds. It conserves time & helps in processing complex data according to our need. But we cannot understand the digital data in real world.

In order to understand the data that we process in a digital domain, we need to convert it into analog domain. An example of that would be the process of audio & video editing. We capture the data using our digital camera & microphone to convert the analog data into digital. We process it using our computers to edit it according to over needs. In order to view our edited work, we use DACs to convert it back into the analog domain to view & listen it through our screen & speakers.

5.4.2. WORKING OF DAC: The digital binary data exists in the form of bits. Each bit is either 1 or 0 & they represent its weight corresponding to its position. The weight is 2^n where the n is the position of the bit from right hand side & it start from 0.

A7	A6	A5	A4	A3	A2	A1	A0

8- bit Binary Number

Bit Weight = 2^n
Bit weight of 5th bit from left= $2^n = 2^4 = 16$
The bit weight is multiplied by the bit value. Since the bit could be either 0 or 1, it means;
Bit value of 1 x bit weight = $1 \times 2^n = 2^n$
Bit value of 0 x bit weight = $0 \times 2^{(n-1)} = 0$

Now adding the weights of all the bits with its value in a binary number 10011;

$1\ 0001_2 = (1 \times 2^4) + (0 \times 2^3) + (0 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$

$10001_2 = 16 + 0 + 0 + 0 + 1$

$10001_2 = 17$

This is how the digital to analog converter DAC works by adding the weights of all corresponding bits with its value to generate the analog value at its output

5.4.3. TYPES OF DAC

The DAC can be designed using one of the following types of circuits.

5.4.3.1. WEIGHTED RESISTOR METHOD: The weighted resistor method utilizes the summing operational amplifier circuit. The summing amplifier adds the input signals with different gains corresponding to their resistors.
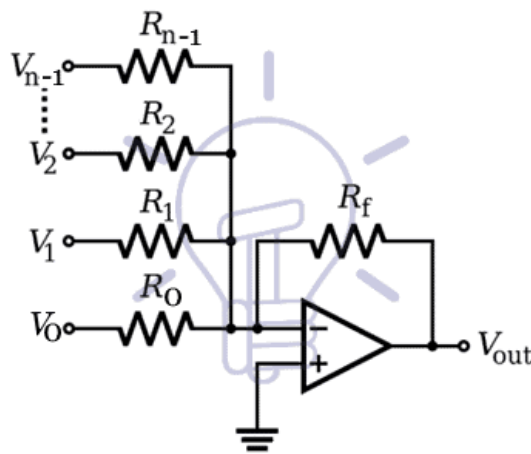

Fig. 5.6.: Weighted Resistor Method Circuit

$$V_{out} = - \{(R_f / R_0)\ V_0 + (R_f / R_1)\ V_1 + (R_f / R_2)\ V_2 + \ldots + (R_f / R_{n-1})\ V_{n-1}\}$$

It can be used as a DAC if we assign each resistor a with specific value to scale their gain in the form of 2, 4, 8 ,16 & so on. As we know the V_{ref} (the reference voltage or the maximum analog output voltage) is the only input signal (beside the binary input) so;
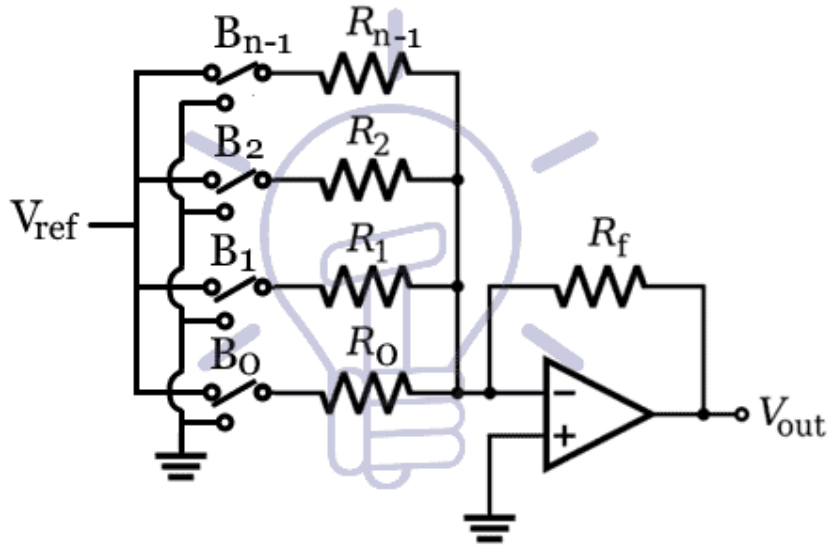
Fig. 5.7: Weighted Resistor Method Circuit

$$V_{out} = - \{(R_f /R_0) V_{ref} + (R_f /R_1) V_{ref} + (R_f /R_2) V_{ref} + \ldots + (R_f/R_{n-1}) V_{ref}\}$$

$$V_{out} = - V_{ref} \{(R_f /R_0) + (R_f /R_1) + (R_f /R_2) + \ldots + (R_f/R_{n-1}) \}$$

In this circuit, the binary input 1 or 0 is used for switching between the v_{ref} & GND. The input $B = 1$ means the switch is connected with V_{ref} & $B = 0$ means the switch is connected with GND. In such case the equation for a binary number B_0, B_1, B_2… B_n ; where B_0 is LSB & B_n is MSB, become

$$V_{out} = - V_{ref} \{ B_0 (R_f /R_0) + B_1 (R_f /R_1) + B_2 (R_f /R_2) + \ldots + B_{n-1} (R_f/R_{n-1}) \}$$

The resistor $R_f = R$. while the R_0, R_1, R_2, & R_{n-1} are scaled to provide the necessary gain corresponding to the weight of each bit. The resistors are scaled with the values $2^{(N-1)-n}$, such that;

$$R_n = 2^{(N-1)-n} R \text{ where N is number of bits & n is the bit position}$$

So

$$V_{out} = - V_{ref} \{ B_0 (R/2^{(N-1)} R) + B_1 (R /2^{(N-2)} R) + B_2 (R /2^{(N-3)} R) + \ldots + B_{N-2} (R /2^1 R) + B_{N-1} (R /2^0 R) \}$$

$$V_{out} = - V_{ref} \{ B_0 (1/2^{(N-1)}) + B_1 (1 /2^{(N-2)}) + B_2 (1/2^{(N-3)}) + \ldots + B_{N-2} (1 /2^{(1)}) + B_{N-1} (1 /2^0) \}$$

The output voltage for a 4 bit binary number would be;

$$V_{out} = - V_{ref} \{ B_0 (1/2^3) + B_1 (1 /2^{(2)}) + B_2 (1/2^{(1)}) + B_3 (1/2^0) \}$$

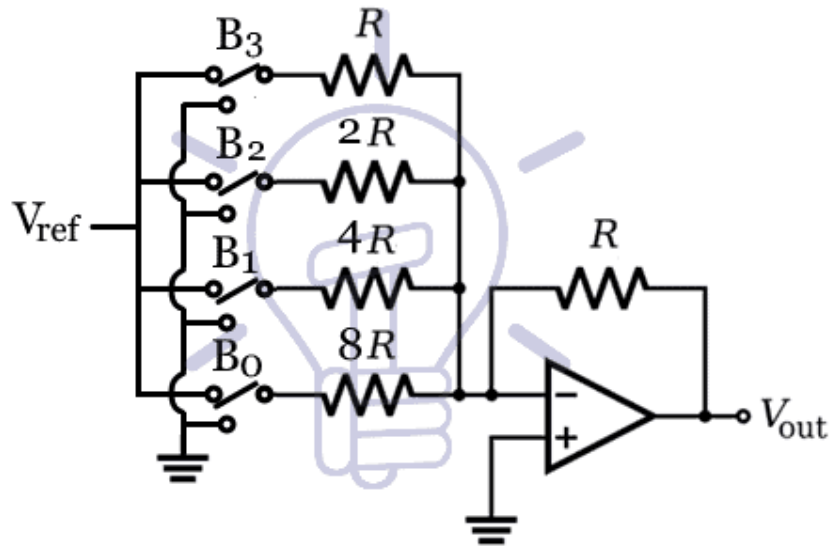$$V_{out} = - V_{ref} \{ B_0 (1/8) + B_1 (1 /4) + B_2 (1/2) + B_3 \}$$

Fig. 5.8: **Weighted Resistor Method Circuit**

As you can see, each resistor is scaled to add the bit-weight of each bit of a binary input. Simplified formulae for such circuit would be

$V_{out} = - V_{ref} \{ B_0 (1/2^{(N-1)})) + B_1 (1/2^{(N-2)}) + B_2 (1/2^{(N-3)})) + B_3 (1/2^{(N-4)}) + B_4 (1/2^{(N-5)} + ...\}$

Where the denominator $2^{(N-1)}$ represents the scaling factor of each corresponding resistor.

Drawbacks of Weighted Resistor Method;

- Increasing the number of input bits require large value resistors (increases exponentially)
- The values of large resistors are not accurate & always have some % of give or take.
- The error in resistor value causes to lose the accuracy of the DAC for large binary numbers.
- Due to the difficulty of designing resistors, it is not practical to implement it.

5.4.3.2. R-2R LADDER CIRCUIT: The drawback raised in weighted resistor method can be resolved in it. This method is more precise, accurate & easy to design then the weighted resistor method. R- 2R ladder circuit is made by adding combination R & 2R resistor in cascaded form as shown in the following figure.
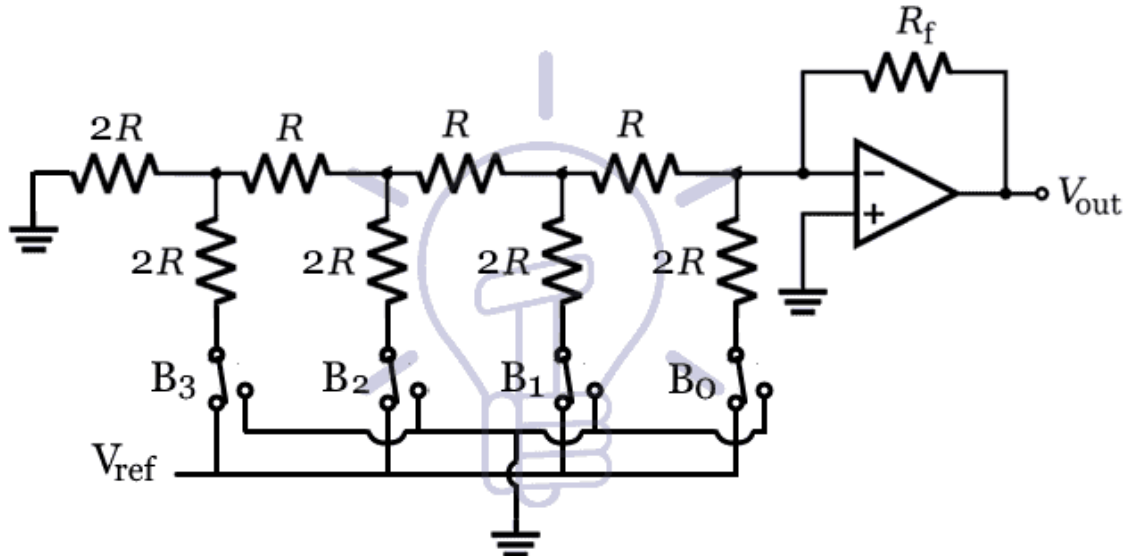

Fig. 5.9: R- 2R Ladder Circuit

There are only two types of resistor used. Each stage contains R & 2R, is used for a single bit. There is switch between the V_{ref} & GND which is controlled by the binary input. Bit 0 means the GND is connected & bit 1 means the V_{ref} is connected.

Working;
Let's assume a 3 bit DAC using R-2R ladder network.
$B_2B_1B_0$ are the 3 bits of the binary input. When $B_0 = 1$, B_1 & $B_2 = 0$. Then the equivalent circuit would be;
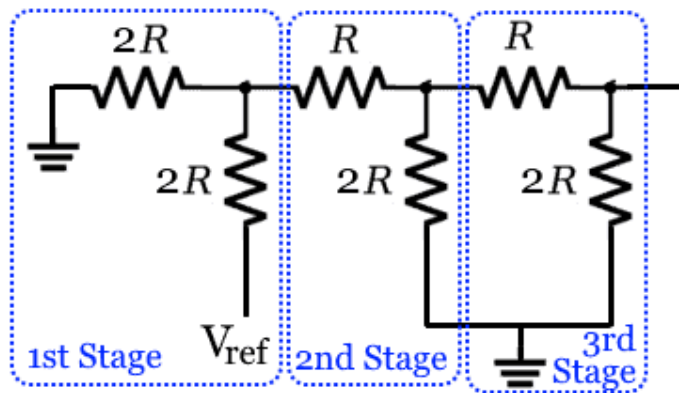

Fig. 5.10: R- 2R Ladder Circuit

Replacing the 1ˢᵗ stage with its V_{th} & R_{th};

$$V_{th} = V_{ref}/2 \ \& \ R_{th} = R$$
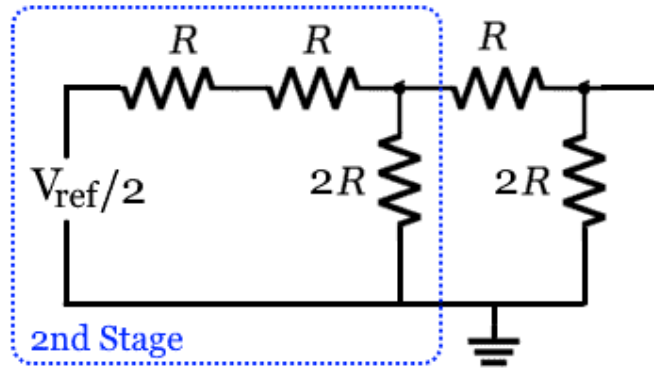

Fig. 5.11: R- 2R Ladder Circuit

Now the 2ⁿᵈ stage V_{th} & R_{th};

$$V_{th} = V_{ref}/4 \ \& \ R_{th} = R$$
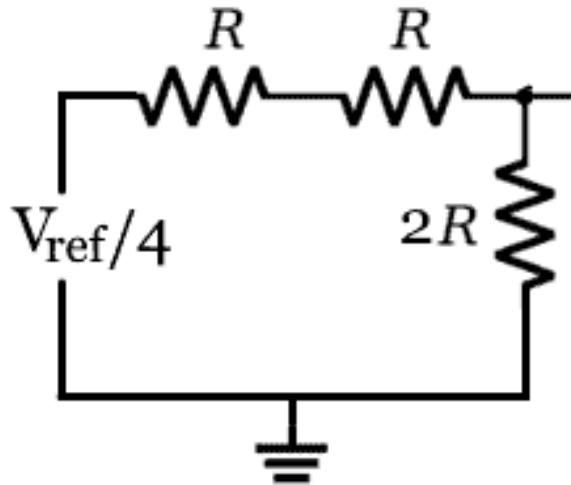
Fig. 5.12: R- 2R Ladder Circuit

Now the 3ʳᵈ stage Vth & R_{th}

$$V_{th} = V_{ref}/8 \ \& \ R_{th} = R$$

Fig. 5.13: R- 2R Ladder Circuit

So the output voltage in this case would become

$$V_{out} = -V_{th} (R_f/R) = -(V_{ref}/8) (R/R) = -(V_{ref}/8)$$

When $B_1 = 1$, B_0 & $B_2 = 0$. Then the equivalent circuit would be;

Fig. 5.14: R- 2R Ladder Circuit

Applying the same process the output voltage will be

$$V_{out} = -(V_{ref}/4)$$
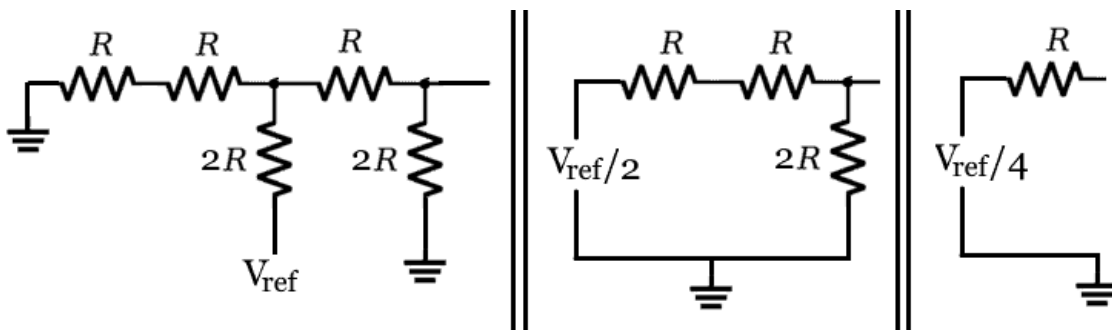
Fig. 5.15: R- 2R Ladder Circuit

When $B_2 = 1$, B_0 & $B_1 = 0$. Then the equivalent circuit would be
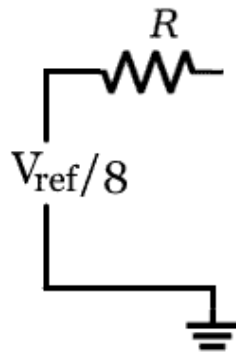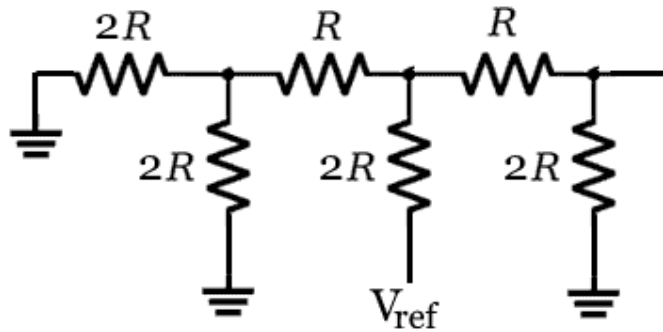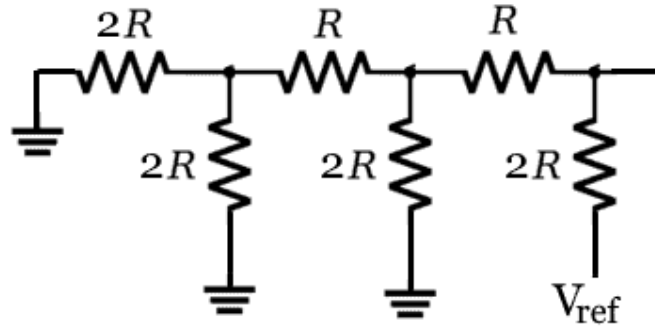

Fig. 5.16: R- 2R Ladder Circuit

Applying the same process the output voltage will be
$$V_{out} = -(V_{ref}/2)$$
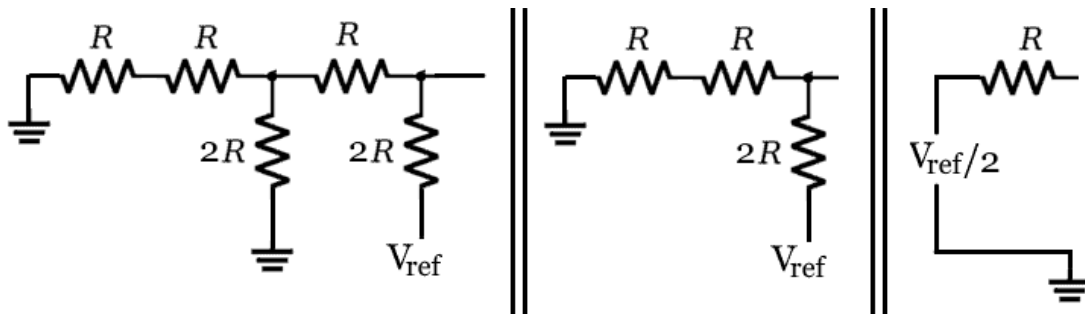
Fig. 5.17: R- 2R Ladder Circuit

As we know the output of the opamp is the sum of individual inputs where each bit is

$$V_{out} = -\{ B_0 (V_{ref}/8) + B_1 (V_{ref}/4) + B_2 (V_{ref}/2)\}$$
$$V_{out} = - V_{ref} \{ B_0(1/8) + B_1 (1/4) + B_2 (1/2)\}$$
$$V_{out} = - V_{ref} \{ B_0(1/2^3) + B_1 (1/2^2) + B_2 (1/2^1)\}$$

We can generalize this formula for an N bit binary number as;
$$V_{out} = - V_{ref} \{B_0(1/2^N) + B_1(1/2^{N-1}) + B_2(1/2^{N-2}) +...+ B_{N-2}(1/2^2) + B_{N-1}(1/2^1)\}$$

Advantages of R-2R Ladder DAC;
* Uses only two types of resistors
* Easiliy scalable to any number of bits
* Output impedance is always R

5.4.3.3. PWM BASED CONVERSION: It is another method used in digital to analog converter & microcontrollers such as Arduino can be easily programed to utilize its PWM function to generate an analog output.

Pulse Width Modulation or PWM is a method of varying the average power of a signal by varying its duty cycle. He duty is the % turn on time of the signal, the % amount of time for which the signal remains high. Like 40% duty cycle signal means it stays high for 40% of time & stays low for 60%.

We can use a binary number to generate such type signal whose duty cycle depends on the binary digit. The PWM wave is the filtered using a low pass filter to remove the fluctuations & provide a smooth analog voltage.

The low pass filter used can be a first order, 2nd order low pass filter would be a great choice for a PWM base digital to analog converter.

5.5. Resolution of DAC: Resolution is the number of possible output levels a DAC can produce. It depends on the number of input bits.

$$Resolution = 2^n$$

The resolution of an n-bit DAC is 2^n. For example, a 4-bit DAC has resolution of 2^4 or 16 output levels.

Step Size of a DAC

The step size of a DAC is the smallest change in the analog output & it is the difference between two consecutive output voltage levels.

The step size can be calculated by dividing the range (maximum output voltage) or V_{ref} by 2^n where n is the number of bits.

$$Step\ size = Range\ /\ 2^n$$

For example, the step size of a 4 bit DAC with range of 5v is;

$$Step\ size = 5/2^4 = 5/16 = 0.3125v$$

The step size of this DAC is 0.3125. So for a single bit increment, its analog output will increase by 0.3125 v.

Increasing the resolution of a DAC decreases the step size & generates a smooth analog wave with much more accuracy.

5.5.1. APPLICATIONS OF DAC: Digital to analog converters are used in various applications to convert a digitally processed signal into an analog signal. Some of the various applications of a DAC are given below;

Audio: The audio signal is analog in nature but it is converted using ADC (analog to digital converter) into digital format to edit & store in storage devices in various digital formats such as mp3, wav etc. The audio amplifier or the sound card in a system contains DAC that converts the audio signal stored in digital device into an analog signal. The signal can be modified by the amplifier by varying its gain (volume), bass, treble etc. & then converted into analog signal because the speaker cannot support a digital signal.

Video: Digital video players utilize DAC to play any digital video using an analog monitor. These video players convert the digital signal from the digital source file into an analog signal.

A digital video player has digital video ports such as DVI or HDMI. But if it has any analog output ports (composite port of yellow color), it contains a DAC whose job is to convert the video file into analog signal.

Motor Control: One of the most important components in controlling a motor using a digital device such as a microcontroller is a DAC.

In various electronics projects, motor is embedded with a microcontroller. The microcontroller generates a digital signal to vary the speed of the motor which is converted into an analog signal using a DAC (Digital to Analog Converter).

5.6 SUMMARY

In this unit, you have studied about conversion of Analog to Digital and Digital to analog conversion and their applications.

5.7 REFERENCES

1. Digital Logic and Computer Design by M. Morris Mano, Pearson.
2. Modern Digital Electronics by R. P. Jain, TMH, 2010.

5.8 SUGGESTED READINGS

1. Digital Fundamentals,10th Ed, Floyd T L, Prentice Hall, 2009.
2. You tube
3. Online tutorials
4. NPTL website

5.9 TERMINAL QUESTIONS

5.9.1 Short Answer type

1. What are analog signals why do we convert analog to digital signals?
2. What are digital signals why do we convert digital to analog signals.
3. Explain comparator circuit.
4. Discuss weighted resistor method.
5. Discuss R- 2R ladder circuit.

UNIT 6   Modulation AM and FM

(Transmission and Reception)

Structure

6.1 INTRODUCTION TO COMMUNICATION SYSTEM

What do you mean by communication, and what are its different components? The process of transmitting and receiving useful information from one point in space and time to another point is called communication. The basic block diagram of the communication system is given in figure 1.
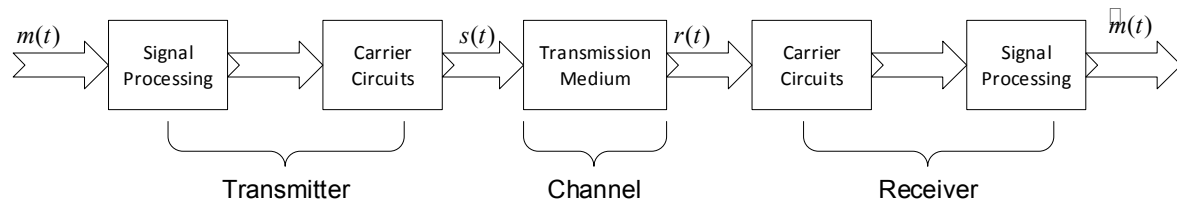

Fig.1: A typical communication system

The different components of a typical communication system are as follows-

(1) Information Sources- An information source is the message signal that we need to transmit, e.g., audio, music, speech, video, image, data. These signals are also called baseband signals i.e., signals having a majority of its power near to DC.

(2) Transmitter- Transducer in the transmitter converts the message signal into electrical signals. Signal processing is used for conditioning the message signal e.g., the low pass filtering operation is done to bandlimit the message signal to a specific band. The carrier circuits then convert the low-frequency message signal into an appropriate high-frequency band employing analog or digital modulation, which can be transmitted over for the channel.

(3) Channel- The channel is the transmission medium over which the signals propagate. Transmission media can be of two types: (1) Wired media- Twisted pair, coaxial, optical wires etc. (2) Wireless media- space, indoor/air, outdoor/air etc. The signal while propagating gets degraded over distance, and signal boosters are required to improve the signal and reduce noise e.g., repeaters. The signal degradation can occur because of any of the following effects: (a) attenuation- reduction in the signal strength (b) spreading of signal- widening of the pulse duration (c) fading (wireless)- multiplicative noise (d) phase jitter- different phases are experienced by the same signal in the channel (e) multiple propagation paths (wireless)- the transmitted signal may arrive at the receiver from multiple paths and (f) additive noise- noise can come into the picture either from the transmitter, channel, and receiver.

(4) Receiver- The receiver undoes everything which is done on the signal at the receiver side. The carrier circuits do the demodulation at the receiver, i.e., it converts the bandpass signal back to a baseband signal. The signal processing then extracts and enhances the baseband signal. This extracted signal is then again converted from electrical signals into appropriate forms using transducers and send to output devices such as TV displays, speakers, computer screens etc.

6.2 OBJECTIVES

After studying this unit, you should be able to-

- Analyze and compare different analog modulation schemes for their efficiency and bandwidth.
- Establish a foundation for understanding the relationship among various technical factors useful in designing & operating a communication system.
- Analyze the behavior of a communication system in the presence of noise.
- Solve problems on Amplitude Modulation and Frequency Modulation.

6.3 AMPLITUDE MODULATIONS AND DEMODULATIONS

How can you transmit information to large distances? To answer this question, you should first ask the question: what is modulation, and why is it required? Modulation is the process by which some characteristic of a high-frequency carrier signal is varied in accordance with the low-frequency message signal (baseband or modulating signal). As you all know, a signal (typically sinusoids) has two main characteristic parameters: **Amplitude and Angle**. If the amplitude of the high-frequency carrier wave is varied according to the variation in the low-frequency message signal, then it is called as Amplitude Modulation (AM). If the angle of the high-frequency carrier wave is varied according to the low-frequency message signal, then it is called as angle modulation. Angle modulation can be of two types: Frequency Modulation (FM) and Phase Modulation (PM) depending upon whether the frequency or phase of the carrier wave is varied according to the message signal.

Modulation provides a number of advantages such as:

(1) Low-frequency signals cannot propagate over long distances. They can only be transmitted over short distances

(2) Practical length of antennas- In wireless media, antennas are used to transmit and receive the signals. From antenna theory, it is well known that the antennas can operate effectively only when the dimension of the antenna is of the order of the magnitude of the wavelength of the signal used. At low frequencies, the wavelength is large, and therefore the dimension of the antenna required is enormous and impractical. Modulation translates the signal to a higher frequency range, thereby reducing the wavelength of the signal, and the dimension of the antenna required is small and practical.

(3) Frequency Division Multiplexing- Multiple bandlimited signals falling in the same frequency band can be transmitted simultaneously through a transmission channel if each signal is translated to a different frequency band through modulation.

(4) Narrow banding- For a bandlimited wideband signal, designing an antenna would be problematic as the antenna dimension for use at one end of the frequency range may fall short or too large for use at another end of the frequency range. The reason behind this is that the ratio of the highest to lowest frequency is very large. This ratio can be reduced to unity by

translating the signal to a higher frequency range. Such a signal having the highest to lowest frequency ratio close to unity is called a **narrowband signal**. Narrowband signal works effectively well with the same antenna dimension for both the ends of the frequency range.

(5) Common Processing- Processing of different signals occupying different frequency bands may always require to tune the equipment to different frequency ranges. This can be avoided if every time the frequency of the signal is translated down to the operating frequency range of the equipment.

6.3.1 AMPLITUDE MODULATION (AM or DSB-FC)

Amplitude Modulation is the process of varying the amplitude of a relatively high-frequency carrier signal in accordance with the amplitude of the modulating message signal. The carrier amplitude is varied linearly by the modulating signal, which consists of a range of radio frequencies. By doing so, the frequency and phase of the carrier waves remain the same, but the frequency of the message signal gets translated to a higher frequency range. Figure 2 below shows an AM signal and its envelope when the modulating signal is a sinusoidal wave. It can be observed that the envelope of the modulated signal is the same as of the modulating message signal; the frequency of the envelope is the same as of the message signal, and the frequency of the modulated AM signal is the same as the frequency of the carrier wave. It seems as if the low
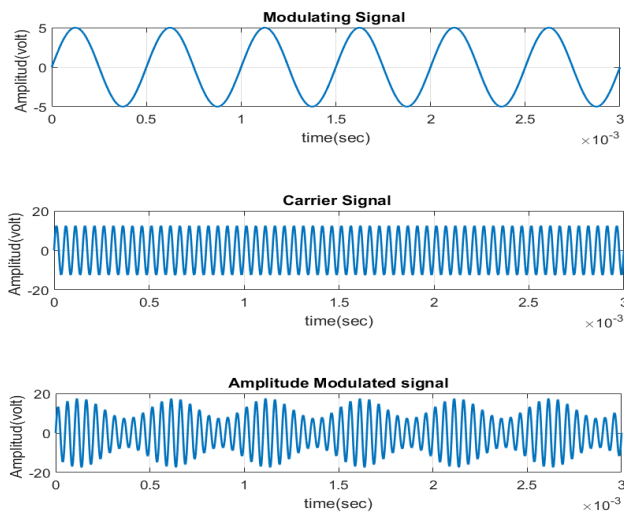

Fig.2: AM signal example

frequency message signal rides over the high-frequency carrier wave. Amplitude Modulation can be of the following types:

1.   Double Sideband with Full Carrier (DSB-FC or AM)

2.   Double Sideband Suppressed Carrier (DSB-SC)

3.   Quadrature Amplitude Modulation (QAM)

4.   Single Sideband Suppressed Carrier (SSB-SC)

5.   Vestigial Sideband (VSB)

Demodulation of DSB-SC modulated waves using **synchronous detection** requires a sophisticated and costly receiver. The reason for this is the absence of the carrier wave information in the modulated wave. This calls for the generation of a carrier at the receiver in frequency and phase synchronization with the carrier at the transmitter. A simple remedy to this issue is to transmit the carrier wave ($A_c \cos(\omega_c t)$) [along with the DSB-SC modulated wave $m(t)\cos(\omega_c t)$] so that there is no need to generate a carrier at the receiver. This is the so-called **AM (amplitude modulation).** The obvious disadvantage of this is the increase in the power to be transmitted, which in turn makes the AM transmitter expensive. In **point-to-point communications**, we have one transmitter for each receiver. In such cases, having complex receivers can be justified if there is large enough saving in the expensive high-power transmitting equipment. On the other hand, for **broadcast systems**, we have multiple receivers for one transmitter. In this case, it would be more economical to have a single expensive high-power transmitter and simpler, less expensive receivers. Therefore, situations which demand broadcast communication is where AM or DSB-FC modulated waves can be used for transmission. The AM modulated wave s(t) is represented as:

$$s(t) = A_c \cos(\omega_c t) + m(t)\cos(\omega_c t) = A_c[1 + k_a m(t)]\cos(\omega_c t)$$

$$= A_c \cos(\omega_c t) + A_c K_a m(t)\cos(\omega_c t)$$ ……

(1)

Where $K_a = \dfrac{1}{A_c}$ is the amplitude sensitivity, $k_a > 0$ and $\omega_c \gg$ Maximum frequency content in m(t). From equation (1) the following can be readily deduced:

1. Since the DSB-SC signal is $m(t)\cos(\omega_c t)$, it follows that the AM signal is the same as the DSB-SC signal with $A_c[1 + k_a m(t)]$ or $A_c + m(t)$ as the modulating signal instead of m(t).

2. The frequency of the AM signal is, ω_c i.e., the frequency of the carrier wave.

3. The amplitude of the AM signal is $A_c[1 + k_a m(t)]$. This means that the amplitude of an AM signal is (constant) + (linear variation of modulating signal m(t)), which in turn means that the amplitude of the AM signal varies according to the message signal (something that we have already observed from figure 2)

4. Therefore, the plot of the AM signal will be a sinusoid of carrier frequency varying between the amplitudes $A_c[1 + k_a m(t)]$ and $-A_c[1 + k_a m(t)]$.

From equation (1), two cases may arise, as is also illustrated in figure 3 below. In one case (figure 3b), the carrier amplitude A_c is large enough that the quantity $A_c[1 + k_a m(t)] > 0$ or

equivalently $A_c + m(t) > 0 \ \forall t$. This means that the envelope of the modulated signal has the same shape as message signal m(t) but riding over a DC component A_c (as shown in figure 3d).

(a)

$A_c + m(t) > 0 \quad \forall t$

$A_c + m(t) \leq 0 \quad \forall t$

(b)

(c)

$Envelope: \ A_c + m(t)$

$Envelope: \ |A_c + m(t)|$

(d)

(e)
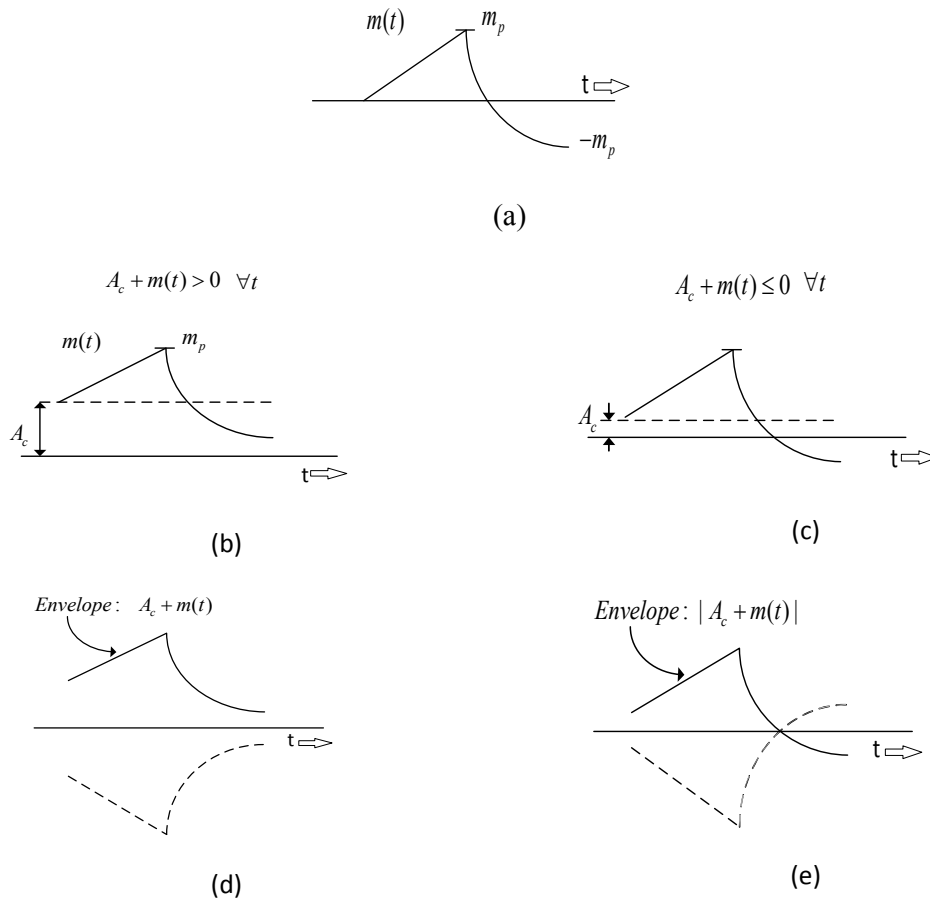
Fig. 3: AM signal and its envelope

In the other case (figure 3c), the carrier amplitude A_c is not large enough, and we have a condition $A_c + m(t) \leq 0$ for all time instances t. In this case, the envelope of the AM wave is not exactly the message signal m(t) but is its rectified form $|A_c + m(t)|$. This means that our message signal can be deducted in the first case by deducting the envelope of the AM signal and removing the DC part from it, whereas such detection is not possible in the second case. This envelope detection is a straightforward and inexpensive technique and does not require the generation of the local carrier at the detector side for demodulation. It is important to note that the envelope of an AM signal $A_c[1 + k_a m(t)]\cos(\omega_c t)$ contains the information about the message signal m(t) if and only if it satisfies the condition $A_c[1 + k_a m(t)] > 0$ or $A_c + m(t) > 0$ for all time instances t. We define a quantity $\mu = \dfrac{A_m}{A_c} = k_a A_m$ known as the

modulation index, where A_m is the maximum amplitude of message signal m(t). Based on the modulation index, an AM signal can be classified as these two cases:

1. $\mu > 1$: This case is called **over-modulation**. This case arises when the maximum amplitude of the baseband/message signal is greater than the amplitude of the carrier signal, i.e. $A_m > A_c$ (see figure 3c, 3e). Overmodulated AM signal serves no benefit, as the main objective for which AM signals are used (i.e., use of simpler and inexpensive demodulators) fails in this case. This does not mean that overmodulated AM signals cannot be demodulated to obtain message signal (they can still be recovered if we do synchronous detection), it merely means that we cannot use simple and inexpensive envelope detectors for its detection. In this case, the baseband signal is not preserved in the AM envelope (as we obtain the rectified form of the amplitude as discussed before), and hence the baseband signal recovered from the envelope will be distorted.

2. $\mu < 1$: This case is called **under-modulation**. Here the maximum amplitude of the baseband/message signal is less than the carrier amplitude, i.e. $A_m < A_c$ (see figure 3b, 3d). In this case, the message signal is preserved in the detected AM envelope, and hence we can use the envelope detector in this case.

The spectrum of an AM wave, $s(t) = A_c \cos(\omega_c t) + m(t)\cos(\omega_c t)$, is the same as that of DSC-SC signal $m(t)\cos(\omega_c t)$ with two additional impulses at $\pm \omega_c$ and is given by

$$s(t) = A_c\cos(\omega_c t) + m(t)\cos(\omega_c t) \xrightleftharpoons{FT} \frac{1}{2}\left[M(\omega + \omega_c) + M(\omega - \omega_c)\right] + \pi A_c\left[\delta(\omega + \omega_c) + \delta(\omega - \omega_c)\right]$$

…… (2)

From equation (2), it can be seen that the spectrum of the message signal m(t), i.e. $M(\omega)$, gets translated to the carrier frequency ω_c with half the magnitude (this will also be the same for DSB-SC signals). Along with this, in the case of AM, as shown by equation (2), we have impulses at locations of the carrier frequency ω_c of strength πA_c. The translated message spectrum is also called as sideband and can be divided into two parts, i.e., a lower sideband (LSB) and an upper sideband (USB) corresponding to whether the sideband (w.r.t to the carrier frequency ω_c) belongs to the lower frequency or, the higher frequency respectively.

6.3.2 AM Generation

Any of the DSC-SC modulators, e.g., Multiplier Modulators, Nonlinear Modulators (Square Law Modulator or Single balanced modulator), Switching Modulators (diode bridge modulator, Ring Modulator or double balanced modulator) etc. can be used to generate the

AM signals, provided that, the modulating signal is $A_c + m(t)$ instead of just $m(t)$. In the case of AM generation, we do not require the modulating circuits to be balanced as there is no need to suppress the carrier in the output (**NOTE: DSC-SC signal can be generated using balanced modulators).** Figure 4 below shows a switching modulator with only one diode instead of a diode bridge, as in the case of a diode bridge used in DSB-SC modulation. The input to the modulator is $m(t) + c\cos(\omega_c t)$ with the amplitude of the carrier much higher than the maximum amplitude of the modulating signal m(t), i.e., $c \gg m(t)$ in order to satisfy the condition required for envelope detection. By doing so, it can be clearly seen that the switching action of the diode is controlled by $c\cos(\omega_c t)$. The diode switches on and off periodically with the carrier frequency ω_c. This on-off action of the diode can be visualized as a square pulse train $w(t)$ of frequency ω_c. Since $w(t)$ is periodic, it can be expanded in its Fourier series as

$$w(t) = \frac{1}{2} + \frac{2}{\pi}\left(\cos(\omega_c t) - \frac{1}{3}\cos(3\omega_c t) + \frac{1}{5}\cos(5\omega_c t) - ... \right) \qquad \ldots\ldots (3)$$

Therefore, in effect, this operation of the AM modulator can be thought of as multiplying the input signal $m(t) + c\cos(\omega_c t)$ by the square pulse train of frequency ω_c. The voltage appearing at the terminal bb' is

$$v_{bb'} = [c\cos(\omega_c t) + m(t)]w(t) = [c\cos(\omega_c t) + m(t)]\left[\frac{1}{2} + \frac{2}{\pi}\left(\cos(\omega_c t) - \frac{1}{3}\cos(3\omega_c t) + \frac{1}{5}\cos(5\omega_c t) - ... \right) \right]$$

$$= \frac{c}{2}\cos(\omega_c t) + \frac{2}{\pi}m(t)\cos(\omega_c t) + \text{ other terms}$$

$$\ldots\ldots (4)$$

Fig.4 AM generator

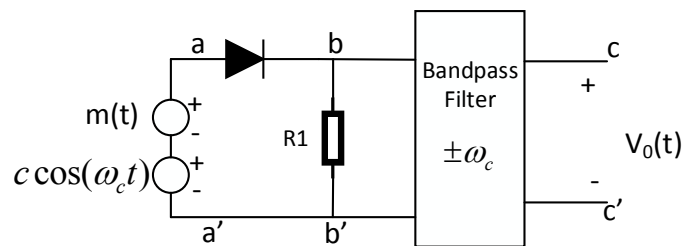The bandpass filter is tuned to ω_c in order to suppress all the other high-frequency components (see equation (4)), yielding the desired AM signal at the output.

6.3.3 POWER CONSIDERATION

An Amplitude Modulated signal is expressed as $s(t) = A_c \cos(\omega_c t) + m(t)\cos(\omega_c t)$. Hence, the total average normalized power of an AM signal is the addition of the powers of the carrier

signal (corresponding to the first term in the above equation) and the sideband power (corresponding to the second term in the above equation), i.e. $P_{total} = P_{carrier} + P_{sideband}$. The sideband power is the useful power, and the carrier power is the power wasted as the carrier component of the AM signal carries no information. Therefore, we can also say that the total power is the addition of useful power and wasted power.

The carrier power $P_{carrier}$ is the mean square value of $A_c \cos(\omega_c t)$, which is

$$P_{carrier} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{T/2} A_c^2 \cos^2(\omega_c t) dt = \frac{A_c^2}{2}$$ ......

(5)

The sideband power $P_{sideband}$ is the power of $m(t)\cos(\omega_c t)$ which is

$$P_{sideband} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{T/2} m^2(t) \cos^2(\omega_c t) dt = \frac{1}{2} \overline{m^2}(t)$$ ......

(6)

Hence, the power efficiency is defined as

$$\eta = \frac{\text{useful power}}{\text{total power}} = \frac{P_{useful}}{P_{carrier} + P_{useful}} = \frac{\overline{m^2}(t)}{A_c^2 + \overline{m^2}(t)} 100\% \ , \ \text{where } \overline{m^2}(t) = \text{Average signal power}$$

......

(7)

As a special case of tone modulation $m(t) = A_m \cos(\omega_m t)$, we have average signal power $\overline{m^2}(t) = \frac{A_m^2}{2}$. Hence, the power efficiency for this special case of **tone modulation** is

$$\eta = \frac{\text{useful power}}{\text{total power}} = \frac{P_{useful}}{P_{carrier} + P_{useful}} = \frac{\dfrac{A_m^2}{2}}{A_c^2 + \dfrac{A_m^2}{2}} = \frac{A_m^2}{2A_c^2 + A_m^2} = \frac{\mu^2}{2 + \mu^2}$$ ......

(8)

Where μ is the modulation index, and its value is in the range $0 \le \mu \le 1$. The following can be observed:

1. Power efficiency η increases monotonically with the modulation index μ

2. It can be observed that the maximum value of power efficiency μ_{max} occurs at $\mu_{max} = 1$, for which $\mu_{max} = 33\%$. Therefore, clearly for tone modulation case

(considering no noise), even in the best possible scenario, only 33% of the total power transmitted is a useful power, i.e., the power used for carrying the information.

3. A smaller value of μ would mean poor power efficiency, and the maximum value that can be used is $\mu_{max} = 1$. For this reason, to achieve maximum power efficiency in AM, full modulation has to be maintained most of the time. Therefore, in practice, volume compression and peak limiting are usually done in AM.

Another useful relation between total power and carrier power (for monotone signal, and can be expanded for the case of multi-tone signals) can be derived using equation (5) and (6) as

$$P_{total} = P_{carrier} + P_{sideband} = \frac{A_c^2}{2} + \frac{A_m^2}{4} = \frac{A_c^2}{2}\left(1 + \frac{\mu^2}{2}\right) = P_{carrier}\left(1 + \frac{\mu^2}{2}\right) \qquad \ldots\ldots$$

(9)

Example 1: What will be the power efficiency for total power carried by the sidebands of the AM wave for tone modulation when (a) $\mu = 0.5$ and (b) $\mu = 0.3$

Solution 1: For the modulation index $\mu = 0.5$, $\eta = \frac{\mu^2}{2 + \mu^2}100\% = \frac{(0.5)^2}{2 + (0.5)^2}100\% = 11.11\%$.

Hence, only 11.11% of the total power is useful and lies in the sidebands. For the modulation index $\mu = 0.3$, $\eta = \frac{\mu^2}{2 + \mu^2}100\% = \frac{(0.3)^2}{2 + (0.3)^2}100\% = 4.3\%$. Therefore, only 4.3% of the total power is a useful power that lies in the sidebands.

Example 2: The peak voltage of an AM signal varies from 2V to 10V (assume sinusoids). Find the total power and power efficiency.

Solution 2: We know that $\mu = \frac{A_m}{A_c}$. The maximum peak of an AM signal

$A_{max} = A_c + A_m = A_c(1 + \mu)$. Similarly, the minimum peak of an AM signal

$A_{min} = A_c - A_m = A_c(1 - \mu)$. Therefore, we can write the modulation index as, $\mu = \frac{A_{max} - A_{min}}{A_{max} + A_{min}}$.

According to this relation we get, $\mu = \frac{A_{max} - A_{min}}{A_{max} + A_{min}} = \frac{10 - 2}{10 + 2} = \frac{8}{12} = 0.66$

Again, using the same relationships given above, we obtain $A_c = \frac{A_{max} + A_{min}}{2} = \frac{10 + 2}{2} = 6$ volts. Also, since carrier waveform is a sinusoid, its power is

$P_c = \frac{A_c^2}{2} = \frac{6^2}{2} = 18$ watts. Hence, the total power is

$P_t = P_c \left(1 + \dfrac{\mu^2}{2}\right) = 18\left(1 + \dfrac{0.66^2}{2}\right) = 22$ watts. Now, since we have all the unknown

components, the power efficiency can be calculated as $\eta = \dfrac{\mu^2}{2 + \mu^2} = \dfrac{0.66^2}{2 + 0.66^2} = 18\%$.

6.3.4 SINGLE SIDE BAND (SSB) MODULATION

You should have observed by now that in AM and even in DSB-SC signals, the lower sideband (LSB) and upper sideband (USB) are symmetric about the carrier frequency ω_c. This would simply mean that, if the information about the amplitude and phase spectrum is completely known in any one of the bands, then the information about the other band can be obtained from it. This means that for the transmission of information, only one sideband can be transmitted. This, in turn, implies that the bandwidth can be saved when only one sideband is transmitted. Further, if the carrier component and one of the sideband is not transmitted (which is present in AM signals), the power required for transmission will be lower than what is required for the AM or DSB-SC case. In general, for a message signal m(t), the SSB signal can be described as:

$$\phi_{ssb}(t) = m(t)\cos(\omega_c t) \mp m_h(t)\sin(\omega_c t) \qquad \ldots\ldots (10)$$

Where the minus sign applies to USB, and the plus sign applies to LSB. $m_h(t)$ denotes the **Hilbert transform** of the message signal m(t) and is defined as

$$m_h(t) = m(t) * h(t) = m(t) * \frac{1}{\pi t} = \frac{1}{\pi}\int_{-\infty}^{\infty} \frac{m(\alpha)}{t - \alpha}\, d\alpha \qquad \ldots\ldots$$

(11)

Equation (11) tells us that if the message signal m(t) is passed through a filter (Hilbert transformer) with the impulse response $h(t) = \dfrac{1}{\pi t}$, then the output is $m_h(t)$. The transfer function of the filter, $H(\omega) = -j\,\mathrm{sgn}(\omega)$, can be obtained by performing the Fourier transform of the impulse function h(t). Therefore, the Fourier domain representation of equation (11), i.e., the Hilbert transform of the message signal m(t) in the frequency domain, is $M_h(\omega) = -jM(\omega)\mathrm{sgn}(\omega)$. Since

$$H(\omega) = -j\,\mathrm{sgn}(\omega) = \begin{cases} -j = 1e^{-j\pi/2} & \omega > 0 \\ j = 1e^{j\pi/2} & \omega > 0 \end{cases} \qquad \ldots\ldots (12)$$

it implies that $|H(\omega)| = 1$ and $\theta_h(\omega) = \begin{cases} -\pi/2 & \omega > 0 \\ \pi/2 & \omega < 0 \end{cases}$. This further means that if we delay each

and every component of m(t) by $\pi/2$ keeping the magnitude constant, the resulting signal we

will get is $m_h(t)$. Therefore, a Hilbert transformer is simply an ideal phase shifter which shifts the phase of every spectral component by a phase of $-\pi/2$.

6.3.5 SSB GENERATION

Now we know that the SSB signal consists of only one sideband (either LSB or USB), and equation (10) is what defines an SSB signal. This gives us two methods using which we can generate an SSB signal. In the first method, a sharp cutoff filter is used to eliminate the undesired sideband, whereas, in the second method, we use phase-shifting networks to implement equation (10) and produce an SSB signal. Let us now briefly discuss them:

1. **Selective-Filtering Method:** It is the most common method of generating SSB signals. In this method, we pass a DSB-SC signal through a very sharp cutoff filter, and the undesired sideband is removed. E.g., If we want to obtain USB, then the cutoff filter should be designed in such a way that all the components below the carrier frequency ω_c must be removed, and all the components above the carrier frequency ω_c must be passed. The disadvantage of this method is that the realization of an ideal or sharp cutoff filter is impossible.

2. **Phase-Shift Method:** In this method, SSB is generated using equation (10), as shown in figure 5 below. In this, the block containing $\left(-\pi/2\right)$ is a phase shifter which shifts the phase by delaying each and every spectral component by $\pi/2$ radians. Therefore, it behaves like a Hilbert transformer, as mentioned in the above section.

   NOTE: An ideal phase shifter is also unrealizable, but at most, it can be approximated over some finite band. However, we can realize a filter having two outputs of the same (constant) amplitude spectrum, and the phase spectrums are such that one output has a phase spectrum of $\phi(\omega)$ whereas that of the other has the phase spectrum of $\phi(\omega)-\pi/2$. The term $\phi(\omega)$ is an unwanted phase distortion. However, the human ear is insensitive to this phase distortion.
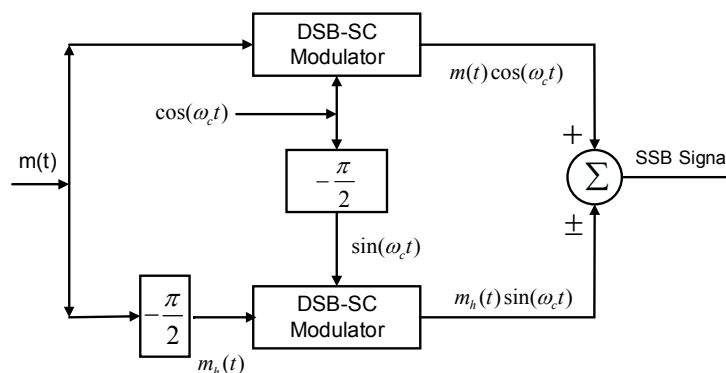

Fig.5 SSB generation using phase-shift method

Example 3: An AM transmitter power is given by 500 Watt. Find the amount of power saved if the carrier and one of the sideband is suppressed with $\mu = 0.8$?

Solution 3: Compared to AM, power saved in SSB can be derived to be

$$\frac{\text{Power saved}}{\text{Total Power}} = \frac{P_c + \dfrac{P_c \mu^2}{4}}{P_c\left(1 + \dfrac{\mu^2}{2}\right)} = \frac{4 + \mu^2}{4 + 2\mu^2}$$

Therefore, the percentage of power saved is 87.8%. Amount of power saved is 87.8 % of Total Power = 87.8 % * 500 = 439.39 watts

6.3.6 AM AND SSB DETECTION

1. **AM Detection:** AM signal can be deducted both coherently and non-coherently. The advantage offered by AM, as discussed in the above sections, is that it allows for a cheap and simple detector, which is not possible in the case of any other modulations. One such simple detector is the envelope detector.

    Envelope detectors are the most commonly used commercial AM radio receiver because of its simplicity and cost-effectiveness. A typical envelope detector is shown in figure 6. In an envelope detector, during the positive half cycle of the input AM signal, the diode D gets forward biased, and the capacitor C starts charging up rapidly to the maximum value of the input signal. Now when the input signal value falls below this maximum value, the diode becomes reverse-biased, and the capacitor C starts discharging through the load resistor R_l. This discharging of the capacitor continues until the next positive half cycle of the input AM signal. When the input signal becomes greater than the voltage across the capacitor C, the diode starts to conduct again, and the whole process repeats again.
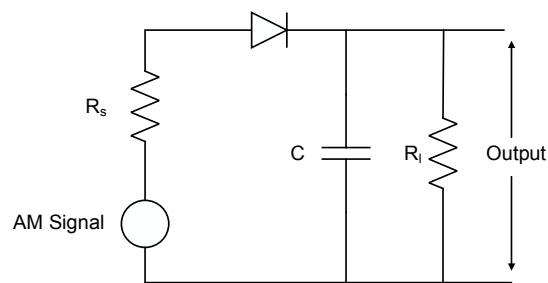

Fig. 6 Envelope Detector

If the forward resistance of the diode is R_f, then the charging time constant is $(R_f + R_s)C$, and the value of this charging time constant must be small compared to the time period of the carrier wave. By doing so, the capacitor charges rapidly, and thereby it follows the applied voltage to the positive peak of the input AM signal

when the diode is conducting. This can be translated into $(R_f + R_s)C << \dfrac{1}{f_c}$. During the discharging process, the discharging time constant is $R_l C$. This discharging time constant must be large enough to ensure that the capacitor discharges slowly through the load resistor R_l between the positive peaks of the carrier wave, and it should not be that large so that the capacitor voltage discharges at the maximum rate of change of the modulating wave. This all translates into the equation $\dfrac{1}{f_c} << R_l C << \dfrac{1}{W}$, where 'W' is the bandwidth of the message signal, and f_c is the frequency of the carrier wave. So, what this equation ensures is that the capacitor voltage or the detector output voltage is nearly the same as the envelope of the AM wave.

2. **SSB Detection:** SSB signals can be demodulated coherently, and it can be readily verified: We know that an SSB signal is given by
$$\phi_{ssb}(t) = m(t)\cos(\omega_c t) \pm m_h(t)\sin(\omega_c t)$$

Hence,
$$\phi_{ssb}(t)\cos(\omega_c t) = \frac{1}{2}m(t)\left[1+\cos(2\omega_c t)\right] \pm \frac{1}{2}m_h(t)\sin(2\omega_c t) = \frac{1}{2}m(t) + \frac{1}{2}\left[m(t)\cos(2\omega_c t) \pm m_h(t)\sin(2\omega_c t)\right]$$

It can be seen from the above equation that the product $\phi_{ssb}(t)\cos(\omega_c t)$ gives the baseband signal and another SSB signal with the carrier frequency $2\omega_c$. The desired baseband signal, $\frac{1}{2}m(t)$, can be extracted by passing the above signal through a low pass filter of an appropriate frequency.

6.3.7 AUTOMATIC GAIN CONTROL (AGC)

Automatic Gain Control is a system that automatically varies the overall gain of a radio receiver with the variations in the strength of the receiver signal so that the output is kept almost constant. The circuitry of Automatic Gain Control derives the DC bias voltage from the output of the detector. This DC bias voltage is applied to the RF, IF, and mixer stages to control their gains. When the average DC bias voltage level increases, the size of the AGC bias increases, and the gain of the controlled stages decreases. When there is no signal, there will be minimum AGC bias, and the amplifiers will produce a maximum gain. There are mainly two types of AGC circuits: Simple AGC and Delayed AGC.

1. **Simple AGC:** In this, the AGC bias starts to increase as soon as the received signal exceeds the background noise level. As a result, receiver gain starts falling down, reducing the sensitivity of the receiver. In simple AGC, dc bias produced by half-wave rectifier as an AM detector is used to control the gain of RF or IF amplifier. Before we apply this voltage to the base of the RF and or IF stage amplifier, the audio signal is removed by the LPF, and the time constant of the filter is kept at least ten times more than the period of the lowest received modulation frequency. This is done

so because, more the time constant, better will be the filtering. But if this time constant made very large, then it will cause an annoying delay in the application of the AGC control when tuning from one signal to another. The recovered signal is then passed through the C_c to remove the DC. The AC signal is then further amplified and applied to the loudspeaker.

2. **Delayed AGC:** We can observe that in simple AGC, the performance improves compared to when no AGC is used. However, in simple AGC, the unwanted weak signals (noise signals) also gets amplified with high gain. To avoid this, in delayed AGC circuits, AGC bias is not applied to amplifiers until the strength of the signal reaches some predefined threshold value. After this threshold value is attained, the AGC bias is applied as with the case of simple AGC, but more strongly.

6.3.8 RADIO RECEIVER CHARACTERISTICS

The characteristics of a radio receiver that determines its performance are:

1. **Selectivity**: It refers to the ability of a receiver to select a signal of the desired frequency and reject all other frequencies. To select the desired frequency, LC circuits are used and are tuned such that its resonant frequency is the desired frequency. The quality factor, Q (defined as the ratio of inductive inductance to resistance, i.e. $Q = X_L/R$), of these tuned circuits determines the selectivity. Selectivity tells about the attenuation offered by the receiver to the signals at frequencies near to the point of tuning. A receiver is said to be good if it is able to isolate the desired signal from all other signals in the RF spectrum. The bandwidth of the tuned circuit is given by $BW = f_r/Q$, where f_r is the resonant frequency. This bandwidth of the tuned circuit is the measure of selectivity. Narrower the bandwidth BW, better is the selectivity. Therefore, to have narrow bandwidth (to have a good selectivity), the Q factor of the tuned circuit must be high.

2. **Sensitivity**: It refers to the ability of the communication receivers to pick up weak signals and amplify it. It is defined in terms of the voltage that must be applied to the receiver input terminal to give a standard output power at the receiver output terminal. This means that, if the gain of the receiver is more, then even for a small signal at the input will produce the desired output power. It is expressed in microvolts or DB. As discussed above, it can be seen that the sensitivity of the receiver mostly depends upon the gain of the IF amplifiers. Good communication receivers have a sensitivity of 0.2 to 1 μV.

3. **Fidelity**: It refers to the ability of the receiver to reproduce all the modulating frequencies equally. At low frequencies, the fidelity is determined by the low-frequency response of the IF amplifier, whereas at higher frequencies, fidelity is determined by the high frequency of the IF amplifier. It is difficult to obtain Fidelity

in AM receiver because, for good fidelity, the bandwidth of the IF amplifier must be more, which in turn would result in poor selectivity.

4. **Image frequency and its rejection**: In the standard broadcast receiver, the local oscillator frequency is set higher than the signal frequency by an amount equal to an intermediate frequency (IF), i.e. $f_0 = f_s + f_i$. If this oscillator frequency f_0 is mixed with the incoming signal frequency f_s, then at the output, we get f_i as one of the byproducts which is passed and amplified by the IF stages. If a frequency $f_{si} = f_0 + f_i = f_s + 2f_i$ appears at the input of the mixer, then it will produce the sum and difference frequencies regardless of the inputs. Therefore, the mixer output will be the difference frequency at the IF frequency. This frequency f_{si} is known as the **image frequency** and is defined as the sum of signal frequency and twice of intermediate frequency. This image frequency also gets amplified by the IF amplifiers, which results in the interference. This has an effect on receiving two stations simultaneously, which is undesirable. The image rejection ratio (IRR) is characterized by its RF filter and is given by $IRR = \sqrt{1 + \rho^2 Q^2}$, where $\rho = \dfrac{f_{si}}{f_s} - \dfrac{f_s}{f_{si}}$ and Q is the quality factor of the tuned circuit.

5. **Double spotting**: In this, the receiver picks up the same short-wave station at two nearby points on the receiver. This usually occurs at high frequencies because of the poor selectivity of the receivers.

Self-Assessment Question (SAQ) 1: Derive the result used in example 3, i.e., % power saved in SSB compared to that in AM is given by: $\% \text{ Power saved} = \dfrac{4 + \mu^2}{4 + 2\mu^2} * \text{Total Power}$.

Self-Assessment Question (SAQ) 2: What will be the total power of a multi-tone Amplitude Modulated signal? (Multi-tone signal is a signal that is a linear combination of sinusoids of different frequencies)

Self-Assessment Question (SAQ) 3: List the advantages and disadvantages of AM and SSB signals. Also, give one application of each.

Self-Assessment Question (SAQ) 4: A sinusoidal carrier of 1V, 100 MHz, is passed through a product modulator having a sinusoidal message signal of 1V, 1 MHz on the other end. The resulting signal is passed through a High Pass Filter of the cutoff frequency of 100 MHz. The High Pass Filter output is then added with the sinusoidal signal of 1V, 100 MHz, 90^0 phase shift. Find the envelope of output?

(i) $\sqrt{\dfrac{5}{4} - \sin(2\pi * 10^6 t)}$ (ii) $\sqrt{1 + 2\cos(2\pi * 10^6 t)}$ (iii) $\sqrt{2 - \sin(2\pi * 10^6 t)}$ (iv) Constant

6.4 ANGLE MODULATION

So far, we have studied variants of amplitude modulations. Multiple questions should arise in your minds (1) Are we satisfied with AM and its variants? (2) What another scheme can we think of?

To answer the first question, we must visualize and understand how noise affects the message signal when transmitted using any of the variants of the Amplitude Modulation. In radio or voice transmission, the interference to the reception is typically considered as something unwanted and gets added to the received signal. This addition of the desired signal by some other unwanted signal (or even noise), changes the amplitude of the received signal. As we know that the information in AM signal resides in its amplitude, so because of this interference, the information gets distorted. This was a major disadvantage offered by AM, and therefore researchers were in constant search of some other modulation technique to transmit the message. This leads us to the solution of the second question.

Any signal (and in particular sinusoids) consists of two important components: Amplitude and Angle. When the amplitude of the high-frequency carrier wave was varied according to the information/message signal, we obtained Amplitude Modulation. However, if now we encode the information/message signal in the angle of the carrier wave (keeping the amplitude of the carrier wave constant), it would result in Angle Modulation. In Angle Modulation, since all the information resides within the angle of the carrier wave, we can expect that the effect of interference or noise will be minimal or less than it was in Amplitude Modulation.

Once this is understood, it immediately comes in mind that an angle consists of two parts: (1) Frequency and (2) Phase. Therefore, Angle Modulation can be performed in two ways. In the first method, the frequency of the carrier wave can be varied according to the message signal. This is called Frequency Modulation (FM). In the other method, the phase of the carrier wave can be varied according to the message signal. This modulation is known as Phase Modulation (PM). We shall now discuss Analog Modulation mathematically and focus our attention on only one of its variants, i.e., Frequency Modulation (FM).

The general form of Angle Modulation is $s(t) = A_c \cos(\phi_i(t))$, where the subscript "$i$" denotes instantaneous, A_c is the carrier amplitude and $\phi_i(t)$ is the instantaneous angle of modulation in radians. If the phase $\phi_i(t)$ increases monotonically with time, then we can define the average frequency over a time interval $(t, t + \Delta t)$ as

$$f_{\Delta t}(t) = \frac{\phi_i(t, t + \Delta t) - \phi_i(t)}{2\pi \Delta t} \qquad \text{...... (13)}$$

Hence, from the knowledge of calculus, we can now define instantaneous frequency as

$$f_i(t) = \lim_{\Delta t \to 0} f_{\Delta t}(t) = \frac{1}{2\pi} \frac{d}{dt} \phi_i(t) \qquad \text{...... (14)}$$

This implies that

$$\phi_i(t) = 2\pi \int_0^t f_i(t)dt \qquad\qquad \text{……(15)}$$

There can be an infinite number of possibilities that $\phi_i(t)$ can be varied according to the message signal. However, the two most common ways of doing this are:

- Phase Modulation (PM) in which the instantaneous phase varies as $\phi_i(t) = 2\pi f_c t + k_p m(t)$. Here, k_p is known as phase sensitivity.

- Frequency Modulation (FM) in which the instantaneous phase varies according to the equation $\phi_i(t) = 2\pi f_c t + 2\pi k_f \int_0^t m(t)dt$. Here k_f is known as frequency sensitivity.

6.4.1 FREQUENCY MODULATION (FM)

Now we have got some insights about Angle modulation, instantaneous phase, and instantaneous frequency. We also observed how the instantaneous phase varies in PM and FM. Now let us focus on the FM signal. A transmitted FM signal can be described as

$$s(t) = A_c \cos(\phi_i(t)) = A_c \cos(2\pi f_c t + 2\pi k_f \int_0^t m(t)dt) \qquad \text{……(16)}$$

What can be said about the properties of this system? Well, it can be easily seen and verified that the system is Non-linear, Time-varying, memory, and causal. It is because of this non-linear property of the system, which makes it difficult to perform its spectral analysis.

Let us now consider a case of tone-modulation where $m(t) = A_m \cos(2\pi f_m t)$. The instantaneous frequency for this message signal will be

$$f_i(t) = f_c + k_f A_m \cos(2\pi f_m t) = f_c + \Delta f \cos(2\pi f_m t) \qquad \text{……(17)}$$

Where $\Delta f = k_f A_m$ is the frequency deviation, i.e., the maximum frequency deviation from carrier frequency f_c that the instantaneous frequency can have in value. From equations 14 and 17, the instantaneous angle is given by

$$\phi_i(t) = 2\pi \int_0^t f_i(t)dt = 2\pi f_c t + \frac{\Delta f}{f_m} \sin(2\pi f_m t) \qquad \text{……(18)}$$

We define a parameter $\beta = \dfrac{\Delta f}{f_m}$, known as the modulation index. The value of the modulation index lies in the range $0 \leq \beta \leq \infty$. Therefore, the transmitted Frequency Modulated (FM) signal becomes

$$s(t) = A_c \cos\left(2\pi f_c t + \beta \sin(2\pi f_m t)\right) \qquad \text{……(19)}$$

Based on the value of the modulation index, β, we have two extreme cases for Frequency Modulation:

1. **Narrowband FM (NBFM):** FM signal is narrowband when $\beta \ll 1$ where $\beta < 0.3$ is sufficient.

2. **Wideband FM (WBFM):** FM signal is wideband when $\beta \gg 1$ where $\beta > 20$ is sufficient.

6.4.2 FM GENERATION: DIRECT METHOD USING REACTANCE TUBE

Now, let us see how we can generate FM waves. FM waves are usually generated by two methods: Direct method and the Indirect Method. In the Direct Method, a device called voltage-controlled oscillator (VCO) is used whose oscillation frequency depends linearly on the modulating message signal. In the Indirect method, an NBFM signal is first produced using an amplitude modulator. This NBFM signal is then converted into a WBFM signal by frequency multiplications. We shall now focus our attention on the Direct Method using Reactance Tube for FM generation.

Figure 7 below shows a reactance-tube modulator circuitry. In this, a tank circuit of an ordinary oscillator is shunted by the plate cathode of the pentode, called the reactance tube. The arrangement of the pentode is such that it draws a reactive current that is proportional to the message signal m(t).

The voltage V_{gk} (control grid to cathode voltage potential) applied to the control grid of the pentode is 90^0 out of phase with respect to the voltage V_{pk} (plate to cathode voltage potential), that is obtained employing an RC phase splitter, with $R \ll j\omega C$. This results in the pentode to draw a reactive current I_{pk}, which leads the voltage V_{pk} by 90^0. You can think of this as an equivalent circuit where an oscillator plate-cathode circuit is shunted by a capacitive reactance. The modulating signal m(t) is superimposed on the grid voltage of the reactance tube. This varies the trans-conductance of the tube in accordance with the modulating signal m(t), and hence there is a variation in the equivalent resistance offered to V_{pk}. The overall effect of all this is that the instantaneous frequency of the oscillator varies according to the modulating signal m(t). Such a modulator is essentially a Low-Level Modulator, and the power is increased to the desired level through a class-C power amplifier.
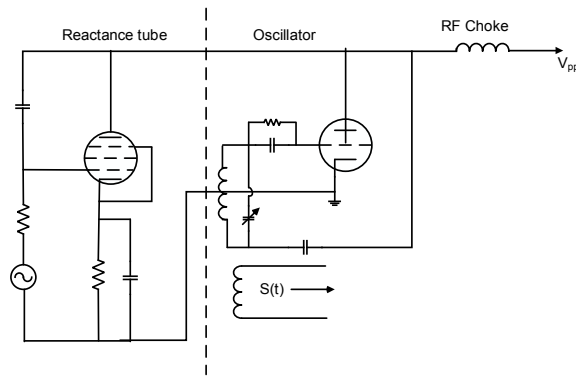
Fig.7 Reactance-Tube Modulator

6.4.3 FM TRANSMITTER

The FM transmitter is a single transistor circuit. Generally speaking, the FM transmitter usually transmits and receives the radio waves in the VHF band, i.e., from 87.5 to 108.0 MHz. This transmitter utilizes the most excellent range with less power. The performance and working of the wireless audio transmitter circuit depend on the values of the inductor and variable capacitor.

The FM transmitter is a low power transmitter, and it uses FM waves for transmitting the sound. The signal in the FM transmitter is transmitted through the carrier wave by the difference frequency. The main components of the FM transmitter are a microphone, audio pre-amplifier, modulator, oscillator, RF-amplifier, and an antenna. In it, we have two frequencies, one is the audio frequency, and the other is the carrier frequency. Figure 8 below shows a typical FM transmitter circuit. It requires a power supply of 9 V and has resistors, capacitors, inductors, microphone, transmitter, and antenna. The microphone converts the sound signals into electrical signals using a capacitive sensor. An NPN transistor is used for amplification. The combination of an inductor and a variable capacitor in parallel forms an oscillating Tank Circuit. On passing the current through this tank circuit, produces a resonant frequency of the FM modulation. Capacitor C_2 connects the output of the tank circuit to the transistor in a negative feedback manner. The input audio signal from the microphone is fed into the base of the transistor, which then modulates the LC tank circuit carrier frequency in the FM format. A variable capacitor can be used to vary the resonant frequency for fine-tuning within the FM frequency range. The modulated signal is then transmitted from the antenna as radio waves in the FM frequency range.
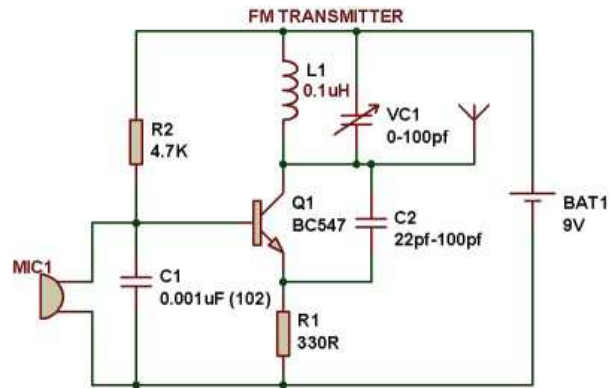
Fig.8: FM Transmitter Circuit [source: https://www.elprocus.com/]

6.4.4 AUTOMATIC FREQUENCY CONTROL (AFC)

AFC circuits are required when we need to accurately control the frequency of an oscillator through some external signal. The purpose of an AFC is twofold (1) It produces a control voltage proportional to the difference in the frequencies of oscillator and the desired signal (2) It uses the control voltage to change the frequency of an oscillator to the desired frequency. AFC circuits can be used to control the frequencies of both the sinusoidal and non-sinusoidal oscillators. AFC circuits are used in radio receivers, FM transmitters, and frequency synthesizers to achieve frequency stability. Figure 9 shows a block diagram illustrating an AFC operation in a receiver.
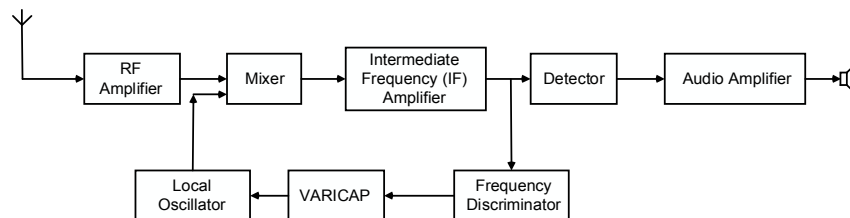
Fig. 9 Block diagram of a receiver with AFC circuit

The frequency discriminator controls the varicap in the receiver circuit shown above. Varicap keeps the IF amplifier to operate in stable mode. The varicap produces an apparent reactance, which is included in the oscillator frequency control circuitry, e.g., let the IF frequency be 455 KHz and let the local oscillator is tracking the incoming signal. When the local oscillator output frequency gets slightly lower than the input frequency, the IF amplifier output will rise. This will, in turn, cause the output of the frequency discriminator to increase the capacitive reactance of the varicap, which in turn increases the oscillator frequency to the desired value. Now let us consider the case when the local oscillator output frequency increases. The IF will then decrease. This will cause the discriminator output to decrease the capacitive reactance of the varicap. This will cause the oscillator frequency to increase.

6.4.5 PHASE-SHIFT DISCRIMINATOR

How can we recover the message signal back from the received FM signal? Several methods can do this, but we should concentrate on one such widely used approach known as a phase-shift discriminator. Phase-shift discriminators consist of circuits that have a linear phase response. This is in contrast to slope detectors, which have a linear amplitude response. The basic principle behind phase-shift discriminators is the approximation for time differentiation, i.e., if t_1 is small compared to the variations in v(t), then we can write it as

$\dot{v}(t) \approx \frac{1}{t_1}\left[v(t) - v(t - t_1)\right]$. We know that phase of an FM wave is $\phi(t) = 2\pi f_c t + 2\pi k_f \int_0^t m(t)dt$.

Therefore, the time-derivative of phase is $\dot{\phi}(t) = 2\pi f_c + 2\pi k_f m(t)$ and if the DC component is removed, (The limiter at the input serves two purposes: (1) to remove any spurious amplitude variations from the input signal s(t) before they reach to BPF and (2) it includes a DC blocker so that the constant carrier frequency offset part can be removed from the output) then we have $\dot{\phi}(t) = 2\pi k_f m(t)$. This can be rewritten as

$$\phi(t) - \phi(t - t_1) \approx t_1\dot{\phi}(t) = 2\pi f_\Delta t_1 m(t) \qquad \text{...... (20)}$$

where f_Δ is the frequency deviation, i.e., the maximum shift relative to the carrier frequency. The term $\phi(t - t_1)$ can be obtained with the help of a delay line or, equivalently, a linear phase shift network.
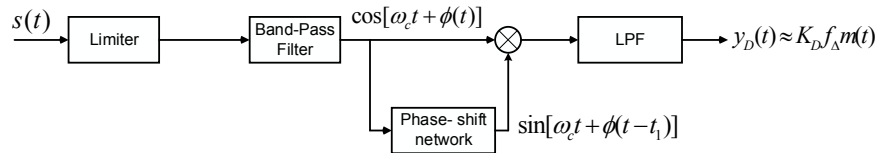
Fig. 10: Phase-shift discriminator or quadrature detector

Figure 10 above shows a phase shift discriminator that is built using a network having group delay t_1 and carrier delay t_0 such that $\omega_c t_0 = 90^0$. It is because of this, phase-shift discriminator is also known as quadrature detector. It can be shown that the output of a phase-shift network is a phase-shifted signal that is proportional to $\cos\left[\omega_c t - 90^o + \phi(t - t_1)\right] = \sin\left[\omega_c t + \phi(t - t_1)\right]$. Multiplication of this signal with $\cos\left[\omega_c t + \phi(t)\right]$ followed by an LPF gives an output proportional to $\sin\left[\phi(t) - \phi(t - t_1)\right] \approx \phi(t) - \phi(t - t_1)$, assuming that t_1 is very small such that $|\phi(t) - \phi(t - t_1)| \square \pi$. Therefore, using equation (20), we have $y_D(t) \approx K_D f_\Delta m(t)$, where the detection constant K_D includes t_1.

It is to be noted that despite all these approximations, a phase shift discriminator provides better linearity than balanced discriminator and is very often found in high-quality receivers.

6.5 NOISE IN AM AND FM

Noise is an unwanted random signal that affects the wanted signal. It can be generated either through an internal source (e.g., noise due to movement of electrons in electronic circuits such as transistors, diodes, resistors etc., thermal noise, shot noise) or an external source (e.g., man-made and natural sources, sources over which we have no control such as atmosphere, cosmic, motors, generators etc.). Signal to Noise Ratio (SNR) is defined as

$$\frac{S}{N} = \frac{\text{Average power of useful signal voltage}}{\text{Average power of noise voltage}} \qquad \text{...... (21)}$$

To compare different continuous-wave modulation systems, we normalize the receiver performance by dividing the output SNR by the SNR of the channel. This ratio is called the Figure Of Merit (FOM). Higher the value of FOM means better is the noise performance of the receiver.

$$\text{FOM } (\gamma) = \frac{(\text{SNR})_o}{(\text{SNR})_c} \qquad \text{...... (22)}$$

Where, $(SNR)_o = \dfrac{\text{Average power of the demodulated message signal}}{\text{Average power of noise}} \Big|_{\text{measured at the receiver output}}$ and

$$(SNR)_c = \frac{\text{Average power of the modulated signal}}{\text{Average power of noise in the message BW}} \Big|_{\text{measured at the receiver input}} \qquad \text{...... (23)}$$

We shall now very briefly see the effect of noise in AM and FM systems:

1. **Effect of Noise in AM Systems:** Noise is introduced in the signal by the channel. Let the noise be an Additive White Gaussian Noise. Total noise can be obtained as a product of noise power spectral density and the bandwidth i.e.

$$N = (\text{noise power spectral density}) * (\text{bandwidth}) = \frac{N_0}{2} * BW \qquad \text{...... (24)}$$

   For AM-SC: For both DSB and SSB, the Figure Of Merit γ is 1. Thus, the S/N ratios at the input and output of the detector are identical, i.e., we do not achieve any improvement in the SNR.

   For conventional AM (DSB-FC): When we use envelope detector then the Figure Of Merit $\gamma = 1/3$ for modulation index $\mu = 1$. Thus, the maximum value that the Figure Of Merit, γ, can have in the case of an AM detection using envelope detector is 1/3 for the modulation index of unity.

2. **Noise in Angle Modulated Systems:** Similar to the case of AM, Figure Of Merit γ, characterizes the noise performance of an angle modulated system. For the case of the

FM signal, $\gamma_{FM} = \dfrac{3}{2}\beta^2$ where β is the modulation index. To get a comparison with the AM signal, $\dfrac{\gamma_{FM}}{\gamma_{AM}} = \dfrac{1}{2}\left(\dfrac{\Delta f}{BW}\right)^2 = \dfrac{1}{2}\beta^2$.

Hence, when $\dfrac{3}{2}\beta^2 > \dfrac{1}{3}$, then, the performance of FM is better than AM. Equivalently we can say that the performance of FM is better than an AM system when $\beta > \dfrac{\sqrt{2}}{3} = 0.471$. We define $\beta = 0.5$ the transition between narrowband FM and wideband FM.

Example 4: An unmodulated carrier frequency is given by 1 MHz. After frequency modulation, the maximum frequency is given by 1.4 MHz. Find the frequency deviation Δf and minimum frequency f_{min}.

Solution 4: Given that: $f_{max} = 1.4$ MHz $= f_c + \Delta f = 1 + \Delta f$. Hence the frequency deviation $\Delta f = 0.4$ MHz. Also, on the same lines, we have $f_{min} = f_c - \Delta f = 1 - 0.4 = 0.6$ MHz.

Example 5: For an FM signal, f_{max} is given by 1.5 MHZ. The total frequency swing is given by 900 kHz. Find f_c, Δf and f_{max}.

Solution 5: Total frequency swing $= 2\Delta f = 900$ KHz. Thus, frequency deviation $\Delta f = 450$ kHz. Now, $f_{max} = 1.5$ MHz $= f_c + \Delta f$. Therefore, $f_c = f_{max} - \Delta f = 1.05$ MHz. and $f_{min} = f_c - \Delta f = 1.05 * 1000 - 450 = 600$ KHz.

Example 6: A sinusoidal carrier of 20 V, 2 MHz if frequency modulated by a message signal of $10\sin(4\pi * 10^3 t)$. Frequency sensitivity constant, K_f, is given by 50KHz/Volt. Find Δf, f_{min}, and f_{max}?

Solution 6: Given, a message signal $m(t) = 10\sin(4\pi * 10^3 t)$ and carrier signal $c(t) = 20\cos(2\pi * 2 * 10^6 t)$. So, $f_{max} = f_c + K_f m(t) = 2000 + 50 * 10 = 2500$ KHz. Also, we have $f_{min} = f_c - K_f m(t) = 2000 - 50 * 10 = 1500$ KHz. We know that $2\Delta f = f_{max} - f_{min}$. Therefore, the frequency deviation $\Delta f = \dfrac{f_{max} - f_{min}}{2} = \dfrac{1000}{2} = 500$ KHz.

Self-Assessment Question (SAQ) 5: _____ and _____ requirements of NBFM is same as AM signal. (Hint: Expand the expression of FM and then use the approximation that for small angle θ, $\cos(\theta) \approx 1$ and $\sin(\theta) \approx \theta$).

Self-Assessment Question (SAQ) 6: AM and NBFM signals having the same modulation index are added together. The resulting signal will be (i) USB (ii) SSB (iii) SSB with carrier (USB with carrier) (iv) Noise

Self-Assessment Question (SAQ) 7: What is Carson's rule for finding the Bandwidth of an FM (wideband) signal? To answer this, you need to look into textbooks and literature.

Self-Assessment Question (SAQ) 8: Power in an angle modulated signal is constant (T/F)?

Self-Assessment Question (SAQ) 9: What is the ideal bandwidth in AM and in NBFM and WBFM (let message signal be bandlimited to f_m)? What is meant by ∞ bandwidth? (Hint: See Carson's rule for finding the bandwidth of WBFM. Observe that it consists of ∞ number of sidebands)

Self-Assessment Question (SAQ) 10: Even though we have studied Phase Modulation (PM) in passing by, can you look at the equations of FM and PM and tell how one signal can be generated by only using the other signal.

6.6 SUMMARY

In this unit, you have studied about two fundamental continuous-wave modulation techniques AM and FM. We also very briefly looked at the effects of noise in these signals. We started with the question: what is modulation, and why do we need to do modulation? We then looked at the situations when the amplitude of the carrier signal is used to carry the message signal. This modulated signal is called as AM. We saw how AM signal could be generated as well as how the message signal can be retrieved back for the AM signal at the receiver. One of the advantages offered by the AM signal is the availability of very cheap receivers that uses an envelope detector. We also looked at the power considerations in the case of AM. The bandwidth of the transmitted AM signal is twice the bandwidth of the message signal, and the power required for a transmission includes the carrier power. Since the carrier signal contains no information, it results in a wasteful power. To mitigate these disadvantages, a more bandwidth-efficient scheme of SSB was introduced. We saw how this SSB signal could be generated, and the message signal can be demodulated from an SSB signal at the receiver. We then also studied Automatic Gain Control and looked at the characteristics of a good receiver.

In the next section, we observed that, as the information in an AM signal resides in its amplitude, so it is very much susceptible to noise. So, with this motivation in mind, we looked for another modulation scheme, which led us to angle modulation. In angle modulation, the information resides in the angle of the carrier signal. It can be further subdivided into Frequency Modulation and Phase Modulation. We then studied in detail about what is FM, PM, and how FM signal can be generated and demodulated at the receiver. We also studied about Automatic Frequency Control and its importance in the FM transmitter and receiver. Towards the end, we also briefly studied how noise affects the AM and FM signals.

6.7 GLOSSARY

Bandwidth – (Maximum +ve frequency) - (Minimum +ve frequency)

Frequency Spectrum- distribution of amplitudes and phases of each frequency component Vs. frequency

Amplitude Spectrum- distribution of amplitude Vs. frequency

Frequency- the number of waves that pass a fixed place in a given amount of time.

Carrier Wave/ signal- Usually a wave of higher frequency

Message signal- Usually a low frequency signal which contains useful information that we want to transmit to a distant place e.g. voice, image, video, text etc.

LPF and BPF- They stand for Low Pass Filter and Band Pass Filter. LPF allows low frequencies to pass and stop (attenuates) high-frequency components to pass through them. BPF allows only a band of frequencies to pass through them and stops (attenuates) high-frequency components to pass.

6.8 REFERENCES

1. Modern Digital and Analog Communication Systems, BP Lathi, Oxford University Press

2. Communication Systems, Simon Haykin, John Wiley and Sons

3. Communication Systems Engineering, John G. Proakis, Pearson Education

4. Principles of Communication Systems, Taub H. and Schilling D.L., Tata McGraw Hill

6.9 SUGGESTED READINGS

1. Digital and Analog Communication Systems, Leon W. Couch, Pearson

2. Analog and Digital Communications, Simon Haykin, Wiley India Pvt Ltd

6.10 TERMINAL QUESTIONS

(Should be divided into Short Answer Type, Long Answer Type, Numerical, Objective type)

6.10.1 Short Answer type

1. Which of the following analog modulation scheme requires the minimum transmitted power and minimum channel bandwidth?

   (A) AM   (B) SSB   (C) DSB-SC   (D) None of the above

2. A DSB-SC signal is generated using the carrier $\cos(\omega_c t + \theta)$ and modulating signal x(t). The envelope of the DSB-SC signal is

   (A) $x(t)$ (B) $|x(t)|$ (C) only positive part of $x(t)$ (D) $x(t)\cos(\theta)$

3. $v(t) = 5\left[\cos(10^6 \pi t) - \sin(10^3 \pi t) \times \sin(10^6 \pi t)\right]$ represents

        (A) DSB-SC signal (B) AM signal (C) SSB upper sideband signal (D) NBFM signal

4. Mention the difference between AM and FM signals.

6.10.2 Long Answer type

1. What is Narrowband FM and Wideband FM? What will be their bandwidth and power requirements?

2. What is a Hilbert Transform? How does Hilbert Transform help in generating SSB signals? Explain how equation (10) generates or represents an SSB signal.

3. Explain AM and FM Modulation and Demodulation systems. What is meant by Synchronous demodulation? How can AM and FM be synchronously detected?

4. Write notes on-

   (i) Power requirements of AM signal (ii) Noise in AM systems (iii) Noise in FM systems

6.10.3 Numerical Answer type

1. Consider the signal $s(t) = m(t)\cos(2\pi f_c t) + \hat{m}(t)\sin(2\pi f_c t)$, where $\hat{m}(t)$ denotes the Hilbert transform of m(t), and the bandwidth of m(t) is very small compared to f_c. The signal s(t) is a

(A) High-Pass Signal (B) Low-Pass Signal (C) Bandpass Signal   (D) Double sideband suppressed carrier signal

2. Consider an FM signal $f(t) = \cos\left[2\pi f_c t + \beta_1 \sin(2\pi f_1 t) + \beta_2 \sin(2\pi f_2 t)\right]$. The maximum deviation of the instantaneous frequency from the carrier frequency f_c is

(A) $\beta_1 f_1 + \beta_2 f_2$ (B) $\beta_1 f_2 + \beta_2 f_1$ (C) $\beta_1 + \beta_2$ (D) $f_1 + f_2$

3.   Consider   an   angle   modulated   signal $s(t) = 6\cos\left[2\pi 10^6 t + 2\sin(8000\pi t) + 4\cos(8000\pi t)\right]$ V. What is the average power if x(t)?

4. A modulated signal is given by $s(t) = m_1(t)\cos(2\pi f_c t) + m_2(t)\sin(2\pi f_c t)$, where the baseband signal $m_1(t)$ and $m_2(t)$ have bandwidths 10 kHz and 15 kHz, respectively. What is the bandwidth of the modulated signal s(t)?

5. An AM signal is detected using an envelope detector. The carrier frequency and modulating signal frequency are 1 MHz and 2 MHz, respectively. An appropriate value for the time constant of the envelope detector is

(A) 500μsec   (B) 20 μsec   (C) 0.2 μsec   (D) 1 μsec

6.11 ANSWERS

6.11.1 Self-Assessment Questions (SAQs):

1. Note that: $\% \text{ Power Saved} = \dfrac{\text{Power Saved}}{\text{Total Power}} \bullet 100$. Total power in an AM signal is-

$P_c\left(1 + \dfrac{\mu^2}{2}\right)$. This consists of carrier power and power of two sidebands. However, in SSB, we have only one sideband. Therefore, power saved = Carrier Power + Power of one

sideband $= P_c + \dfrac{P_c\mu^2}{4}$. Hence, the % of power saved will be $\dfrac{P_c + \dfrac{P_c\mu^2}{4}}{P_c\left(1 + \dfrac{\mu^2}{2}\right)} = \dfrac{4 + \mu^2}{4 + 2\mu^2}$

2. If the AM signal is $S_{AM}(t) = A_c(1 + \mu_1\cos(2\pi f_{m1}t) + \mu_2\cos(2\pi f_{m2}t))\cos(2\pi f_c t)$, then total

power transmitted is $P_t = P_c\left\{1 + \dfrac{\mu_t^2}{2}\right\}$, where the total modulation index $\mu_t = \sqrt{\mu_1^2 + \mu_2^2}$

3. Advantage of AM: simpler demodulation, used for long-distance communication.

Disadvantages of AM: Transmitter power is wasted (maximum power efficiency = 33%), needs high transmission bandwidth, profoundly affected by noise.

Applications of AM: preferred to be used in broadcasting (for point-to-multipoint communication) since the AM receiver is simple & cheaper.

Advantage of SSB: transmitter power is saved, transmitter bandwidth is saved

Disadvantages of SSB: demodulation is complex, limited only for voice signal transmission.

Applications of SSB: preferred for voice signal transmission.

4. The correct option is (i)

5. Bandwidth and Power

6. SSB with the carrier, i.e., option (c)

7. According to Carson, WBFM consist of the significant sidebands up to "$\beta + 1$" where the modulation index is β. The bandwidth of WBFM is given by: $BW = (\beta + 1)2f_m$

8. True.

9. WBFM consists of carrier frequency components, ∞ number of USB, and ∞ number of LSB. Therefore, the actual Bandwidth of WBFM is ∞. For WBFM, the strength of higher-order sidebands goes on decreasing and finally becomes zero.

10. PM from FM: Pass the message signal from a differentiator and then pass the resultant from a Frequency Modulator circuit. The output will be a PM signal.

   FM from PM: Pass the message signal from an integrator and then pass the resultant from a Phase Modulator circuit. The output will be an FM signal.

6.11.2 Terminal Questions: Short Answer type

1. (B)

2. (B)

3. (D)

6.11.3 Numerical type question

1. Band-Pass Signal. Correct option is (C)

2. The correct option is (A).

3. average power $= \left(\dfrac{A_c}{\sqrt{2}} \right)^2 = \left(\dfrac{6}{\sqrt{2}} \right)^2 = 18$

4. 30 kHz

5. (B)

UNIT 7   ANTENNA

Structure

7.1 INTRODUCTION

An antenna is an array of conductors (elements), electrically connected to the receiver or transmitter. Antennas are required by any radio receiver or transmitter to couple its electrical connection to the electromagnetic field. Radio waves are electromagnetic waves which carry signals through the air (or through space) at the speed of light with almost no transmission loss.

The dipole antenna, which is the basis for most antenna designs, is a balanced component, with equal but opposite voltages and currents applied at its two terminals. The vertical antenna is a monopole antenna, not balanced with respect to ground.

A phased array consists of two or more simple antennas which are connected together through an electrical network.

An electromagnetic wave refractor in some aperture antennas is a component which due to its shape and position functions to selectively delay or advance portions of the electromagnetic wavefront passing through it.

High frequency (HF) is the ITU designation for the range of radio frequency electromagnetic waves (radio waves) between 3 and 30 megahertz (MHz).

A Yagi–Uda antenna or simply Yagi antenna, is a directional antenna consisting of two or more parallel resonant antenna elements in an end-fire array

A communications satellite is an artificial satellite that relays and amplifies radio telecommunication signals via a transponder; it creates a communication channel between a source transmitter and a receiver at different locations on Earth.

An image orthicon camera can take television pictures by candlelight because of the more ordered light-sensitive area and the presence of an electron multiplier at the base of the tube, which operated as a high-efficiency amplifier. A vidicon tube is a video camera tube design in which the target material is a photoconductor.

7.2 OBJECTIVES

After studying this unit, you will learn about-

- Antenna
- Properties of Antenna
- Yagi Antenna
- Loop Antenna
- HF Antenna
- Satellite Communication
- Image Orthicon
- Videocon

7.3. ANTENNA (RADIO): In radio engineering, an antenna or aerial is the interface between radio waves propagating through space and electric currents moving in metal conductors, used with a transmitter or receiver. In transmission, a radio transmitter supplies an electric current to the antenna's terminals, and the antenna radiates the energy from the current as electromagnetic waves (radio waves). In reception, an antenna intercepts some of the power of a radio wave in order to produce an electric current at its terminals that is applied to a receiver to be amplified. Antennas are essential components of all radio equipment.

An antenna is an array of conductors (elements), electrically connected to the receiver or transmitter. Antennas can be designed to transmit and receive radio waves in all horizontal directions equally (omnidirectional antennas), or preferentially in a particular direction (directional, or high-gain, or "beam" antennas). An antenna may include components not connected to the transmitter, parabolic reflectors, horns, or parasitic elements, which serve to direct the radio waves into a beam or other desired radiation pattern. Strong directivity and good efficiency when transmitting are hard to achieve with antennas with dimensions that are much smaller than a half wavelength.

Antennas are required by any radio receiver or transmitter to couple its electrical connection to the electromagnetic field. Radio waves are electromagnetic waves which carry signals through the air (or through space) at the speed of light with almost no transmission loss.

Antennas can be classified as omnidirectional, radiating energy approximately equally in all horizontal directions, or directional, where radio waves are concentrated in some direction(s). A so-called beam antenna is unidirectional, designed for maximum response in the direction of the other station, whereas many other antennas are intended to accommodate stations in various directions but is not truly omnidirectional. Since antennas obey reciprocity the same radiation pattern applies to transmission as well as reception of radio waves. A hypothetical antenna that radiates equally in all vertical as well as all horizontal angles is called an isotropic radiator however these cannot exist in practice nor would they be particularly desired. For most terrestrial communications, rather, there is an advantage in reducing radiation toward the sky or ground in favor of horizontal direction(s). A dipole antenna oriented horizontally sends no energy in the direction of the conductor this is called the antenna null but is usable in most other directions. A number of such dipole elements can be combined into an antenna array such as the Yagi-Uda in order to favor a single horizontal direction, thus termed a beam antenna.

The dipole antenna, which is the basis for most antenna designs, is a balanced component, with equal but opposite voltages and currents applied at its two terminals. The vertical antenna is a monopole antenna, not balanced with respect to ground. The ground (or any large conductive surface) plays the role of the second conductor of a dipole. Since monopole antennas rely on a conductive surface, they may be mounted with a ground plane to approximate the effect of being mounted on the Earth's surface.

More complex antennas increase the directivity of the antenna. Additional elements in the antenna structure, which need not be directly connected to the receiver or transmitter, increase its directionality. Antenna "gain" describes the concentration of radiated power into a particular solid angle of space. "Gain" is perhaps an unfortunately chosen term, by comparison with amplifier "gain" which implies a net increase in power. In contrast, for antenna "gain", the power increased in the desired direction is at the expense of power reduced in undesired directions. Unlike amplifiers, antennas are electrically "passive" devices which conserve total power, and there is no increase in total power above that delivered from the power source (the transmitter), only improved distribution of that fixed total.

A phased array consists of two or more simple antennas which are connected together through an electrical network. This often involves a number of parallel dipole antennas with certain spacing. Depending on the relative phase introduced by the network, the same combination of dipole antennas can operate as a "broadside array" (directional normal to a line connecting the elements) or as an "end-fire array" (directional along the line connecting the elements). Antenna arrays may employ any basic (omnidirectional or weakly directional) antenna type, such as dipole, loop or slot antennas. These elements are often identical.

Log-periodic and frequency-independent antennas employ self-similarity in order to be operational over a wide range of bandwidths. The most familiar example is the log-periodic dipole array which can be seen as a number (typically 10 to 20) of connected dipole elements with progressive lengths in an endfire array making it rather directional; it finds use especially as a rooftop antenna for television reception. On the other hand, a Yagi–Uda antenna (or simply "Yagi"), with a somewhat similar appearance, has only one dipole element with an electrical connection; the other parasitic elements interact with the electromagnetic field in order to realize a highly directional antenna but with a narrow bandwidth.

Even greater directionality can be obtained using aperture antennas such as the parabolic reflector or horn antenna. Since high directivity in an antenna depends on it being large compared to the wavelength, highly directional antennas (thus with high antenna gain) become more practical at higher frequencies (UHF and above).

At low frequencies (such as AM broadcast), arrays of vertical towers are used to achieve directionality and they will occupy large areas of land. For reception, a long Beverage antenna can have significant directivity. For non directional portable use, a short vertical antenna or small loop antenna works well, with the main design challenge being that of impedance matching. With a vertical antenna a loading coil at the base of the antenna may be employed to cancel the reactive component of impedance; small loop antennas are tuned with parallel capacitors for this purpose.

An antenna lead-in is the transmission line, or feed line, which connects the antenna to a transmitter or receiver. The "antenna feed" may refer to all components connecting the antenna to the transmitter or receiver, such as an impedance matching network in addition to the transmission line. In a so-called "aperture antenna", such as a horn or parabolic dish, the

"feed" may also refer to a basic radiating antenna embedded in the entire system of reflecting elements (normally at the focus of the parabolic dish or at the throat of a horn) which could be considered the one active element in that antenna system. A microwave antenna may also be fed directly from a waveguide in place of a (conductive) transmission line.

An antenna counterpoise, or ground plane, is a structure of conductive material which improves or substitutes for the ground. It may be connected to or insulated from the natural ground. In a monopole antenna, this aids in the function of the natural ground, particularly where variations (or limitations) of the characteristics of the natural ground interfere with its proper function. Such a structure is normally connected to the return connection of an unbalanced transmission line such as the shield of a coaxial cable.

An electromagnetic wave refractor in some aperture antennas is a component which due to its shape and position functions to selectively delay or advance portions of the electromagnetic wavefront passing through it. The refractor alters the spatial characteristics of the wave on one side relative to the other side. It can, for instance, bring the wave to a focus or alter the wave front in other ways, generally in order to maximize the directivity of the antenna system. This is the radio equivalent of an optical lens.

An antenna coupling network is a passive network (generally a combination of inductive and capacitive circuit elements) used for impedance matching in between the antenna and the transmitter or receiver. This may be used to minimize losses on the feed line, by reducing transmission line's standing wave ratio, and to present the transmitter or receiver with a standard resistive impedance needed for its optimum operation. The feed point location(s) is selected, and antenna elements electrically similar to tuner components may be incorporated in the antenna structure itself, to improve the match.

7.3.1. RECIPROCITY:
It is a fundamental property of antennas that the electrical characteristics of an antenna described such as gain, radiation pattern, impedance, bandwidth, resonant frequency and polarization, are the same whether the antenna is transmitting or receiving. For example, the "receiving pattern" (sensitivity as a function of direction) of an antenna when used for reception is identical to the radiation pattern of the antenna when it is driven and functions as a radiator. This is a consequence of the reciprocity theorem of electromagnetics. Therefore, in discussions of antenna properties no distinction is usually made between receiving and transmitting terminology, and the antenna can be viewed as either transmitting or receiving, whichever is more convenient.

A necessary condition for the reciprocity property is that the materials in the antenna and transmission medium are linear and reciprocal. Reciprocal (or bilateral) means that the material has the same response to an electric current or magnetic field in one direction, as it has to the field or current in the opposite direction. Most materials used in antennas meet these conditions, but some microwave antennas use high-tech components such as isolators and circulators, made of nonreciprocal materials such as ferrite. These can be used to give the antenna a different behavior on receiving than it has on transmitting, which can be useful in applications like radar.

7.3.2. RESONANT ANTENNAS: The majority of antenna designs are based on the resonance principle. This relies on the behaviour of moving electrons, which reflect off surfaces where the dielectric constant changes, in a fashion similar to the way light reflects when optical properties change. In these designs, the reflective surface is created by the end of a conductor, normally a thin metal wire or rod, which in the simplest case has a feed point at one end where it is connected to a transmission line. The conductor, or element, is aligned with the electrical field of the desired signal, normally meaning it is perpendicular to the line from the antenna to the source (or receiver in the case of a broadcast antenna).

The radio signal's electrical component induces a voltage in the conductor. This causes an electrical current to begin flowing in the direction of the signal's instantaneous field. When the resulting current reaches the end of the conductor, it reflects, which is equivalent to a 180-degree change in phase. If the conductor is 1⁄4 of a wavelength long, current from the feed point will undergo 90 degree phase change by the time it reaches the end of the conductor, reflect through 180 degrees, and then another 90 degrees as it travels back. That means it has undergone a total 360 degree phase change, returning it to the original signal. The current in the element thus adds to the current being created from the source at that instant. This process creates a standing wave in the conductor, with the maximum current at the feed.

The ordinary half-wave dipole is probably the most widely used antenna design. This consists of two 1⁄4 wavelength elements arranged end-to-end, and lying along essentially the same axis (or collinear), each feeding one side of a two-conductor transmission wire. The physical arrangement of the two elements places them 180 degrees out of phase, which means that at any given instant one of the elements is driving current into the transmission line while the other is pulling it out. The monopole antenna is essentially one half of the half-wave dipole, a single 1⁄4 wavelength element with the other side connected to ground or an equivalent ground plane (or counterpoise). Monopoles, which are one-half the size of a dipole, are common for long-wavelength radio signals where a dipole would be impractically large. Another common design is the folded dipole which consists of two (or more) half-wave dipoles placed side by side and connected at their ends but only one of which is driven.

The standing wave forms with this desired pattern at the design operating frequency, fo, and antennas are normally designed to be this size. However, feeding that element with 3 f0 (whose wavelength is 1⁄3 that of fo) will also lead to a standing wave pattern. Thus, an antenna element is also resonant when its length is 3⁄4 of a wavelength. This is true for all odd multiples of 1⁄4 wavelength. This allows some flexibility of design in terms of antenna lengths and feed points. Antennas used in such a fashion are known to be harmonically operated.[15] Resonant antennas usually use a linear conductor (or element), or pair of such elements, each of which is about a quarter of the wavelength in length (an odd multiple of quarter wavelengths will also be resonant). Antennas that are required to be small compared to the wavelength sacrifice efficiency and cannot be very directional. Since wavelengths are so small at higher frequencies (UHF, microwaves) trading off performance to obtain a smaller physical size is usually not required.

7.3.3. CURRENT AND VOLTAGE DISTRIBUTION: The quarter-wave elements imitate a series-resonant electrical element due to the standing wave present along the conductor. At the resonant frequency, the standing wave has a current peak and voltage node (minimum) at the feed. In electrical terms, this means the element has minimum reactance, generating the maximum current for minimum voltage. This is the ideal situation, because it produces the maximum output for the minimum input, producing the highest possible efficiency. Contrary to an ideal (lossless) series-resonant circuit, a finite resistance remains (corresponding to the relatively small voltage at the feed-point) due to the antenna's radiation resistance as well as any actual electrical losses.

Recall that a current will reflect when there are changes in the electrical properties of the material. In order to efficiently transfer the received signal into the transmission line, it is important that the transmission line has the same impedance as its connection point on the antenna, otherwise some of the signal will be reflected backwards into the body of the antenna; likewise part of the transmitter's signal power will be reflected back to transmitter, if there is a change in electrical impedance where the feedline joins the antenna. This leads to the concept of impedance matching, the design of the overall system of antenna and transmission line so the impedance is as close as possible, thereby reducing these losses. Impedance matching is accomplished by a circuit called an antenna tuner or impedance matching network between the transmitter and antenna. The impedance match between the feedline and antenna is measured by a parameter called the standing wave ratio (SWR) on the feedline.

Consider a half-wave dipole designed to work with signals with wavelength 1 m, meaning the antenna would be approximately 50 cm from tip to tip. If the element has a length-to-diameter ratio of 1000, it will have an inherent impedance of about 63 ohms resistive. Using the appropriate transmission wire or balun, we match that resistance to ensure minimum signal reflection. Feeding that antenna with a current of 1 Ampere will require 63 Volts, and the antenna will radiate 63 Watts (ignoring losses) of radio frequency power. Now consider the case when the antenna is fed a signal with a wavelength of 1.25 m; in this case the current induced by the signal would arrive at the antenna's feedpoint out-of-phase with the signal, causing the net current to drop while the voltage remains the same. Electrically this appears to be a very high impedance. The antenna and transmission line no longer have the same impedance, and the signal will be reflected back into the antenna, reducing output. This could be addressed by changing the matching system between the antenna and transmission line, but that solution only works well at the new design frequency.

The result is that the resonant antenna will efficiently feed a signal into the transmission line only when the source signal's frequency is close to that of the design frequency of the antenna, or one of the resonant multiples. This makes resonant antenna designs inherently narrow-band: Only useful for a small range of frequencies centered around the resonance(s).

7.3.4. ELECTRICALLY SHORT ANTENNAS: It is possible to use simple impedance matching techniques to allow the use of monopole or dipole antennas substantially

shorter than the 1/ 4 or 1/ 2 wave, respectively, at which they are resonant. As these antennas are made shorter (for a given frequency) their impedance becomes dominated by a series capacitive (negative) reactance; by adding an appropriate size'' loading coil'' a series inductance with equal and opposite (positive) reactance the antenna's capacitive reactance may be cancelled leaving only a pure resistance.

Sometimes the resulting (lower) electrical resonant frequency of such a system (antenna plus matching network) is described using the concept of electrical length, so an antenna used at a lower frequency than its resonant frequency is called an *electrically short antenna*.

For example, at 30 MHz (10 m wavelength) a true resonant 1/ 4 wave monopole would be almost 2.5 meters long, and using an antenna only 1.5 meters tall would require the addition of a loading coil. Then it may be said that the coil has lengthened the antenna to achieve an electrical length of 2.5 meters. However, the resulting resistive impedance achieved will be quite a bit lower than that of a true 1/ 4 wave (resonant) monopole, often requiring further impedance matching (a transformer) to the desired transmission line. For ever shorter antennas (requiring greater "electrical lengthening") the radiation resistance plummets (approximately according to the square of the antenna length), so that the mismatch due to a net reactance away from the electrical resonance worsens. Or one could as well say that the equivalent resonant circuit of the antenna system has a higher Q factor and thus a reduced bandwidth which can even become inadequate for the transmitted signal's spectrum. Resistive losses due to the loading coil, relative to the decreased radiation resistance, entail a reduced electrical efficiency, which can be of great concern for a transmitting antenna, but bandwidth is the major factor that sets the size of antennas at 1 MHz and lower frequencies.

7.3.5. ARRAYS AND REFLECTORS:
The radiant flux as a function of the distance from the transmitting antenna varies according to the inverse-square law, since that describes the geometrical divergence of the transmitted wave. For a given incoming flux, the power acquired by a receiving antenna is proportional to its effective area. This parameter compares the amount of power captured by a receiving antenna in comparison to the flux of an incoming wave (measured in terms of the signal's power density in watts per square metre). A half-wave dipole has an effective area of about $0.13 \lambda 2$ seen from the broadside direction. If higher gain is needed one cannot simply make the antenna larger. Due to the constraint on the effective area of a receiving antenna detailed below, one sees that for an already-efficient antenna design, the only way to increase gain (effective area) is by reducing the antenna's gain in another direction.

If a half-wave dipole is not connected to an external circuit but rather shorted out at the feedpoint, then it becomes a resonant half-wave element which efficiently produces a standing wave in response to an impinging radio wave. Because there is no load to absorb that power, it retransmits all of that power, possibly with a phase shift which is critically dependent on the element's exact length. Thus such a conductor can be arranged in order to transmit a second copy of a transmitter's signal in order to affect the radiation pattern (and feedpoint impedance) of the element electrically connected to the transmitter. Antenna elements used in this way are known as passive radiators.

A Yagi–Uda array uses passive elements to greatly increase gain in one direction (at the expense of other directions). A number of parallel approximately half-wave elements (of very specific lengths) are situated parallel to each other, at specific positions, along a boom; the boom is only for support and not involved electrically. Only one of the elements is electrically connected to the transmitter or receiver, while the remaining elements are passive. The Yagi produces a fairly large gain (depending on the number of passive elements) and is widely used as a directional antenna with an antenna rotor to control the direction of its beam. It suffers from having a rather limited bandwidth, restricting its use to certain applications.

Rather than using one driven antenna element along with passive radiators, one can build an array antenna in which multiple elements are all driven by the transmitter through a system of power splitters and transmission lines in relative phases so as to concentrate the RF power in a single direction. What's more, a phased array can be made "steerable", that is, by changing the phases applied to each element the radiation pattern can be shifted without physically moving the antenna elements. Another common array antenna is the log-periodic dipole array which has an appearance similar to the Yagi (with a number of parallel elements along a boom) but is totally dissimilar in operation as all elements are connected electrically to the adjacent element with a phase reversal; using the log-periodic principle it obtains the unique property of maintaining its performance characteristics (gain and impedance) over a very large bandwidth.

When a radio wave hits a large conducting sheet it is reflected (with the phase of the electric field reversed) just as a mirror reflects light. Placing such a reflector behind an otherwise non-directional antenna will insure that the power that would have gone in its direction is redirected toward the desired direction, increasing the antenna's gain by a factor of at least 2. Likewise, a corner reflector can insure that all of the antenna's power is concentrated in only one quadrant of space (or less) with a consequent increase in gain. Practically speaking, the reflector need not be a solid metal sheet, but can consist of a curtain of rods aligned with the antenna's polarization; this greatly reduces the reflector's weight and wind load. Specular reflection of radio waves is also employed in a parabolic reflector antenna, in which a curved reflecting surface effects focussing of an incoming wave toward a so-called feed antenna; this results in an antenna system with an effective area comparable to the size of the reflector itself. Other concepts from geometrical optics are also employed in antenna technology, such as with the lens antenna.

7.3.6. CHARACTERISTICS: The antenna's power gain (or simply "gain") also takes into account the antenna's efficiency, and is often the primary figure of merit. Antennas are characterized by a number of performance measures which a user would be concerned with in selecting or designing an antenna for a particular application. A plot of the directional characteristics in the space surrounding the antenna is its radiation pattern.

7.3.7. BANDWIDTH: The frequency range or bandwidth over which an antenna functions well can be very wide (as in a log-periodic antenna) or narrow (as in a small loop antenna); outside this range the antenna impedance becomes a poor match to the transmission line and transmitter (or receiver). Use of the antenna well away from its design frequency affects its radiation pattern, reducing its directive gain.

Generally an antenna will not have a feed-point impedance that matches that of a transmission line; a matching network between antenna terminals and the transmission line will improve power transfer to the antenna. A non-adjustable matching network will most likely place further limits the usable bandwidth of the antenna system. It may be desirable to use tubular elements, instead of thin wires, to make an antenna; these will allow a greater bandwidth. Or, several thin wires can be grouped in a cage to simulate a thicker element. This widens the bandwidth of the resonance.

Amateur radio antennas that operate at several frequency bands which are widely separated from each other may connect elements resonant at those different frequencies in parallel. Most of the transmitter's power will flow into the resonant element while the others present a high impedance. Another solution uses traps, parallel resonant circuits which are strategically placed in breaks created in long antenna elements. When used at the trap's particular resonant frequency the trap presents very high impedance (parallel resonance) effectively truncating the element at the location of the trap; if positioned correctly, the truncated element makes a proper resonant antenna at the trap frequency. At substantially higher or lower frequencies the trap allows the full length of the broken element to be employed, but with a resonant frequency shifted by the net reactance added by the trap.

The bandwidth characteristics of a resonant antenna element can be characterized according to its Q where the resistance involved is the radiation resistance, which represents the emission of energy from the resonant antenna to free space.

The Q of a narrow band antenna can be as high as 15. On the other hand, the reactance at the same off-resonant frequency of one using thick elements is much less, consequently resulting in a Q as low as 5. These two antennas may perform equivalently at the resonant frequency, but the second antenna will perform over a bandwidth 3 times as wide as the antenna consisting of a thin conductor.

Antennas for use over much broader frequency ranges are achieved using further techniques. Adjustment of a matching network can, in principle, allow for any antenna to be matched at any frequency. Thus the small loop antenna built into most AM broadcast (medium wave) receivers has a very narrow bandwidth, but is tuned using a parallel capacitance which is adjusted according to the receiver tuning. On the other hand, log-periodic antennas are not resonant at any single frequency but can (in principle) be built to attain similar characteristics (including feedpoint impedance) over any frequency range. These are therefore commonly used (in the form of directional log-periodic dipole arrays) as television antennas.

7.3.8. GAIN: Gain is a parameter which measures the degree of directivity of the antenna's radiation pattern. A high-gain antenna will radiate most of its power in a particular direction, while a low-gain antenna will radiate over a wide angle. The antenna gain, or power gain of an antenna is defined as the ratio of the intensity (power per unit surface area) "I" radiated by the antenna in the direction of its maximum output, at an arbitrary distance, divided by the intensity "I_" radiated at the same distance by a hypothetical isotropic antenna which radiates equal power in all directions. This dimensionless ratio is usually expressed logarithmically in decibels, these units are called decibels-isotropic (dBi)

7.3.9. EFFECTIVE AREA OR APERTURE: The effective area or effective aperture of a receiving antenna expresses the portion of the power of a passing electromagnetic wave which the antenna delivers to its terminals, expressed in terms of an equivalent area. For instance, if a radio wave passing a given location has a flux of 1 pW / m2 (10−12 Watts per square meter) and an antenna has an effective area of 12 m2, then the antenna would deliver 12 pW of RF power to the receiver (30 microvolts RMS at 75 ohms). Since the receiving antenna is not equally sensitive to signals received from all directions, the effective area is a function of the direction to the source.

7.3.10. RADIATION PATTERN: The radiation pattern of an antenna is a plot of the relative field strength of the radio waves emitted by the antenna at different angles in the far-field. It is typically represented by a three-dimensional graph, or polar plots of the horizontal and vertical cross sections. The pattern of an ideal isotropic antenna, which radiates equally in all directions, would look like a sphere. Many nondirectional antennas, such as monopoles and dipoles, emit equal power in all horizontal directions, with the power dropping off at higher and lower angles; this is called an omnidirectional pattern and when plotted looks like a torus or donut.

7.3.11. FIELD REGIONS: The space surrounding an antenna can be divided into three concentric regions: The reactive near-field (also called the inductive near-field), the radiating near-field (Fresnel region) and the far-field (Fraunhofer) regions. These regions are useful to identify the field structure in each, although the transitions between them are gradual, and there are no precise boundaries.

7.3.12. EFFICIENCY: Efficiency of a transmitting antenna is the ratio of power actually radiated (in all directions) to the power absorbed by the antenna terminals. The power supplied to the antenna terminals which is not radiated is converted into heat. This is usually through loss resistance in the antenna's conductors, or loss between the reflector and feed horn of a parabolic antenna

7.3.13. IMPEDANCE MATCHING: Maximum power transfer requires matching the impedance of an antenna system (as seen looking into the transmission line) to the complex conjugate of the impedance of the receiver or transmitter. In the case of a transmitter, however, the desired matching impedance might not exactly correspond to the dynamic output impedance of the transmitter as analyzed as a source impedance but rather the design value (typically 50 Ohms) required for efficient and safe operation of the transmitting circuitry. The intended impedance is normally resistive, but a transmitter (and some receivers) may have limited additional adjustments to cancel a certain amount of reactance, in order to "tweak" the match.

When a transmission line is used in between the antenna and the transmitter (or receiver) one generally would like an antenna system whose impedance is resistive and nearly the same as the characteristic impedance of that transmission line, in addition to matching the impedance that the transmitter (or receiver) expects. The match is sought to minimize the amplitude of standing waves (measured via the standing wave ratio; SWR) that a mismatch raises on the line, and the increase in transmission line losses it entails.

7.4. ANTENNA TYPES: Antennas can be classified by operating principles or by their application. Different authorities placed antennas in narrower or broader categories. Generally these include

- Dipole and monopole antennas
- Array antennas
- Loop antennas
- Aperture antennas
- Travelling wave antennas

7.5. HF ANTENNA: High frequency (HF) is the ITU designation for the range of radio frequency electromagnetic waves (radio waves) between 3 and 30 megahertz (MHz). It is also known as the decameter band or decameter wave as its wavelengths range from one to ten decameters (ten to one hundred meters). Frequencies immediately below HF are denoted medium frequency (MF), while the next band of higher frequencies is known as the very high frequency (VHF) band. The HF band is a major part of the shortwave band of frequencies, so communication at these frequencies is often called shortwave radio. Because radio waves in

this band can be reflected back to Earth by the ionosphere layer in the atmosphere – a method known as "skip" or "skywave" propagation – these frequencies are suitable for long-distance communication across intercontinental distances and for mountainous terrains which prevent line-of-sight communications. The band is used by international shortwave broadcasting stations (3.95–25.82 MHz), aviation communication, government time stations, weather stations, amateur radio and citizens band services, among other uses.

7.5.1. PROPAGATION CHARACTERISTICS: The dominant means of long-distance communication in this band is skywave ("skip") propagation, in which radio waves directed at an angle into the sky refract back to Earth from layers of ionized atoms in the ionosphere. By this method HF radio waves can travel beyond the horizon, around the curve of the Earth, and can be received at intercontinental distances. However, suitability of this portion of the spectrum for such communication varies greatly with a complex combination of factors:

- Sunlight/darkness at site of transmission and reception
- Transmitter/receiver proximity to solar terminator
- Sunspot Cycle
- Polar aurora
- Solar activity
- season

At any point in time, for a given "skip" communication path between two points, the frequencies at which communication is possible are specified by these parameters

- Maximum usable frequency (MUF)
- Lowest usable high frequency (LUF) and a
- Frequency of optimum transmission (FOT)

The maximum usable frequency regularly drops below 10 MHz in darkness during the winter months, while in summer during daylight it can easily surpass 30 MHz. It depends on the angle of incidence of the waves; it is lowest when the waves are directed straight upwards, and is higher with less acute angles. This means that at longer distances, where the waves graze the ionosphere at a very blunt angle, the MUF may be much higher. The lowest usable frequency depends on the absorption in the lower layer of the ionosphere (the D-layer). This absorption is stronger at low frequencies and is also stronger with increased solar activity (for example in daylight); total absorption often occurs at frequencies below 5 MHz during the daytime. The result of these two factors is that the usable spectrum shifts towards the lower frequencies and into the medium frequency (MF) range during winter nights, while on a day in full summer the higher frequencies tend to be more usable, often into the lower VHF range.

When all factors are at their optimum, worldwide communication is possible on HF. At many other times it is possible to make contact across and between continents or oceans. At worst, when a band is "dead", no communication beyond the limited ground wave paths is possible

no matter what powers, antennas or other technologies are brought to bear. When a transcontinental or worldwide path is open on a particular frequency, digital, SSB and Morse code communication is possible using surprisingly low transmission powers, often of the order of milliwatts, provided suitable antennas are in use at both ends and that there is little or no manmade or natural interference. On such an open band, interference originating over a wide area affects many potential users. These issues are significant to military, safety and amature radio users of the HF bands.

USES: The main uses of the high frequency spectrum are:

- Military and governmental communication systems
- Aviation air-to-ground communications
- Amateur radio
- Shortwave international and regional broadcasting
- Maritime sea-to-shore and ship-to-ship services
- Over the horizon radar systems
- Global maritime Distress and safety system (GMDSS) communication
- Citizens Band radio services worldwide (generally 26-28 MHz, the higher portion of the HF band, that behaves more like low-VHF)

7.6. YAGI ANTENA:
A Yagi–Uda antenna or simply Yagi antenna, is a directional antenna consisting of two or more parallel resonant antenna elements in an end-fire array; these elements are most often metal rods acting as half-wave dipoles.Yagi–Uda antennas consist of a single driven element connected to a radio transmitter and/or receiver through a transmission line, and additional "passive radiators" with no electrical connection, usually including one so-called reflector and any number of directors.

Reflector elements (usually only one is used) are slightly longer than the driven dipole and placed behind the driven element, opposite the direction of intended transmission. Directors, on the other hand, are a little shorter and placed in front of the driven element in the intended direction.[4] These parasitic elements are typically off-tuned short-circuited dipole elements, that is, instead of a break at the feedpoint (like the driven element) a solid rod is used. They receive and reradiate the radio waves from the driven element but in a different phase determined by their exact lengths. Their effect is to modify the driven element's radiation pattern. The waves from the multiple elements superpose and interfere to enhance radiation in a single direction, increasing the antenna's gain in that direction.

Also called a beam antenna and parasitic array, the Yagi is very widely used as a directional antenna on the HF, VHF and UHF bands. It has moderate to high gain of up to 20 dBi,depending on the number of elements used, and a front-to-back ratio of up to 20 dB. It radiates linearly polarized radio waves, and can be mounted for either horizontal or vertical polarization. It is relatively lightweight, inexpensive and simple to construct. The bandwidth of a Yagi antenna, the frequency range over which it maintains its gain and feedpoint impedance, is narrow, just a few percent of the center frequency, decreasing for models with higher gain, making it ideal for fixed-frequency applications. The largest and best-known use is as rooftop terrestrial television antennas, but it is also used for point-to-point fixed communication links, in radar antennas, and for long distance shortwave communication by shortwave broadcasting stations and radio amateurs.

7.6.1. DESCRIPTION:
The Yagi–Uda antenna typically consists of a number of parallel thin rod elements, each approximately a half wave in length. Often they are supported on a perpendicular crossbar or "boom" along their centers. Usually there is a single driven element in the center (usually but not always consisting of two rods each connected to one side of the transmission line), and a variable number of parasitic elements, reflectors on one side and optionally one or more directors on the other side. The parasitic elements are not electrically connected to the transmission line, and serve as passive radiators, reradiating the radio waves to modify the radiation pattern. Typical spacings between elements vary from about 1⁄10 to 1⁄4 of a wavelength, depending on the specific design. The directors are slightly shorter than the driven element, while the reflector(s) are slightly longer. The radiation pattern is unidirectional, with the main lobe along the axis perpendicular to the elements in the plane of the elements, off the end with the directors.

Conveniently, the dipole parasitic elements have a node (point of zero RF voltage) at their centre, so they can be attached to a conductive metal support at that point without need of insulation, without disturbing their electrical operation.They are usually bolted or welded to the antenna's central support boom. The most common form of the driven element is one fed at its centre so its two halves must be insulated where the boom supports them.

The gain increases with the number of parasitic elements used. Only one reflector is normally used since the improvement of gain with additional reflectors is small, but more reflectors may be employed for other reasons such as wider bandwidth. Yagis have been built with up to 30–40 directors.

7.6.2. THEORY OF OPERATION: Consider a Yagi–Uda consisting of a reflector, driven element and a single director as shown here. The driven element is typically a $1/2\lambda$ dipole or folded dipole and is the only member of the structure that is directly excited (electrically connected to the feedline). All the other elements are considered parasitic. That is, they reradiate power which they receive from the driven element. They also interact with each other, but this mutual coupling is neglected in the following simplified explanation, which applies to far-field conditions.

Consider a parasitic element to be a normal dipole element of finite diameter fed at its centre, with a short circuit across its feed point. The principal part of the current in a loaded receiving antenna is distributed as in a center-driven antenna. It is proportional to the effective length of the antenna and is in phase with the incident electric field if the passive dipole is excited exactly at its resonance frequency. Now we imagine the current as the source of a power wave at the (short-circuited) port of the antenna. As is well known in transmission line theory, a short circuit reflects the incident voltage 180 degrees out of phase. So one could as well model the operation of the parasitic element as the superposition of a dipole element receiving power and sending it down a transmission line to a matched load, and a transmitter sending the same amount of power up the transmission line back toward the antenna element. If the transmitted voltage wave were 180 degrees out of phase with the received wave at that point, the superposition of the two voltage waves would give zero voltage, equivalent to shorting out the dipole at the feedpoint (making it a solid element, as it is). However, the current of the backward wave is in phase with the current of the incident wave. This current drives the reradiation of the (passive) dipole element. At some distance, the reradiated electric field is described by the far-field component of the radiation field of a dipole antenna. Its phase includes the propagation delay (relating to the current) and an additional 90 degrees lagging phase offset. Thus, the reradiated field may be thought as having a 90 degrees lagging phase with respect to the incident field.

Parasitic elements involved in Yagi–Uda antennas are not exactly resonant but are somewhat shorter (or longer) than $1/2\lambda$ so that the phase of the element's current is modified with respect to its excitation from the driven element. The so-called reflector element, being longer than $1/2\lambda$, has an inductive reactance, which means the phase of its current lags the phase of the open-circuit voltage that would be induced by the received field. The phase delay is thus larger than 90 degrees and, if the reflector element is made sufficiently long, the phase delay may be imagined to approach 180 degrees, so that the incident wave and the wave reemitted by the reflector interfere destructively in the forward direction (i.e. looking from the driven element towards the passive element). The director element, on the other hand, being shorter than $1/2\lambda$, has a capacitive reactance with the voltage phase lagging that of the current. The phase delay is thus smaller than 90 degrees and, if the director element is made sufficiently short, the phase delay may be imagined to approach zero and the incident wave and the wave reemitted by the reflector interfere constructively in the forward direction.

Interference also occurs in the backward direction. This interference is influenced by the distance between the driven and the passive element, because the propagation delays of the incident wave (from the driven element to the passive element) and of the reradiated wave (from the passive element back to the driven element) have to be taken into account. To illustrate the effect, we assume zero and 180 degrees phase delay for the reemission of director and reflector, respectively, and assume a distance of a quarter wavelength between the driven and the passive element. Under these conditions the wave reemitted by the director interferes destructively with the wave emitted by the driven element in the backward direction (away from the passive element), and the wave reemitted by the reflector interferes constructively.

In reality, the phase delay of passive dipole elements does not reach the extreme values of zero and 180 degrees. Thus, the elements are given the correct lengths and spacings so that the radio waves radiated by the driven element and those re-radiated by the parasitic elements all arrive at the front of the antenna in-phase, so they superpose and add, increasing signal strength in the forward direction. In other words, the crest of the forward wave from the reflector element reaches the driven element just as the crest of the wave is emitted from that element. These waves reach the first director element just as the crest of the wave is emitted from that element, and so on. The waves in the reverse direction interfere destructively, cancelling out, so the signal strength radiated in the reverse direction is small. Thus the antenna radiates a unidirectional beam of radio waves from the front (director end) of the antenna.

7.7. LOOP ANTENNA: A loop antenna is a radio antenna consisting of a loop or coil of wire, tubing, or other electrical conductor, that is usually fed by a balanced source or feeding a balanced load. Loop antennas may be in the shape of a circle, a square or any other closed geometric shape that allows the total perimeter to be slightly more than one wavelength. The most popular shape in amateur radio is the quad antenna or "quad", a self-resonant loop in a square shape so that it can be constructed of wire strung across a supporting '×' shaped frame. There may be one or more additional loops stacked parallel to the first as parasitic elements or driven elements, creating an antenna array which is unidirectional with increased gain.

7.7.1. RADIATION PATTERN: The radiation pattern of a first-resonance loop antenna peaks at right angles to the plane of the loop. At the lower shortwave frequencies a full loop is physically quite large, and can practically only be installed "lying flat", with the plane of the loop horizontal to the ground, consisting of wires supported at the same height by masts along its perimeter. This results in horizontally-polarized radiation peaking toward the vertical which is generally less desired.

Above about 10 MHz the loop is approximately 10 meters in diameter, and it becomes more practical for the loop to be mounted "standing up" – that is with the plane of the loop vertical, in order to direct its main beam towards the horizon. If small enough, it may be attached to an antenna rotator in order to rotate that direction as desired. Compared to a dipole or folded dipole, a vertical large loop wastes less radiated power toward the sky or ground, resulting in about 1.5 dB higher gain in the two favored horizontal directions.

7.8. SATELLITE COMMUNICATION: A communications satellite is an artificial satellite that relays and amplifies radio telecommunication signals via a transponder; it creates a communication channel between a source transmitter and a receiver at different locations on Earth. Communications satellites are used for television, telephone, radio, internet, and military applications. As of 1 January 2021, there are 2,224 communications satellites in Earth orbit.[2] Most communications satellites are in geostationary orbit 22,300 miles (35,900 km) above the equator, so that the satellite appears stationary at the same point in the sky; therefore the satellite dish antennas of ground stations can be aimed permanently at that spot and do not have to move to track the satellite.

The high frequency radio waves used for telecommunications links travel by line of sight and so are obstructed by the curve of the Earth. The purpose of communications satellites is to relay the signal around the curve of the Earth allowing communication between widely separated geographical points. Communications satellites use a wide range of radio and microwave frequencies. To avoid signal interference, international organizations have regulations for which frequency ranges or "bands" certain organizations are allowed to use. This allocation of bands minimizes the risk of signal interference.

7.8.1. SATELLITE ORBITS: Communications satellites usually have one of three primary types of orbit, while other orbital classifications are used to further specify orbital details. MEO and LEO are non-geostationary orbit (NGSO).

Geostationary satellites have a geostationary orbit (GEO), which is 22,236 miles (35,785 km) from Earth's surface. This orbit has the special characteristic that the apparent position of the satellite in the sky when viewed by a ground observer does not change, the satellite appears to "stand still" in the sky. This is because the satellite's orbital period is the same as the rotation rate of the Earth. The advantage of this orbit is that ground antennas do not have to track the satellite across the sky, they can be fixed to point at the location in the sky the satellite appears.

Medium Earth orbit (MEO) satellites are closer to Earth. Orbital altitudes range from 2,000 to 36,000 kilometres (1,200 to 22,400 mi) above Earth.

The region below medium orbits is referred to as low Earth orbit (LEO), and is about 160 to 2,000 kilometres (99 to 1,243 mi) above Earth.

As satellites in MEO and LEO orbit the Earth faster, they do not remain visible in the sky to a fixed point on Earth continually like a geostationary satellite, but appear to a ground observer to cross the sky and "set" when they go behind the Earth beyond the visible horizon. Therefore, to provide continuous communications capability with these lower orbits requires a larger number of satellites, so that one of these satellites will always be visible in the sky for transmission of communication signals. However, due to their relatively small distance to the Earth their signals are stronger.

7.8.2. PARABOLIC REFLECTOR: A parabolic (or paraboloid or paraboloidal) reflector (or dish or mirror) is a reflective surface used to collect or project energy such as light, sound, or radio waves. Its shape is part of a circular paraboloid, that is, the surface generated by a parabola revolving around its axis. The parabolic reflector transforms an incoming plane wave travelling along the axis into a spherical wave converging toward the focus. Conversely, a spherical wave generated by a point source placed in the focus is reflected into a plane wave propagating as a collimated beam along the axis.

Parabolic reflectors are used to collect energy from a distant source (for example sound waves or incoming star light). Since the principles of reflection are reversible, parabolic reflectors can also be used to collimate radiation from an isotropic source into a parallel beam. In optics, parabolic mirrors are used to gather light in reflecting telescopes and solar furnaces, and project a beam of light in flashlights, searchlights, stage spotlights, and car headlights. In radio, parabolic antennas are used to radiate a narrow beam of radio waves for point-to-point communications in satellite dishes and microwave relay stations, and to locate aircraft, ships, and vehicles in radar sets. In acoustics, parabolic microphones are used to record faraway sounds such as bird calls, in sports reporting, and to eavesdrop on private conversations in espionage and law enforcement.

The parabolic reflector functions due to the geometric properties of the paraboloidal shape: any incoming ray that is parallel to the axis of the dish will be reflected to a central point, or "focus". Because many types of energy can be reflected in this way, parabolic reflectors can be used to collect and concentrate energy entering the reflector at a particular angle. Similarly, energy radiating from the focus to the dish can be transmitted outward in a beam that is parallel to the axis of the dish.

In contrast with spherical reflector, which suffers from a spherical aberration that becomes stronger as the ratio of the beam diameter to the focal distance becomes larger, parabolic reflectors can be made to accommodate beams of any width. However, if the incoming beam makes a non-zero angle with the axis (or if the emitting point source is not placed in the focus), parabolic reflectors suffer from an aberration called coma. This is primarily of interest in telescopes because most other applications do not require sharp resolution off the axis of the parabola.

The precision to which a parabolic dish must be made in order to focus energy well depends on the wavelength of the energy. If the dish is wrong by a quarter of a wavelength, then the reflected energy will be wrong by a half wavelength, which means that it will interfere destructively with energy that has been reflected properly from another part of the dish. To prevent this, the dish must be made correctly to within about 1/20 of a wavelength. The wavelength range of visible light is between about 400 and 700 nanometres (nm), so in order to focus all visible light well, a reflector must be correct to within about 20 nm. For comparison, the diameter of a human hair is usually about 50,000 nm, so the required accuracy for a reflector to focus visible light is about 2500 times less than the diameter of a hair. For example, the flaw in the Hubble Space Telescope mirror (too flat by about 2,200 nm at its perimeter) caused severe spherical aberration until corrected with COSTAR.

7.9. VESTIGIAL TRANSMISSION: Vestigial sideband (VSB) is a type of amplitude modulation (AM) technique (sometimes called VSB-AM) that encodes data by varying the amplitude of a single carrier frequency. Portions of one of the redundant sidebands are removed to form a vestigial sideband signal - so-called because a vestige of the sideband remains.

In AM, the carrier itself does not fluctuate in amplitude. Instead, the modulating data appears in the form of signal components at frequencies slightly higher and lower than that of the carrier. These components are called sidebands. The lower sideband (LSB) appears at frequencies below the carrier frequency; the upper sideband (USB) appears at frequencies above the carrier frequency. The actual information is transmitted in the sidebands, rather than the carrier; both sidebands carry the same information. Because LSB and USB are essentially mirror images of each other, one can be discarded or used for a second channel or for diagnostic purposes.

VSB transmission is similar to single-sideband (SSB) transmission, in which one of the sidebands is completely removed. In VSB transmission, however, the second sideband is not completely removed, but is filtered to remove all but the desired range of frequencies.

7.10. TV CAMERA TUBES: Video camera tubes were devices based on the cathode ray tube that were used in television cameras to capture television images prior to the introduction of charge-coupled device (CCD) image sensors in the 1980s. Several different types of tubes were in use from the early 1930s, and as late as the 1990s.

In these tubes, the cathode ray was scanned across an image of the scene to be broadcast. The resultant current was dependent on the brightness of the image on the target.

7.10.1. CATHODE RAY TUBE: Any vacuum tube which operates using a focused beam of electrons, originally called cathode rays, is known as a cathode ray tube (CRT). These are usually seen as display devices as used in older (i.e., non-flat panel) television receivers and computer displays. The camera pickup tubes described in this article are also CRTs, but they display no image.

7.10.2. IMAGE DISSECTOR: An image dissector is a camera tube that creates an "electron image" of a scene from photocathode emissions (electrons) which pass through a scanning aperture to an anode, which serves as an electron detector.

The optical system of the image dissector focuses an image onto a photocathode mounted inside a high vacuum. As light strikes the photocathode, electrons are emitted in proportion to the intensity of the light (see photoelectric effect). The entire electron image is deflected and a scanning aperture permits only those electrons emanating from a very small area of the photocathode to be captured by the detector at any given time. The output from the detector is an electric current whose magnitude is a measure of the brightness of the corresponding area of the image. The electron image is periodically deflected horizontally and vertically ("raster scanning") such that the entire image is read by the detector many times per second, producing an electrical signal that can be conveyed to a display device, such as a CRT monitor, to reproduce the image.

The image dissector has no "charge storage" characteristic; the vast majority of electrons emitted by the photocathode are excluded by the scanning aperture, and thus wasted rather than being stored on a photo-sensitive target, as in the iconoscope or image orthicon (see below), which largely accounts for its low light sensitivity.

7.11. IMAGE ORTHICON:

An image orthicon camera can take television pictures by candlelight because of the more ordered light-sensitive area and the presence of an electron multiplier at the base of the tube, which operated as a high-efficiency amplifier. It also has a logarithmic light sensitivity curve similar to the human eye. However, it tends to flare in bright light, causing a dark halo to be seen around the object; this anomaly was referred to as blooming in the broadcast industry when image orthicon tubes were in operation Image orthicons were used extensively in the early color television cameras, where the increased sensitivity of the tube was essential to overcome the very inefficient optical system of the camera.
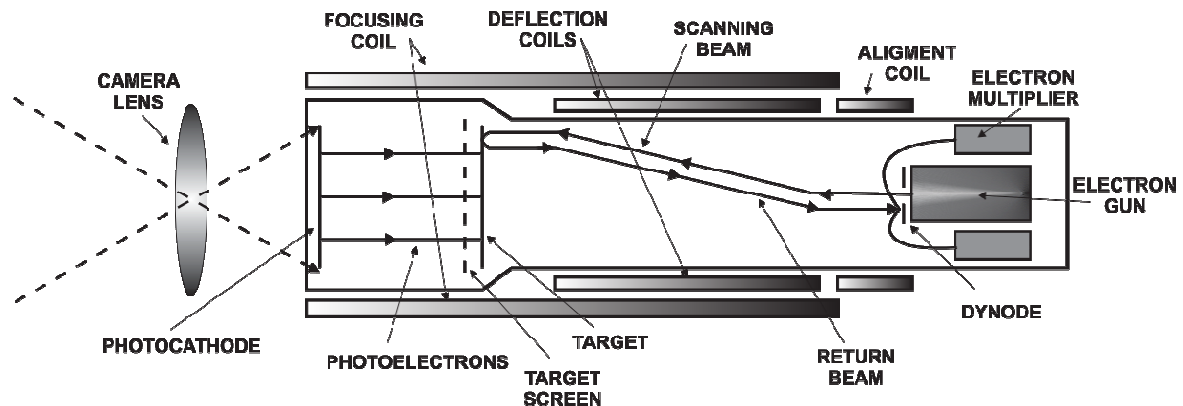

Fig. 7.1.: IMAGE ORTHICON

An image orthicon consists of three parts: a photocathode with an image store (target), a scanner that reads this image (an electron gun), and a multistage electron multiplier.

In the image store, light falls upon the photocathode which is a photosensitive plate at a very negative potential (approx. -600 V), and is converted into an electron image (a principle borrowed from the image dissector). This electron rain is then accelerated towards the target (a very thin glass plate acting as a semi-isolator) at ground potential (0 V), and passes through a very fine wire mesh (nearly 200 wires per cm), very near (a few hundredths of a cm) and parallel to the target, acting as a screen grid at a slightly positive voltage (approx +2 V). Once the image electrons reach the target, they cause a splash of electrons by the effect of secondary emission. On average, each image electron ejects several splash electrons (thus adding amplification by secondary emission), and these excess electrons are soaked up by the positive mesh effectively removing electrons from the target and causing a positive charge on it in relation to the incident light in the photocathode. The result is an image painted in positive charge, with the brightest portions having the largest positive charge.

A sharply focused beam of electrons (a cathode ray) is generated by the electron gun at ground potential and accelerated by the anode (the first dynode of the electron multiplier) around the gun at a high positive voltage (approx. +1500 V). Once it exits the electron gun, its inertia makes the beam move away from the dynode towards the back side of the target. At this point the electrons lose speed and get deflected by the horizontal and vertical deflection coils, effectively scanning the target. Thanks to the axial magnetic field of the focusing coil, this deflection is not in a straight line, thus when the electrons reach the target they do so perpendicularly avoiding a sideways component. The target is nearly at ground potential with a small positive charge, thus when the electrons reach the target at low speed they are absorbed without ejecting more electrons. This adds negative charge to the positive charge until the region being scanned reaches some threshold negative charge, at which point the scanning electrons are reflected by the negative potential rather than absorbed (in this process the target recovers the electrons needed for the next scan). These reflected electrons return down the cathode ray tube toward the first dynode of the electron multiplier surrounding the electron gun which is at high potential. The number of reflected electrons is a linear measure of the target's original positive charge, which, in turn, is a measure of brightness.

7.12. VIDICON:

A vidicon tube is a video camera tube design in which the target material is a photoconductor. The vidicon was developed in the 1950s at RCA by P. K. Weimer, S. V. Forgue and R. R. Goodrich as a simple alternative to the structurally and electrically complex image orthicon. While the initial photoconductor used was selenium, other targets including silicon diode arrays have been used.

The vidicon is a storage-type camera tube in which a charge-density pattern is formed by the imaged scene radiation on a photoconductive surface which is then scanned by a beam of low-velocity electrons. The fluctuating voltage coupled out to a video amplifier can be used to reproduce the scene being imaged. The electrical charge produced by an image will remain in the face plate until it is scanned or until the charge dissipates. By using a pyroelectric material such as triglycine sulfate (TGS) as the target, a vidicon sensitive over a broad portion of the infrared spectrum is possible.
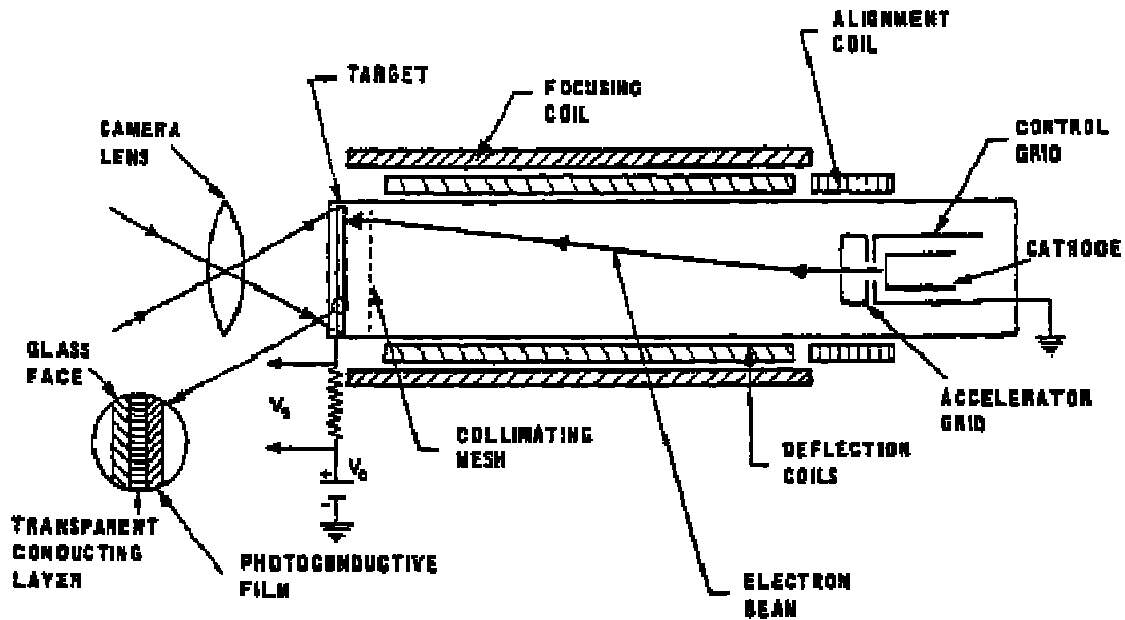
FIG. 7.2.: VIDICON

All vidicon and similar tubes are prone to image lag, better known as ghosting, smearing, burn-in, comet tails, luma trails and luminance blooming. Image lag is visible as noticeable (usually white or colored) trails that appear after a bright object (such as a light or reflection) has moved, leaving a trail that eventually fades into the image. The trail itself does not move, rather it progressively fades as time passes, so areas that were exposed first fade before areas that were later exposed fade. It cannot be avoided or eliminated, as it is inherent to the technology. To what degree the image generated by the vidicon is affected will depend on the properties of the target material used on the vidicon, and the capacitance of the target material (known as the storage effect) as well as the resistance of the electron beam used to scan the target. The higher the capacitance of the target, the higher the charge it can hold and the longer it will take for the trail to disappear. The remmanant charges on the target eventually dissipate making the trail disappear.

7.13. TV TRANSMITTER: A television transmitter is a transmitter that is used for terrestrial (over-the-air) television broadcasting. It is an electronic device that radiates radio waves that carry a video signal representing moving images, along with a synchronized audio channel, which is received by television receivers ('televisions' or 'TVs') belonging to a public audience, which display the image on a screen. A television transmitter, together with the broadcast studio which originates the content, is called a television station. Television transmitters must be licensed by governments, and are restricted to a certain frequency channel and power level. They transmit on frequency channels in the VHF and UHF bands. Since radio waves of these frequencies travel by line of sight, they are limited by the horizon to reception distances of 40–60 miles depending on the height of transmitter station.

Television transmitters use one of two different technologies: analog, in which the picture and sound are transmitted by analog signals modulated onto the radio carrier wave, and digital in which the picture and sound are transmitted by digital signals. The original television technology, analog television, began to be replaced in a transition beginning in 2006 in many countries with digital television (DTV) systems. These transmit pictures in a new format called HDTV (high-definition television) which has higher resolution and a wider screen aspect ratio than analog. DTV makes more efficient use of scarce radio spectrum bandwidth, as several DTV channels can be transmitted in the same bandwidth as a single analog channel. In both analog and digital television, different countries use several incompatible modulation standards to add the video and audio signals to the radio carrier wave.

The principles of primarily analog systems are summarized as they are typically more complex than digital transmitters due to the multiplexing of VSB and FM modulation stages.

7.14 SUMMARY

In this unit, you have studied about basic function of antenna, different types of antenna, and characteristics of antenna. All type of communication discussed. You learnt about image orthicon and Videocon.

7.15 REFERENCES

1. Digital Logic and Computer Design by M. Morris Mano, Pearson.

2. Modern Digital Electronics by R. P. Jain, TMH, 2010.

7.16 SUGGESTED READINGS

1. Digital Fundamentals,10th Ed, Floyd T L, Prentice Hall, 2009.
2. Online tutorials.
3. Different online sites.
4. You tube
5. NPTL site material

7.17 TERMINAL QUESTIONS

7.17.1 Short Answer type

1. What are basic properties of antenna?
2. What do you understand by high frequency antenna?
3. What do you understand by high Yagi antenna?
5. Write short note on
a) Videocon
b) Image orthicon

UNIT 8   SATELLITE COMMUNICATION

Structure

8.1 Introduction
8.2 Orbits and Orbital Mechanics
8.3 Path Loss Calculations
8.4 Satellite Link Description
8.5 Satellite Link Calculations
8.6 Transponders and Effects of Nonlinearity of Transponder
8.7 Multiple Access Techniques in Satellite Communication
    8.7.1 Frequency Division Multiple Access
    8.7.2 Time Division Multiple Access
8.8 Telemetry, Tracking, Command and Monitoring System
4.9 Summary
4.10 References and Suggested Readings
4.11 Terminal Questions and Answers

8.1 Introduction

Satellite Communication is most effective means of transmitting information over a vast geographical area as well as for those locations where conventional communication systems are not accessible. The growth of satellite applications is due to the result of research combining communication and space technologies with the objective to achieve increasing ranges and capacities at lowest possible costs. Since the first artificial satellite named as Sputnik, launched by erstwhile USSR (now Russia) in 1957, satellite communication has come to the age when international telecommunication, global broadcasting services, meteorological and remote sensing applications, and military intelligence are just ,unthinkable without it.

The entire configuration of satellite communication system is composed of three segments namely, (i) Space segment – which comprises satellite as a space ship, (ii) Control segment- which comprises control system to maintain orbital and attitudinal parameters of satellite known as housekeeping and also managing services if shared by number of users, and (iii) Ground segment- which comprises of earth stations establishing links with satellite. For understanding satellite communication we require knowledge of physics behind its orbital mechanism and it is already known as Kepler's laws of planetary motion. Apart from this, we shall explore communication system established through satellite link and the control operation of satellite to keep it stable in the space.

Learning Objectives

After studying this unit, you should be able to-

- ➢ Understand satellite orbits and orbital mechanics behind stability of satellite in space
- ➢ Calculate loss of strength in a line-of-sight path
- ➢ Understand satellite link description
- ➢ Calculate carrier-to-noise ratio for a satellite link
- ➢ Understand transponders functioning and effects of its nonlinearity of Transponder
- ➢ Understand multiple access techniques in satellite communication
- ➢ Understand role of Telemetry, Tracking, Command and Monitoring System in maintaining satellite services

8.2 Orbits and Orbital Mechanics

Satellites are placed in space above the earth and to stay there in stable position it must continuously move and traverse a path which is called its orbit. The orbit in space is governed by two forces it experiences first is the inward centripetal force determined by the Newton's law of gravitation and second one is the centrifugal force governed by Newton's third law of motion, which acts outward. These two forces acting on an orbiting body around the earth are shown in figure 8.1
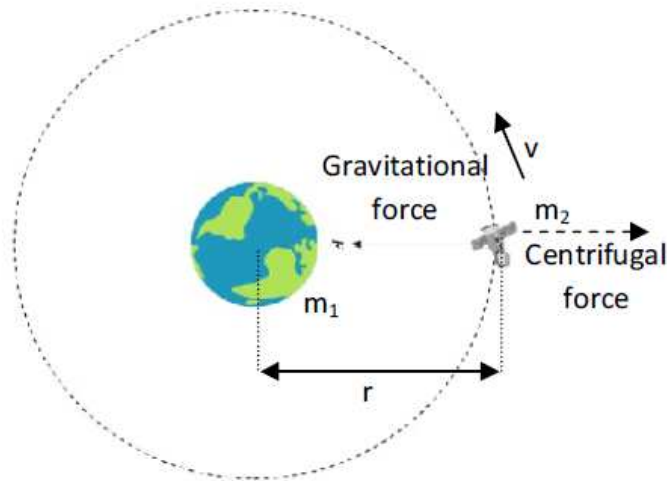

Figure 8.1 Gravitational force and the centrifugal force acting on bodies orbiting Erath

The gravitational force which is centripetal force acting inward, is given by

$$F_{in} = \frac{Gm_1 m_2}{r^2}$$

(8.1)

and the centrifugal force is given by

$$F_{out} = \frac{m_2 v^2}{r}$$

(8.2)

Equating these two forces, we have

$$\frac{Gm_1 m_2}{r^2} = \frac{m_2 v^2}{r} \quad \text{which yields} \quad v = \sqrt{\frac{Gm_1}{r}} = \sqrt{\frac{\mu}{r}}$$

(8.3)

where G is universal gravitational constant = 6.67 x 10^{-11} Nm^2 /kg^2 , m_1 is the mass of the Earth; m_2 the mass of the satellite; $\mu = Gm_1$ = 3.986013 $\times$ 10^5 km^3/s^2 = 3.986013 $\times$ 10^{14} Nm^2/kg. μ is also known as Kepler's constant. The orbital period in such a case can be computed from

$$T = \frac{2\pi r^{\frac{3}{2}}}{\sqrt{\mu}}$$

(8.4)

In the case of an elliptical orbit, the forces governing the motion of the satellite are the same. The velocity at any point on an elliptical orbit at a distance d from the centre of the Earth is given by the formula

$$v = \sqrt{\mu\left(\frac{2}{d} - \frac{1}{a}\right)}$$

(8.5)

where a is the semi-major axis of the elliptical orbit. The orbital period in the case of an circular orbit is also given by same equation with semi-major axis replaced by orbiting radius from the center of the earth, R

$$T = \frac{2\pi R^{\frac{3}{2}}}{\sqrt{\mu}}$$

(8.6)

All the relations between time period, distance and velocity of a satellite are obtainable from the three laws of planetary motion given by Kepler.

Based on the distance of a satellite from the surface of the earth, satellite orbits are mainly classified as, low earth orbit (LEO), medium earth orbit (MEO), and geosynchronous earth orbit (GEO). If GEO is in equatorial plane i.e. having 0° inclination with the equator, it is called geostationary orbit. Following table gives the orbital height, orbital velocity, and orbital time period of various orbits used in satellite communication.

Table 1: Different orbits

Orbit	Height (km)	Velocity (km/s)	Time period (h,m,s)
GEO	35786.03	3.0747	23,56,4
MEO	10255	4.8954	5,55,48
LEO-I	1469	7.1272	1,55,18
LEO-II	780	7.4624	1,40,27

Example 8.1: A satellite is orbiting in an uniform circular orbit at a distance of 630 km from the surface of earth. Assuming the radius of earth equal to 6370 km, find the velocity of satellite in the orbit.

Solution: Total orbital radius of satellite = 6370+630 = 7000 km = 7000000 m = 7x 10^6 m.

The velocity of satellite in the orbit $v = \sqrt{\frac{\mu}{r}} = \sqrt{\frac{3.986013 \times 10^{14}}{7 \times 10^6}}$ = 7.54 km/s

Example 8.2: Find out the orbital time period of the satellite given in example 8.1

Solution: Orbital time period is given by $T = \dfrac{2\pi R^{\frac{3}{2}}}{\sqrt{\mu}} = \dfrac{2\pi (7 \times 10^6)^{\frac{3}{2}}}{\sqrt{3.986013 \times 10^{14}}} = 5829$ seconds

or 1 hour 37 minutes 9 seconds.

To specify the location of a satellite in its orbit around the earth we require six parameters which are called **Orbital elements.** They are known as: semi-major axis, eccentricity, time of passage through perigee, right ascension of ascending node, inclination, and argument of perigee. These six orbital elements are shown in figure 8.2.
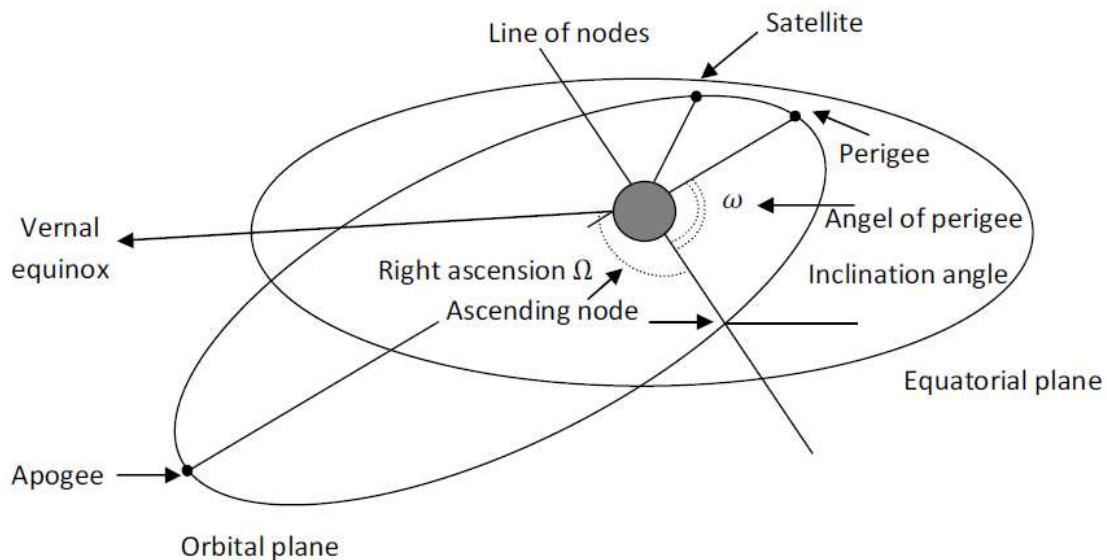

Fig. 8.2: Orbital Elements

Here, as shown in the figure 8.2, the orbit of the satellite is elliptical with some eccentricity e and orbital plane is inclined with equatorial plane at some angle i. The center of the earth coincides with one of the two foci of ellipse and thus the distance of satellite will be maximum and minimum at two fixed points known as apogee, r_a and perigee, r_p respectively. The line joining apogee and perigee passes through center of the earth is also major axis of ellipse and known as line of apsides. In fact, all the parameters of ellipse can be obtained from theory of conic sections. Following are few relations between various parameters of an ellipse which may require while exploring elliptical orbits. If a and b

$r_a + r_p = 2a$, $e = \dfrac{r_a - r_p}{r_a + r_p}$, $e = \dfrac{\sqrt{a^2 - b^2}}{a}$

A satellite moving in an inclined orbit cuts the equatorial plane twice, once when it emerges out of equatorial plane i.e. ascends and other time when it submerges into equatorial plane i.e. descends. These two points on orbit are called ascending node and descending nodes respectively. The line joining these two points is called line of nodes. The position of these nodes cannot be fixed in a latitude-longitude coordinate system as earth itself is spinning on

its own axis, an imaginary line is taken as reference which is the line drawn from the center of the earth to a specific direction in space called vernal equinox . The angle measured from this line to the ascending node in equatorial plane is called right ascension of ascending node, Ω. Another angle measured in orbital plane known as argument of perigee, ω is the angle formed from ascending node to perigee. The time of passage through perigee, t_p is the time when satellite is at perigee i.e. at the nearest distance from the earth.

Over the surface of the earth, satellite is located in terms of sub satellite point (SSP) which is the location cut by the line joining the satellite and center of the earth. It is expressed physically in degrees latitude and longitude of that point. However an earth station requires a pair of look angles for a particular satellite for establishing a link with it. These look angles are known as azimuth and elevation angles. For communicating with a satellite a line-of-sight (LOS) visibility is essential and direction of transmitting or receiving antenna has to be in the direction of satellite which is determined by look angles. The azimuth angle is defined as the angle formed in the local horizon from the direction of true north to the direction of satellite looking for it horizontally. The elevation angle is measured in the plane perpendicular to local horizon in the direction of satellite looking for it vertically.

Satellite and earth stations communicate with each other using directional antennas provided at both the ends. Just like look angles are important for earth stations to look towards satellite, attitude of the satellite is equally important to maintain so the direction of its antenna towards earth station is also maintained. Satellite experiences many perturbations in the space and over a period of time its orbit and attitude may drift from the set position. Therefore, all satellites are continuously monitored for their health and position from the controlling stations. This process is called housekeeping which is discussed later on.

8.3 Path Loss Calculations

Path loss is the total loss in signal strength while signal propagates from earth station to satellite or vice versa. The loss depends on the path characteristics and loss mechanism involved during the propagation phenomenon. In fact, in the absence of any other loss mechanism involved, the signal attenuates substantially due to inherent loss mechanism involved in transmission between two distant points and this loss is referred as free-space loss. So the total path loss is always a sum of free-space loss and other losses.

Free space loss can be calculated as

$$L_{FS} = \left(\frac{4\pi f d}{c}\right)^2 \qquad = \qquad 20 \qquad \log \qquad \left(\frac{4\pi f d}{c}\right) \qquad \text{dB.}$$
(8.7)

Where f is the signal frequency, d is distance between transmitter and receiver and c is the velocity of electromagnetic wave in free-space $\approx$ velocity of light. If c is taken in km/s and f in MHz then free-space loss can be computed from

$$L_{FS} \quad = \quad 32.4 \quad + \quad 20 \quad \log \quad d \quad + \quad 20 \quad \log \quad f \quad dB$$
(8.8)

The sources of **other losses** can be gaseous absorption, rain induced attenuation, signal fading, tracking loss, coupling losses etc. They are calculated or estimated separately.

Example 8.3: Find out the uplink and downlink path loss for geostationary satellites operating in 6/4 GHz and 14/12 GHz bands. Assume geostationary distance from surface of the earth = 36000 km

Solution: Uplink path loss at 6 GHz = 32.4 + 20 log 36000 + 20 log 6000 = 199.1 dB

Downlink path loss at 4 GHz = 32.4 + 20 log 36000 + 20 log 4000 = 195.6 dB

Uplink path loss at 14 GHz = 32.4 + 20 log 36000 + 20 log 14000 = 206.5 dB

Downlink path loss at 12 GHz = 32.4 + 20 log 36000 + 20 log 12000 = 205.1 dB

8.4 Satellite Link Description

Consider a basic satellite link shown in Fig. 8.3. The complete link comprises of two separate microwave links, the uplink connecting transmitting earth station to the satellite and the downlink connecting satellite to the receiving earth station. The basic performance measure of any communication system link is carrier-to-noise ratio, denoted as (C/N) where C is carrier power and N is noise power. However, actual performance measure of the link will include the interferences present in the system, if any, and in such cases it will be necessary to find carrier-to-noise-plus-interference ratio. Noise is generated in the system due to thermal noise and Noise power is calculated as

$N=kTB$
(8.9)

where k is Boltzmann constant = 1.38 X 10^{-23} J/K, T is the Noise temperature and B is the noise bandwidth of receiver. The transmitting earth station transmits the carrier $s(t)$ whose power is simply the effective isotropically radiated power (EIRP) of the carrier given by

EIRP = $P_T G_T$
(8.10)

where P_T = carrier power at antenna feed and G_T = transmit antenna gain. For basic link calculation we simply assume that the transmission is carried under clear-sky conditions and that only loss the carrier $s(t)$ suffers is the uplink free space loss, and no other loss mechanism is involved.
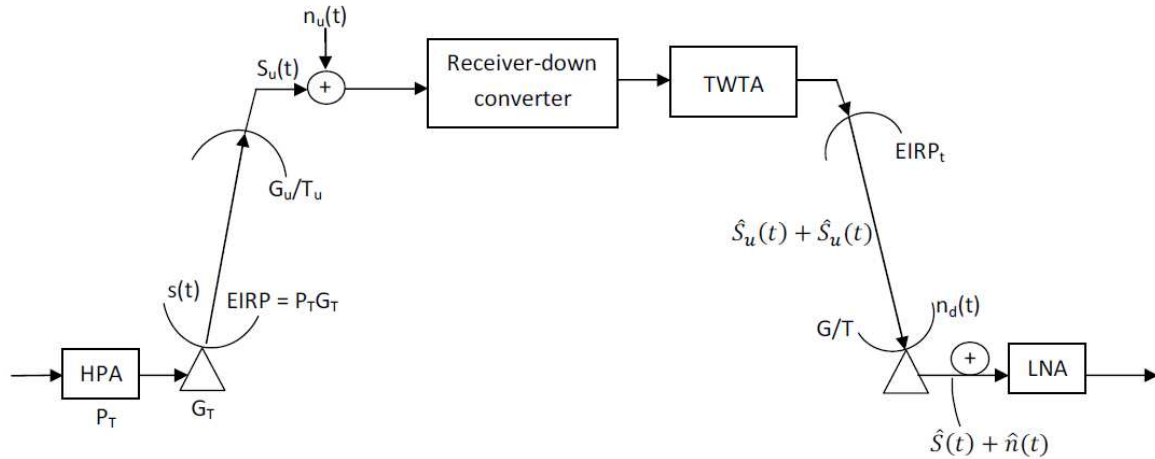
Figure 8.3: Basic satellite link.

Before moving to get the expressions for uplink and downlink $(C/N)_{U \text{ or } D}$, and finally to get the total link $(C/N)_T$ let us find the power received at the receiving station in any microwave link. Using the Friis transmission equation as given below we can get the power receive

$$\left(\frac{\lambda^2 G_R}{4\pi}\right) = \frac{P_T G_T G_R}{\left(4\pi d/\lambda\right)^2} = \frac{P_T G_T G_R}{L_P} = \frac{EIRP_T \, G_R}{L_P}.$$

(8.11)

In dB value notation the above equation can be rewritten as

$$P_R(in \, dBW) = EIRP_T \, (in \, dBW) \mid G_R \, (in \, dB) \quad L_P \, (in \, dB)$$
(8.12)

If other losses are also included the above equation becomes

$$P_R(in \, dBW) = EIRP_T \, (in \, dBW) + G_R \, (in \, dB) - L_P \, (in \, dB) - L_{other} \, (in \, dB)$$
(8.13)

It is convenient to use dB values while writing a equation with ratio terms as it gets converted to addition and subtraction only.

8.5 Satellite Link Calculations

Now we are ready with our understanding of basic link power equation and can proceed to write (C/N) equation for uplink.

$$\left(\frac{C}{N}\right)_u = \frac{C_u}{N_u} = \frac{(EIRP)}{L_{other}}\left(\frac{c}{4\pi f_u d_u}\right)^2 \left(\frac{G_u}{T_u}\right)\left(\frac{1}{kB}\right) = \left(\frac{EIRP}{L_u L_{other}}\right)\left(\frac{G_u}{T_u}\right)\left(\frac{1}{kB}\right)$$
(8.14)

Similarly we can write the downlink equation also and we shall use the subscript '*d*' to indicate that. In dB notation the uplink or downlink (*C/N*) equation can be written as

$$\left(\frac{C}{N}\right)_{u,d} = EIRP + \left(\frac{G}{T}\right) - L_p - L_{other} - k - B$$

(8.15)

where all values are in dB with appropriate units. In this equation (G/T) ratio is treated as a separate parameter defined as figure-of merit of receiver which is the ratio of antenna gain to noise temperature of receiver. This equation is called as link budget equation and it gives a trade-off between transmitted EIRP and G/T ratio of receiver.

Note that in free space $EIRP/4\pi d_u^2$ is simply the carrier *power flux density* (W/m^2) at the satellite:

$$\Omega = \frac{EIRP}{4\pi d_u^2}$$

(8.16)

Also, the term $4\pi d_u^2/c^2$ is simply the gain of an ideal antenna whose aperture area is 1 m^2 and when aperture efficiency, $\eta = 1 \ and \ A = 1$ m^2:

$$G_{1m^2} = \frac{4\pi d_u^2}{c^2}$$

(8.17)

Substituting (4.16) into (8.14) yields

$$\left(\frac{C}{N}\right)_u = \Omega \left(\frac{c^2}{4\pi d_u^2}\right) \left(\frac{G_u}{T_u}\right) \left(\frac{1}{kB}\right) \left(\frac{1}{L_{other}}\right)$$

(8.18)

and using (8.17) we can also write (8.18) as

$$\left(\frac{C}{N}\right)_u = \Omega \left(\frac{1}{G_{1m^2}}\right) \left(\frac{G_u}{T_u}\right) \left(\frac{1}{kB}\right) \left(\frac{1}{L_{other}}\right)$$

(8.19)

Using dB notations the $\left(\frac{C}{N}\right)_u$ can be expressed as

$$\left(\frac{C}{N}\right)_u = \Omega + (G/T)_u - G_{1m^2} - L_{other} - k - B$$

(8.20)

If we compare equation (8.15) and (8.20) we find that in case if we consider power flux density instead of EIRP to refer to power level, the path loss does not come into our calculations. The reason is simple but important to be noted that, EIRP is the measure of power level radiated at the transmitter end and hence to estimate it at receiver located at a

distance we need to find out the path loss factor. However, in case of power level defined in flux density is a measure of power density at a distance and hence already involves the effect of power loss due to that distance.

Once the uplink and downlink (*C/N*) are available, the overall (*C/N*)_{Total} of the satellite link at the receiving earth station can be calculated by

$$(C/N)_{Total} = \left[\left(\frac{C}{N}\right)_u^{-1} + \left(\frac{C}{N}\right)_d^{-1}\right]^{-1}$$

(8.21)

which is applicable **with absolute values only and not with dB values.** So before using above equation to calculate final *C/N*, uplink and downlink *C/N* values should be converted from dB to absolute and upon calculation again can be converted to dB value for (*C/N*)$_{Total}$.

Example 8.4 Consider a Ku-band satellite link with following specifications for uplink and downlink.

Uplink frequency = 14 GHz
Downlink frequency = 12 GHz
Bandwidth B = 36MHz = 75.6 dB-Hz
EIRP$_{ES, saturation}$ = 80dBW
EIRP$_{Sat, Saturation}$ = 44 dBW
(G/T)$_{satellite}$ = 1.6 dB/K
(G/T)$_{ES}$ = 34.3 dB/K
Boltzmann Constant k = 1.38×10^{-23} J/K = -228.6 dBW/K-Hz
Uplink slant range = 37,506 km
Downlink slant range = 37,506 km
Uplink path loss = 206.9 dB
Downlink path loss = 205.5 dB
Uplink tracking loss = 1.2 dB
Downlink tracking loss = 0.9 dB

Solution:
Using (8.15) for uplink and downlink separately

(*C/N*)$_U$ = (80dBW) + (1.6 dB/K) - (206.9 dB) - (-228.6 dBW/K-Hz) - (75.6 dB-Hz) - (1.2 dB)
= 26.5 dB = 446.68

(*C/N*)$_D$ = (44dBW) + (34.3 dB/K) - (205.5 dB) - (-228.6 dBW/K-Hz) – (75.6 dB-Hz) - (0.9 dB)
= 24.9 dB = 309.03

Therefore, (*C/N*)$_{Total}$ = [(1/446.68)+ (1/309.03)]$^{-1}$

$$= [0.002239 + 0.003236]^{-1}$$
$$= [0.005475]^{-1}$$
$$= 182.65$$
$$= 22.6 \text{ dB}$$

The satellite communication link is not only affected by noise but a numbers of interference signals may also affect its performance. The interference sources can be within the satellite communication systems or out of it. Some probable interferences are, adjacent satellite interference, terrestrial interference, cross-polarization interference, adjacent channel interference, intermodulation interference, and intersymbol interference. Similarly to carrier-to-noise ratio, carrier-to- interference ratio (C/I) can also be calculated for uplink and down link separately by estimating the interference signal power and finally overall (C/I)$_{Total}$ can be calculated using

$$(C/I)_{Total} = \left[\left(\frac{C}{I}\right)_u^{-1} + \left(\frac{C}{I}\right)_d^{-1}\right]^{-1}$$

(8.22)

Once the (C/I)$_{Total}$ is available, then overall carrier-to-noise-plus interference ration can be calculated using

$$\left(\frac{C}{N \, plus \, I}\right)_{Total} = \left[\left(\frac{C}{N}\right)_T^{-1} + \left(\frac{C}{i}\right)_T^{-1}\right]^{-1}$$

(8.23)

However, it should be again remembered that only absolute values should be used in all such calculations.

8.6 Transponders and Effects of Nonlinearity of Transponder

Transponder is the key payload of any communication satellite. The satellite in a broad sense is used a repeater station located in space and the device on-board the satellite that performs the amplification and frequency conversion is referred to as transponder. A satellite may carry a number of transponders depending upon its capacity design. Transponders may be classified into two types depending upon the manner in which they process the signal, (i) transparent or bent pipe transponder, (ii) regenerative transponder. Transparent transponders process only amplification and frequency conversion whereas regenerative transponders have an on-board processor for spectral shaping and even changing the modulation in addition to amplification and frequency conversion.

Most common frequency bands used for satellite communication are 6/4 GHz, 14/12 GHz where 6, 14 values are used for uplink and 4, 12 are used for downlink. Figures 8.4 and 8.5 show the block schematic of a transparent and a regenerative transponders respectively.
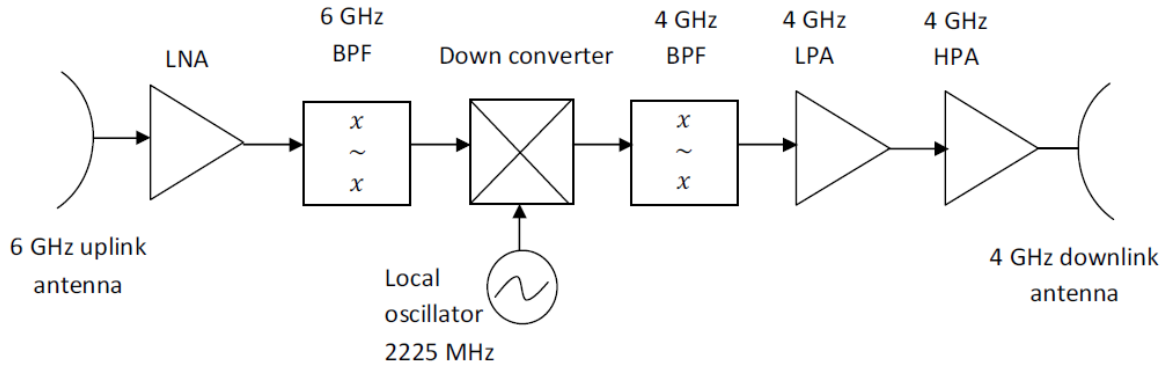
Figure 8.4: Simplified single conversion transponder (bent pipe) for 6/4 GHz band.
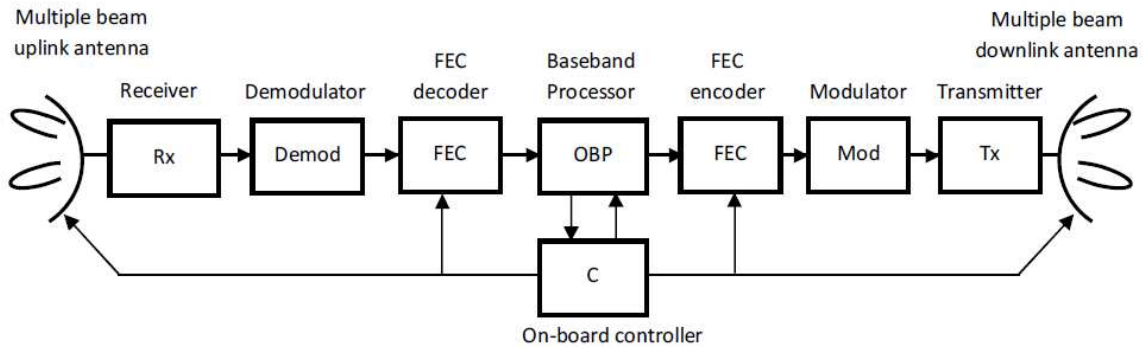
Figure 8.5: Regenerative type transponder with onboard processing

The difference between these two types can easily be seen in their block diagrams. Clearly regenerative transponders are advanced version of older bent-pipe transponders and provides much higher communication capacity because of additional onboard signal processing to provide spectral shaping and enhancing modulation efficiency. This results in higher spectral utilization. It can also support multibeam transmission further increasing the capacity through space domain multiple access (SDMA).

In any transponder, design of high power amplifier (HPA) is most critical task because high power amplifies inherently suffers from nonlinearity in their saturation regions. It simply means that if we operate HPA near to saturation level to draw peak power out of it the signals being amplified will beat and generate harmonics known as intermodulation products. This is very prominent interference especially in cases where multiple carries access the transponder. In order to avoid this, operating point is brought below the saturation level by reducing the uplink signal power. This is known as input back-off, BO_i. The input back-off results in corresponding output back-off, BO_o depending on the gain characteristic of HPA. BO_o is a nonlinear function of BO_i i.e. $BO_o = f(BO_i)$. This is phenomenon is explained in the figure 8.6.
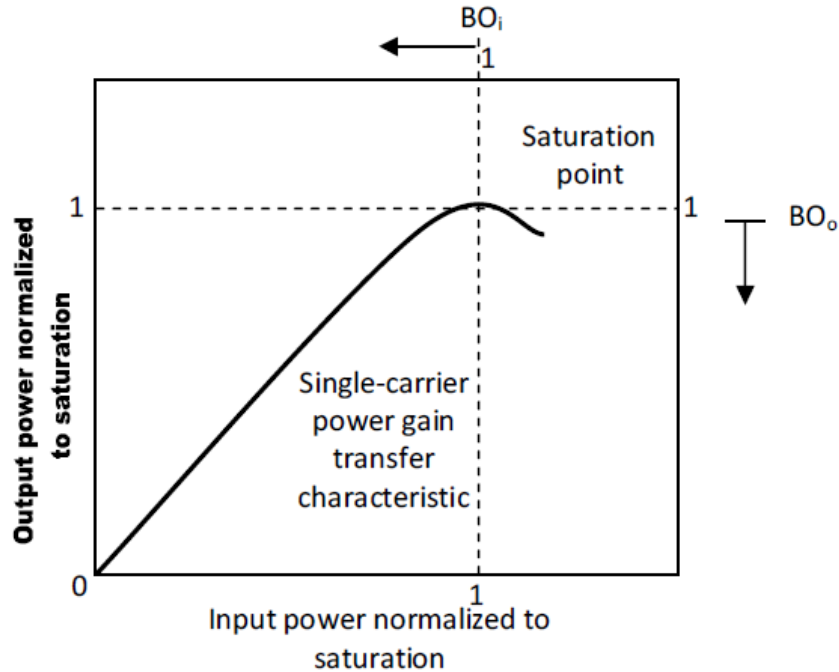
Figure 8.6 Nonlinear characteristic of a satellite TWTA (HPA).

Back-off is the ratio of saturation power level to operating power level and can be calculated for uplink and down link separately. In down link it will be output back-off which needs to be considered if the system has been pushed to back-off its power transmitted in uplink, i.e. if input power of the uplink signal has been reduced to prevent the HPA moving into saturation. For a given HPA, the output back-off

$$BO_0 = \frac{EIRP_{s,sat}}{EIRP_s} > 1$$

(8.24)

Where $EIRP_{s,sat}$ = saturation output power level of the HPA, and

$EIRP_s$ = actual or operating output power level of the HPA

Similarly, if the reduced transmitted power level to prevent HPA saturation is $EIRP_t$ the input back-off is given by

$$BO_i = \frac{EIRP_{s,sat}}{EIRP_t} > 1$$

(8.25)

Back-off can be calculated also in such cases when power levels are considered in flux density instead of EIRP power levels.

Under such cases where the link is operating with power back-off but specifications are given in saturation power level terms, we need to apply back-off while calculating the C/N. Thus, link budget equations for uplink and downlink are obtained as:

185

$$\left(\frac{C}{N}\right)_u = EIRF_{T,satur} + \left(\frac{G}{T}\right)_{R,Satellite} - L_{p,u} - L_{other,u} - k - B - BO_i$$
(8.26)

$$\left(\frac{C}{N}\right)_d = EIRP_{SAT,satur} + \left(\frac{G}{T}\right)_{R,ES} - L_{p,d} - L_{other,d} - k - B - BO_d$$
(8.27)

$$\left(\frac{C}{N}\right)_u = \Omega_u + (G/T)_{R,Satellite} - G_{1m^2} - L_{other,u} - k - B - BO_i$$
(8.28)

$$\left(\frac{C}{N}\right)_d = \Omega_d + (G/T)_{R,ES} - G_{1m^2} - L_{other,d} - k - B - BO_o$$
(8.29)

8.7 Multiple Access Techniques in Satellite Communication

Multiple access simply means providing access for utilization of a single resource to multiple users. In communication through satellite, the resource which provides the communication services is transponder, therefore, multiple access in satellite communication means sharing of transponder by number of users. These users may be located at different locations geographically and have their independent uplinks and downlinks. Commonly used multiple access techniques in any communication systems are named as:

1. Frequency division multiple access (FDMA)
2. Time division multiple access (TDMA)
3. Code division multiple access (CDMA)
4. Space division multiple access (SDMA)

CDMA is the technique which allows multiple users to avail entire bandwidth of the resource to be shared for all the time. This seems attractive from the point of view of sharing a resource without compromising on bandwidth availability and time availability, but the system becomes too complicated to offer any cost benefit in case of satellite communication. It suffers with two problems, first the near-far effect and cell breathing if used for mobile satellite communication. Therefore, in comparison to terrestrial communication using CDMA, satellite communication using CDMA is not very common. However, in navigation satellite services like global positioning system (GPS) it is used by some agencies in conjunction with FDMA, for example GLASNOSS series of Russian satellites use CDMA. This MA technique therefore will not be discussed further.

SDMA is the technique which permits frequency re-use primarily by transmitting multiple narrow beams in different directions so that different earth stations can be linked using the beam in its direction. If the earth stations are close enough to get affected by co-channel interference, the diversity through orthogonal antenna beams polarization. This technique usually used in conjunction with some other MA technique like FDMA or TDMA to provide

services to many users which requires concentration of signal at a specific location to avail SDMA benefits. We shall not discuss this technique also in further details.

8.7.1 Frequency division multiple access

In FDMA, different earth stations access the transponder bandwidth. Figure 8.7 shows the basic concept of FDMA.
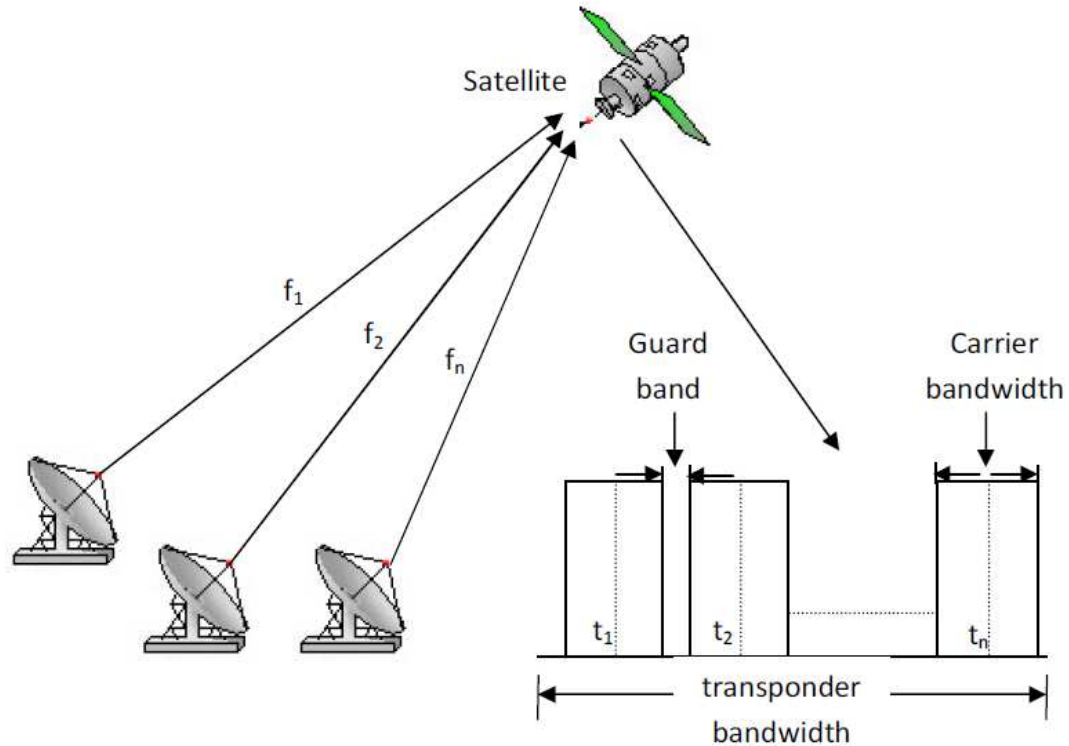

Figure 8.7: Basic concept of FDMA

FDMA scheme can be implemented in two possible ways.

(i) Using different carrier frequencies by different users in such a way that only part of total bandwidth is provided to a single user and the bandwidth demanded by them in total is within the total bandwidth offered by the transponder. Every user operates as independent link and each carrier is modulated independently. In this case the scheme is known as single channel per carrier (SCPC). The schematic diagram of SCPC system is shown in figure 8.8.
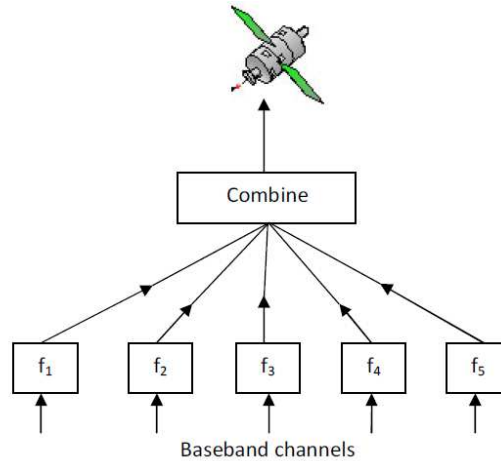
Figure 8.8: Transmission path for SCPC/FM/FDMA System.

The modulation scheme for transmission of signal can be analog or digital e.g. frequency modulation (FM) or phase shift keying (PSK). In such situations the FDMA is called SCPC-FM-FDMA or SCPC-PSK-FDMA. In case the link uses FM as modulation technique the relation between carrier-noise-ratio at the input of detector, C/N and signal-to-noise ratio at the output of detector, S/N is given by:

$$\frac{S}{N} = \frac{3}{2}\left(\frac{C}{N}\right)\left(\frac{B}{f_m}\right)\left(\frac{\Delta f}{f_m}\right)^2$$

(8.30a)

In dB values the same equation can be written as

$$\frac{S}{N}(dB) = 10\log\frac{3}{2} + \left(\frac{C}{N}\right)(dB) + 10\,\log\left(\frac{B}{f_m}\right) + 20\,\log\left(\frac{\Delta f}{f_m}\right)$$

(8.30b)

Where, B is carrier bandwidth after the carrier signal is modulated, f_m is frequency of modulating signal, and Δf is the frequency deviation provided in modulation process. It may be recalled that, approximation of resulting bandwidth can made by Carson's formula:

$$B = 2(\Delta f + f_m)$$ 　　　　　　　　　　　　　　　　　　　　　　　　　　　　　(8.31)

(ii) By multiplexing channels from different users through frequency division multiplexing (FDM) and then using this multiplexed larger baseband signal to modulate a single carrier and upon modulation the required bandwidth is equal to bandwidth offered by the transponder. In this situation the nomenclature used is known as multiple channels per carrier (MCPC). In such case, if modulation used is FM, the scheme is known as FDM-FM-FDMA or more specifically MCPC-FDM-FM-FDMA. This block schematic diagram of this type of MA is shown in figure 8.9.
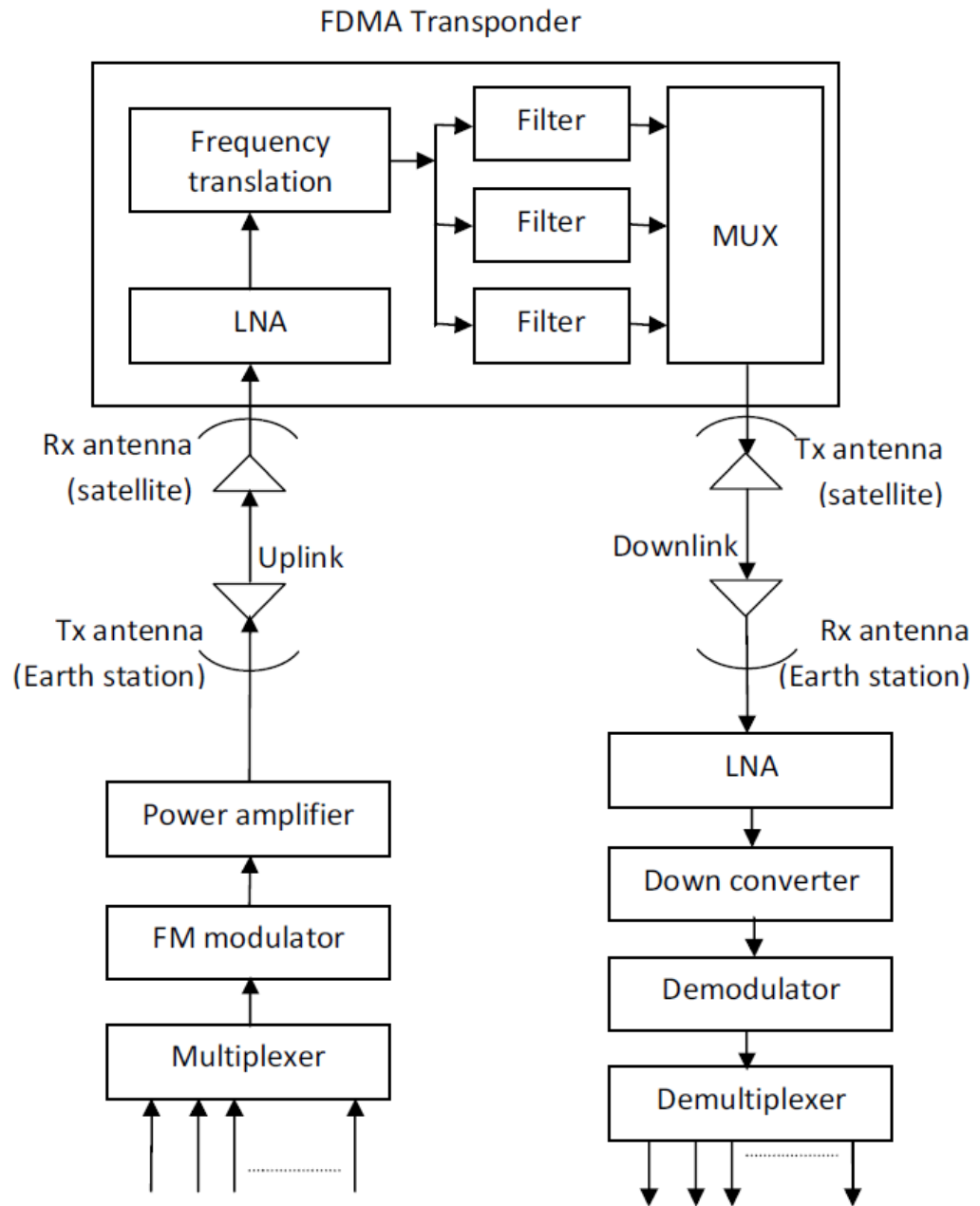
FDMA Transponder

Figure 8.9: Typical block diagram of MCPC/FDM/FM/FDMA System.

The relation between carrier-noise-ratio at the input of detector, C/N and signal-to-noise ratio at the output of detector, S/N is given by:

$$\frac{S}{N} = \frac{C}{N}\left(\frac{B}{b}\right)\left(\frac{f_m}{f_r}\right)^2$$

(8.32a)

In dB values the above equation can be written as

$$\frac{S}{N}(dB) = \left(\frac{C}{N}\right) dB + 10 log \left(\frac{B}{b}\right) + 20\, log \left(\frac{f_m}{f_r}\right)$$

(8.32b)

where, f_r is the 0-dBm test tone rms deviation of each multiplexed channel, f_m is the top channel FDM baseband frequency, and B is the carrier bandwidth which again can be calculated using Carson's rule but corresponding to peak deviation which is different in this case because of loading effect of multiplexing. Also, a peak factor is considered because the reference signal is taken as a single tone frequency and peak-to- rms value changes due to number of channels being multiplexed.

$$B = 2(\Delta f_{peak} + f_m)$$

where   (8.33)

$$\Delta f_{peak} = g.l.f_r$$ (8.34)

Here, g is the peak factor and assuming that if a large number of channels are multiplexed, the resulting baseband signal assumes Gaussian distribution and therefore its value can be taken as 3.16. In other words, the peak value is 3.16 times of rms value if the signal is Gaussian distributed. The loading factor l depends upon number of multiplexed channels, n and can be calculated as

$$l = log^{-1}[(-1 + 4\, log\, n)/20] \qquad\qquad \text{for } n < 240 \qquad\qquad (8.35)$$

$$= log^{-1}[(-15 + 10\, log\, n)/20] \qquad\qquad \text{for } n \geq 240 \qquad\qquad (8.36)$$

Example 8.5: Consider a SCPC-FM-FDMA system for a telephone channel with a specific channel $S/N = 33$ dB and test tone frequency deviation of 9.1 kHz. Assume peak frequency for telephone channel 3.4 kHz and channel bandwidth of 3.1 kHz. Find (a) carrier bandwidth and (b) C/N value in dB

Solution:
The bandwidth of the SCPC-FM-FDMA system is given by
$$B = 2(\Delta f_{peak} + f_m)$$
$$= 2(9.1\ kHz + 3.4 kHz)$$
$$= 25\ kHz.$$
(a)   F

or calculating (C/N) we may rewrite (8.30b) as

$$\frac{C}{N}(dB) = 10 log \frac{2}{3} + \left(\frac{C}{N}\right)(dB) + 10\, log \left(\frac{f_m}{B}\right) + 20\, log \left(\frac{f_m}{\Delta f}\right)$$

$$= 10 log \frac{2}{3} + 33\ dB + 10\, log \left(\frac{3.4}{25}\right) + 20\, log \left(\frac{3.4}{9.1}\right) \quad = 14\ dB$$

8.7.2 Time division multiple access

TDMA is a used to provide access to multiple users to utilize the transponder services on time sharing basis. Each user station can access the transponder in the given time slot within a structured frame. For that duration entire transponder bandwidth is made available to the user. Since, users are required to transmit only in their allocated time slot and their transmissions are called traffic bursts (TB) a strict transmit timing plan is followed by all users. In order to maintain transmission timing protocol a controlling station is required in the system which manages the access services by sharing the service control information with all users. The controlling station transmits a reference burst (RB) in each frame to enable users to extract reference timing and other control and management information. The traffic burst may further be divided into a number of information sub bursts (ISB) which may act as different channels within a station. The satellite, in turn, transmits all the received bursts frame by frame as a continuous stream and receiving stations extract their intended traffic bursts. The success of system operation heavily depends on agreement of all users and to avoid overlapping of TBs from different stations the system requires continuous synchronization information which is used by station to keep them adhered to the time plan shared.

Figure 8.10 shows the frame structure of a typical TDMA frame. It consists of one reference burst and a number of traffic bursts. The frame length is considered from beginning of one RB to just before the next following RB.
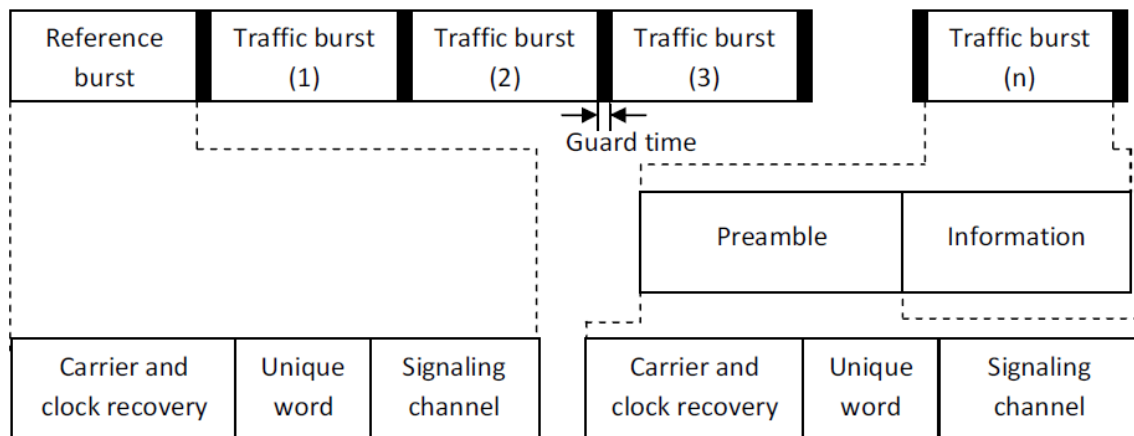

Figure 8.10: Typical TDMA Frame structure

The TDMA frame contains three distinct parts, reference burst, traffic burst, and guard time between any two bursts. The guard time enables the system to avoid any overlapping of traffic burst coming from different stations and reaching to the satellite with delays possible due to different path lengths and transmit timing inaccuracies at transmitting earth stations. The reference burst of TDMA frame does not contain any communication information signal. It contains only system operation and management information. The traffic burst contain two parts, one a preamble similar to reference burst and then rest part contains information signal.

The preamble of TB which precedes the information bits is used to synchronize the burst and to carry management and control information from traffic stations. It may be noted that TDMA as a scheme is based on dividing the time frame into number of slots, hence is best suited for digital signal formats where a defined time slot will have fixed number of bits. Therefore, frame length can be defined in terms of time measurement or in terms of number of bits.

Reference Burst and Traffic Burst Structures

As shown in figure 8.10, RB and preamble of TB contains three part, carrier and clock recovery (CCR) sequence, unique word (UW) and signaling channel. It is the signaling channel of both the bursts which differ with each other. While signaling channel of RB contains order wire channel (OWC), management channel (MC), and transmit timing channel (TTC), the signaling channel of TB contains OWC and service channel (SC).

Carrier and Clock Recovery Sequence

RB and TB both begin with a sequence of bits (or symbols) to enable earth station receiver synchronize the local oscillator frequency and phase and regenerate bit timing clock for data demodulation. Normally the sequence of alternate '0' and '1' is transmitted with total number of bits ranging from 300 to 400 is used for a high bit rate TDMA system.

Unique word

The unique word is a sequence of a particular pattern of bits that follows the CCR sequence in RB to provide the receive frame timing that allows a station to locate the position of a traffic burst in the frame. The UW in TB marks the timing of occurrence of TB and provides time reference to extract the wanted ISBs. The UW word pattern is chosen in such a way that it should have good auto correlation property. At the receiver end, the UW is declared detected when incoming bit stream is continuously correlated with a stored pattern of UW and if the correlator output crosses a threshold value at the end of last bit of UW in correlation a pulse is generated marking the beginning of frame in RB or TB as the case may be. In case, if any part of data in TB happens to resemble UW the UW detector can declare arrival of UW and the system may get confused and frame synchronization may lost. On the other hand if the UW suffers number of bit errors more than the threshold value set at detector the UW may not be detected and again frame synchronization is lost. To overcome first problem, if in the data any resemblance with UW is found it is changed to some extent by stuffing bits according to some known protocol and receiver can know about that bit stuffing has been done. To overcome second problem, a windowing method is used in which a small aperture window is created around expected time of presence of UW to look for it in that expected time window duration. UWs being detected outside of this window are discarded.

Signaling Channel of Reference Burst

In general, signaling channel of RB consists of three sub bursts as mentioned earlier. The OWC carry voice and teletype data through which instructions are passed to and from earth

stations. In fact the term OWC is drawn from manual telephony systems where operators used to communicate with each other using this channel.

The management channel is used by reference station to send frame management instructions to all traffic stations. This information contains burst time plan or any changes in it. It also carries monitoring and control messages for traffic stations.

The transmit timing channel carries acquisition and synchronization information to traffic stations necessary to them to adjust their transmit burst timing so that any possible overlapping is avoided when they transmit their own traffic bursts.

Signaling Channel of Traffic Burst

The signaling channel of TB contains OWC which is same as that of RB and a service channel. The service channel carries traffic station's status information to be communicated to reference station and other traffic stations such as high bit error rate and loss of unique word.

TDMA Frame Efficiency

 Total frame length of TDMA frame can be divided into parts, the length consumed by non-traffic data transmission length and actual traffic data transmission time. The non-traffic data is necessary to satisfactorily operating the entire system but does not contain any information communication which is the traffic between any pair of two earth stations establishing a link. Non-traffic data transmission time is overhead as it does not contribute to actual traffic transmission but it is necessary to run the system. The TDMA frame efficiency η is defined in percent as

$$\eta = \left(1 - \frac{T_x}{T_f}\right) X\ 100\ \%$$
(8.37)

Where T_x the overhead is portion of the frame and T_f is the total length of frame. Both these quantities are usually expressed in terms of number o bits. If there are n bursts in a frame, then overhead can be expressed as

$$T_x = nT_g + \sum_{i=0}^{n} T_{p,i}$$
(8.38)

Where T_g, is the guard time between bursts and $T_{p,i}$ is the preamble of i th burst.

Example 8.6: Consider a TDMA frame with following specifications:

Frame length = 15 ms
Burst bit rate = 90 Mbps
Number of stations = 20, each station transmits 2 TB and number of RB in frame are 2
CCR sequence length = 352 bits

UW sequence length = 48 bits

OWC sequence length = 510 bits

MC sequence length = 256 bits

TTC sequence length = 320 bits

Service channel sequence length = 24 bits

Guard time length = 64 bits

Solution:

Total number of bits in RB preamble = CCR + UW + OWC + MC + TTC

$$= 352+48+510+256+320$$

$$= 1486 \text{ bits}$$

Total number of bits in TB preamble = CCR + UW + OWC + service channel

$$= 352+48+510+24$$

$$= 934 \text{ bits}$$

Total number of overhead bits = (20+2) x 64 + 2 x 1486 + 20 x 934 = 23060 bits

Total number of bits in a frame = 15 x 10^{-3} x 90 x 10^6 = 1.35 x 10^6

Frame efficiency = $\left(1 - \frac{23060}{1350000}\right) x \ 100 \ \% $ = (1- 0.017) x 100 % = 0.9829 x 100 % = 98.29 %

8.8 Telemetry, Tracking, Command and Monitoring System

After having gone through the orbital mechanics, link design, and multiple access techniques used in satellite communication system, finally we shall discuss the telemetry, tracking, command and monitoring (TTC&M) system which is an essential part of any communication satellite. This caters to satellite management operations tasked to a control earth station. The main functions performed in satellite management include orbit and attitude control and the system responsible to perform these tasks consists of a telemetry receiver, tracking system, and Tele-command transmitter. A typical TTC&M system is shown in figure 8.11.
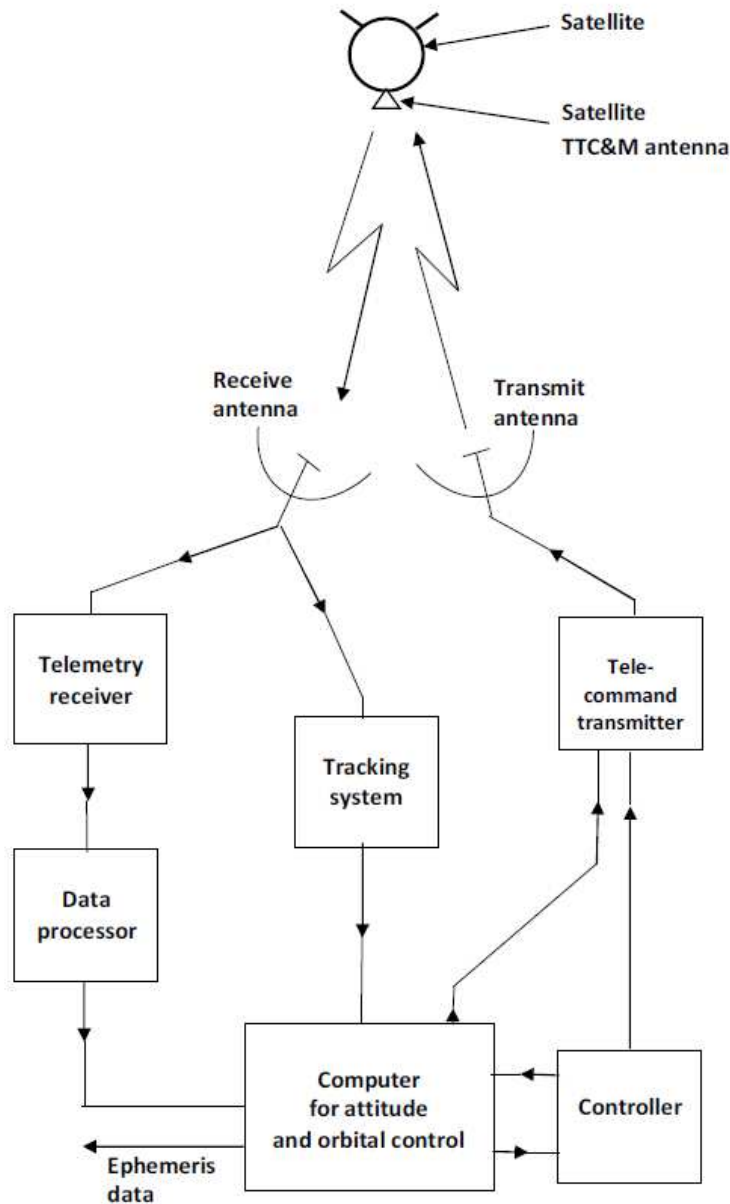
Figure 8.11: Typical tracking, telemetry, command and monitoring system.

As shown in the figure the satellite has a dedicated TTC&M link with its control earth station. The antenna employed at satellite for this link is usually a separate antenna other than the communication antenna. The control station earth station keeps an uplink and downlink established with the satellite continuously. The earth station consists of a telemetry receiver, a tracking system, a telecommand transmitter, a data processor and a controller. All these subsystems are connected to a computer for attitude and orbit control. Telemetry system through a data processor and tracking system provides the data to this central computer received from the satellite through its downlink. The computer also interacts with the controller and both these systems generate necessary commands which are transmitted through the tele-command transmitter via uplink. The system keeps all the data related to

satellite location, its orbital parameters and other health related data of satellite, called as ephemeris data received from central computer. This data is stored for a sufficiently large duration and used to predict the location and other orbital parameters of the satellite in near future. This helps in taking appropriate actions proactively in case of any emergent need

4.9 SUMMARY

In this unit we have studied about the communication satellite as a system. We discussed the orbits and orbital mechanics. We discussed how path loss affects the signal and how it can be calculated between any points. We also studied description of a satellite link and came to know about uplink and downlink. We saw how satellite link calculations are made. Transponders and effects of nonlinearity of transponder was also discussed and learned to prevent intermodulation interference how the uplink is backed-off resulting in downlink back-off too. This unit also discussed two main multiple access techniques in satellite communication i.e. frequency division multiple access and time division multiple access. The unit ended with description of telemetry, tracking, command and monitoring system.

4.10 References text books and Suggested Readings

1. Digital Satellite Communications, Tri T Ha, McGraw-Hill Publishing Company

2. Satellite Communications, Timothy Pratt, Charles Bostian and Jeremy Allnut, John Wiley & Sons

3. Satellite Communications, Anil K Maini and Varsha Agrawal, Wiley India Pvt. Ltd.

4. Satellite Communication Principles and Applications, R. N. Mutagi, Oxford University Press.

5. Satellite Communications Systems, Gerard Maral and Michel Bousquet, Wiley India Pvt. Ltd.

6. https://nptel.ac.in/courses/117/105/117105131/#
    Video Lectures: NPTEL Certificate Course on Satellite Communication by Prof. Kalyan Kumar Bandhyopadhyay

4.11 Terminal Questions and Answers

Self Assessment Questions
1. A transponder is a satellite equipment which
    A. receives a signal from Earth station and amplifies

B. changes the frequency of the received signal

C. retransmits the received signal

D. does all of the above-mentioned function

2. A geosynchronous satellite

A. has the same period a that of the Earth

B. has a circular orbit

C. rotates in the equatorial plane

D. has all of the above

3. The quality of a space-link is measured in terms of the _____ ratio.

A. C/N

B. S/N

C. G/T

D. EIRP

4. While keeping the down-link frequency constant, the diameter of a satellite antenna is reduced by half. To offer the same EIRP over the increased coverage area, the RF output power has to be increases by a factor of

A. 2

B. 4

C. 8

D. 16

5. The multiple access technique suitable only for digital transmission is

A. TDMA

B. FDMA

C. Both TDMA and FDMA

D. Packet Access

6. For an elliptical orbit, the value of eccentricity is given by

A. $0 < e < 1$

B. $e = 1$

C. $e = 0$

D. None of the other mentioned options

7. Apogee means

A. The point nearest from earth

B. The point farthest from earth

C. The point smallest from earth

D. None of the other mentioned options

8. Perigee means

A. The point farthest from earth

B. The point longest from earth

C. The point closest approach to earth

D. None of the other mentioned options

9. Ascending node means
   A. The point where the orbit crosses the equatorial plane going from south to north
   B. The point longest from earth
   C. The point closest approach to earth
   D. None of the other mentioned options

10. In an elliptical orbit the velocity of satellite at apogee is_____than the velocity of satellite at perigee.
    A. Higher
    B. Lower
    C. Equal
    D. Has no relation with velocity at perigee

Answers 1-D, 2-D, 3- A, 4-B, 5-A, 6-A, 7-B, 8-C, 9-A, 10-B

Short Answer Type Questions:
1. Name types of orbits used for satellite communication
2. What are Azimuth and elevation angles? Define with proper diagram.
3. Why uplink frequency is higher than downlink frequency?
4. Explain basic principle of FDMA.
5. Draw the TDMA frame and label it

Numerical Problems
1. A satellite is in a 322 km high circular orbit. Determine
   a) The orbital angular velocity in radians per second
   b) The orbital period in minutes; and
   c) The orbital velocity in kilometers per second.
      (Ans- a): 0.0011512 rad/s, b):90.97 minutes, c): 7.713 km/s)

2. A TDMA system operates at 100M bits/s with a 2ms frame time. Assume that all slots are of equal length and guard time 1 micro sec is required between slots. Compute the efficiency of the TDMA system if total 10 slots per frame are used.
   (Ans- 99.5%)

3. A satellite at a distance of 36,000km from earth radiates a power of 5W from an antenna with a gain of 16dB. Find the power received in dBW by an earth station antenna with gain of 45dB. The operating frequency is 11 GHz.
   (-136.38 dBW)

Long answer type questions
4. What are the elements of satellite communication? Explain each of them with a suitable block diagram.
5. List the orbital elements of a satellite and briefly explain them
6. Compare FDMA and TDMA techniques identifying their merits and demeris.

7. Discuss TTC&M system in detail with the help of a block diagram.