MIT(CS)-404

Computer Organization and Architecture

Block-1

Unit-1

Introduction to Computer Organization and Architecture, Basic Computer Model and different units of Computer, Basic Working Principle of a Computer , Main Memory Organization ,Memory Instruction , Central Processing Unit, Input Output Device

Unit-2

Binary Number System ,Representation of Unsigned Integers, Signed Integer, Representation of signed integer , The concept of complement ,Diminished Radix Complement ,Representation of Signed integer in 1's complement form, Representation of Signed integer in 2's complement form, Representation of Real Number ,Fixed-point representation, Floating-point representation, IEEE standard floating-point format ,Representation of Character

Unit-3

Introduction to Computer Architecture, The Brief History of Computer Architecture, First Generation (1940-1950): Vacuum Tube, Second Generation (1950-1964)Transistors, Third Generation (1964-1974): Integrated Circuits (IC), Fourth Generation (1974-Present): Very Large-Scale Integration (VLSI) / Ultra Large Scale Integration (ULSI), Evolution of Instruction Sets, history of Computer Organization, The advance of microprocessor (Intel), Evolution of Memory ,Major buses and their features, Major ports and connectors/interface.

Unit-4

Introduction to Arithmetic Circuit, Binary Adder , Full Adder, Binary Subtractor , Multiplication Binary Multiplier, Hardware Implementation , Concept of memory ,Register,

Block-2

Unit-5

Cache Memory ,Main Memory, Magnetic Disk ,Removable Media, Main Memory, Binary Storage Cell ,One-bit Binary Cell (BC) , Dynamic Ram (DRAM), Static RAM (SRAM), SRAM

Versus DRAM, Internal Organization of Memory Chips , Cache Memory ,Operation of Cache Memory ,Mapping Functions, Direct Mapping Technique, Associated Mapping Technique , Block-Set-Associative Mapping Technique, Replacement Algorithms, Least Recently Used (LRU) ,Replacement policy, First In First Out (FIFO) replacement policy ,Random replacement policy

Unit-6

Main Memory, Memory Management , swapping, Partitioning ,Fixed sized partitions, Variable size Partition

Unit-7

Paging , Virtual Memory ,Address Translation, Inverted page table ,Translation Look aside Buffer (TLB)

Unit-8

Addressing Modes, Immediate Addressing, Direct Addressing, Indirect Addressing Register Addressing, Register Indirect Addressing , Displacement Addressing, Relative Addressing, Base-Register Addressing, Indexing, Stack Addressing

Block-3

Unit-9

Machine Instruction, Instruction Representation, Instruction Types, Data Processing, Data Storage, , Data Movement, Control, Number of Addresses, Instruction Set Design, Types of Operands ,Types of Operations, ,Data Transfer, Arithmetic, Logical, Conversion, Input/ Output , ,System Control ,Transfer of Control, ,Branch Instruction, Skip Instruction , Procedure Call Instruction, Instruction Format, Instruction Length, Allocation of Bits

Unit-10

Introduction to CPU, Register Organization, User-visible Registers CPU Register Organization, Processor Status Word, Concept of Program Execution

Unit-11

Processor Organization, Storing a word into memory, Register Transfer Operation, Performing the arithmetic or logic operation, Multiple Bus Organization, Execution of a Complete Instructions, Branching

Unit-12

Design of Control Unit, Control Unit Organization, Programmable Logic

Block-4

Unit-13

Micro programmed Control, Control Word (CW), Grouping of control signals, Microprogram Sequencing, Sequencing Techniques, Two Address fields, Single address field, Variable format ,Address Generation

Unit-14

Input/ Output Organization, Input /Output Modules, Control & timings, Processor & Device Communication , Input / Output Subsystem ,Input/Output Port

Unit-15

Programmed I/O, I/O Commands, Interrupt driven I/O, Interrupt Processing, Interrupt driven I/O,Interrupt Processing, Return from Interrupt ,Design Issues for Interrupt ,Device Identification ,Multiple Interrupts Lines, Software Poll ,Daisy Chain, Bus Arbitration ,Handling multiple interrupts, Interrupt Nesting, Direct Memory Access, Single bus, detached DMA - I/O configuration, Single bus, Integrated DMA - I/O configuration, Using separate I/O bus

Unit-16

Concept of Buses, Synchronous Bus, Multiple Cycle Transfer, Asynchronous Bus

Unit-17

External Memory, Magnetic Disk , Physical characteristics of disk , Organization and accessing of data on a disk, Disk Operation, Disk Performance Parameter, Data Striping, Redundancy ,RAID levels

Block-5

Unit-18

Operations, Operands, Procedure Call, Characteristics of Reduced Instruction Set Architecture One machine instruction per machine cycle, Register –to– register operations, Simple Addressing Modes, Simple Instruction Format

Unit-19

Design Issues of RISC, Register Window, Global Variables, Compiler based Register Optimization, Large Register file versus cache

Unit-20

Introduction to Pipeline Processor, Performance Issues, Branching

Unit-21

Parallel Processing, Interconnection Networks